29C532E

32-Bit Bus-Watch EDAC
Error Detection And Correction unit

1. Description

The 29C532E EDAC is a very low power bus-watch 32-bit Error Detection And Correction unit (EDAC). EDAC is used in a high integrity system for monitoring and correcting data values coming from the memory space. Such a bus-watch EDAC is connected as a peripheral on the data bus and watches on and controls the integrity of the data memory.

During a processor write cycle, at each memory location (32-bit width), EDAC calculated checkword (7 or 8-bit width) is added. When performing a read operation from memory, the 29C532E verifies the entire checkword and data combination. It detects and can correct 100% of all the single-bit errors and it detects all multi-bit errors but can not correct them. All the errors are reported to the master system to allow the processor to take action as required. In case of single-bit error, the Correctable ERRor flag is set and the single-bit in error is complemented (corrected). Then, the data can be substituted to the corrupted data on the system data bus. In case of multi-bit error, the Non-Correctable ERRor flag is set, the data can not be repaired. Note that when multi-bit errors occur, there are some bit patterns which may appear as possible correctable errors. Therefore, if the environment produces this type of error, the EDAC must be used in detect-only-without-correction configuration. Data and syndrome analysis must be rapidly done.

Because the 29C532E latches the data, byte or 16-bit word write operations are possible if they take place in a read-modify-write accesses to the memory space.

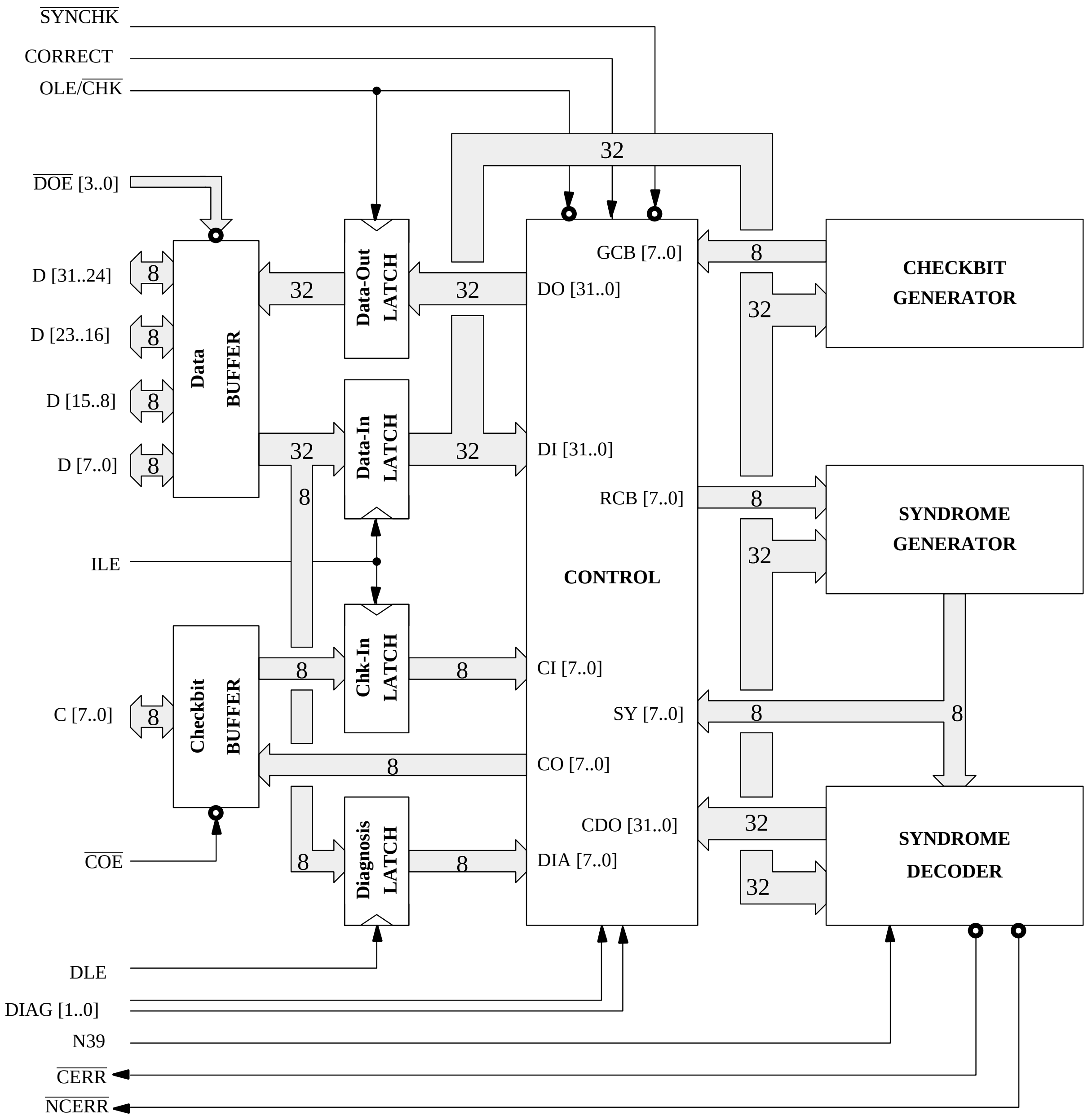
When the 29C532E uses 7-checkbit, it can detect any errors on any single 1 or 4-bit memory chip. The 8-checkbit option gives the additional capability to detect all errors on any 8-bit memory chip.

2. Features

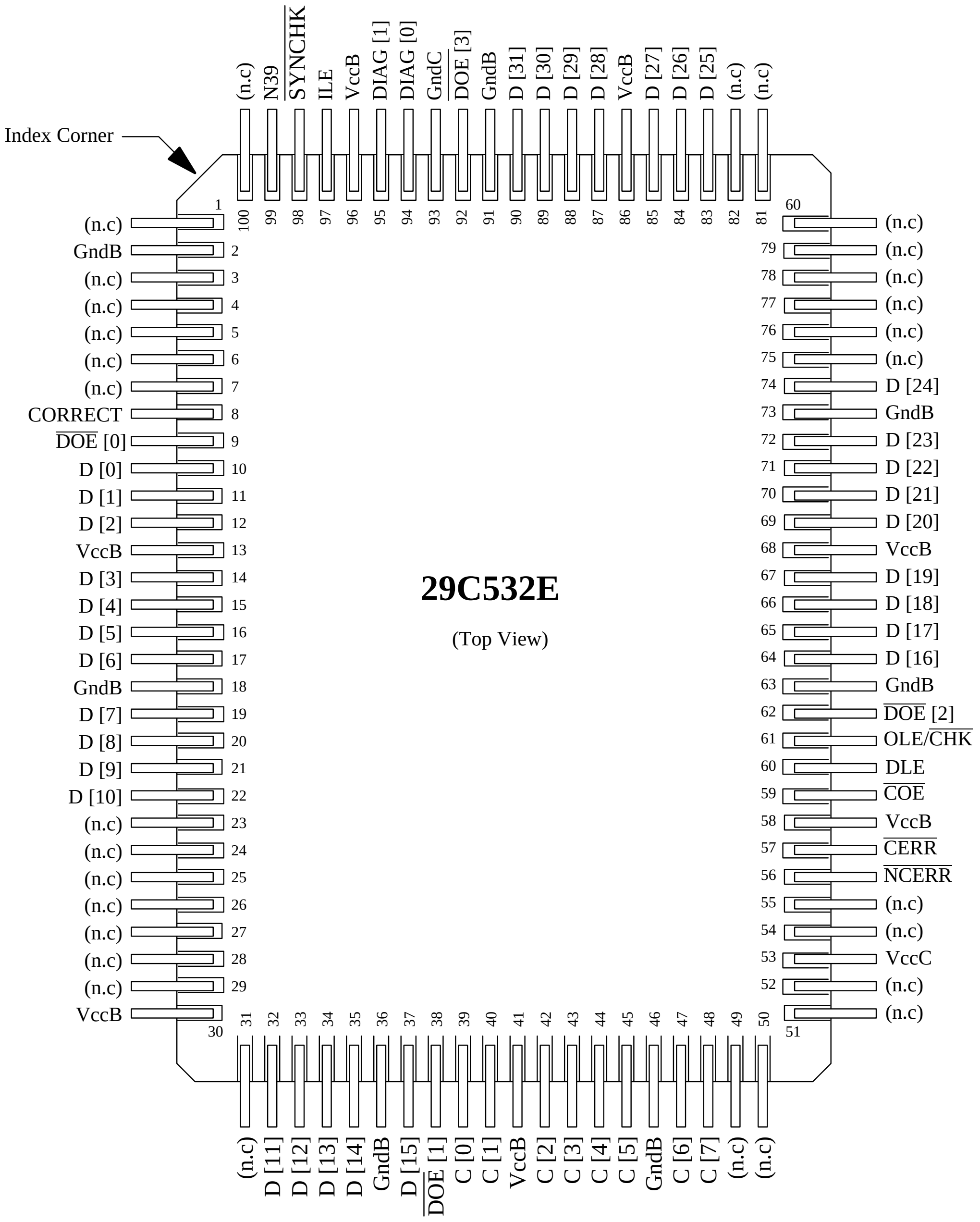
- 32-bit Operation (7 or 8 Check Bits)
- Bus Watch Architecture
- Fast Error Detection: 32 ns
- Fast Error Correction: 39 ns
- Corrects All Single-Bit Errors
  Detects All Double-Bit Errors
  Detects Some Multi-Bit Errors
  Detects Chip Error (x1, x4 & x8 RAM Format)
- Correctable and Non-Correctable Error Flags
- Very Low Power CMOS
- TTL Compatible
- Single 5V ± 10% Power Supply
- High Drive Capability on Bus: 12.8 mA
- 100-Pin Multi-Layer Quad Flatpack

3. Interface

3.1. Block Diagram



3.2. Pin Configuration



3.3. Pin Description

Name	Pin Nb.	I/O	Active	Description
Buses				
D [31..24]	90, 89, 88, 87, 85, 84, 83, 74	I/O	-	Data bus. Output data on D [31..24] bus is controlled by $\overline{\text{DOE}}$ [3]. Output data on D [23..16] bus is controlled by $\overline{\text{DOE}}$ [2]. Output data on D [15..8] bus is controlled by $\overline{\text{DOE}}$ [1]. Output data on D [7..0] bus is controlled by $\overline{\text{DOE}}$ [0].
D [23..16]	72, 71, 70, 69, 67, 66, 65, 64			
D [15..8]	37, 35, 34, 32, 31, 22, 21, 20			
D [7..0]	19, 17, 16, 15, 14, 12, 11, 10			
C [7..0]	48, 47, 45, 44, 43, 42, 40, 39	I/O	-	Checkbit bus. Output checkbit on C [7..0] bus is controlled by $\overline{\text{COE}}$.
Flags				
$\overline{\text{CERR}}$	57	O	Low	Correctable ERror.
$\overline{\text{NCERR}}$	56	O	Low	UnCorrectable ERror.
Controls				
$\overline{\text{DOE}}$ [3]	9	I	Low	Data Output Enable for D [31..24] bus.
$\overline{\text{DOE}}$ [2]	38			Data Output Enable for D [23..16] bus.
$\overline{\text{DOE}}$ [1]	62			Data Output Enable for D [15..8] bus.
$\overline{\text{DOE}}$ [0]	92			Data Output Enable for D [7..0] bus.
$\overline{\text{COE}}$	59	I	Low	Checkbit Output Enable for C [7..0] bus.
OLE/$\overline{\text{CHK}}$	61	I	H/L	OLE: Output Latch Enable for DO [31..0] internal bus: 1: transparent, 0: latched. $\overline{\text{CHK}}$: CHecKbit enable. Only if DIAG [0] = 0 (non active): 0: CO [7..0] = GCB [7..0]. 1: CO [7..0] = SY [7..0].
ILE	97	I	High	Input Latch Enable to produce DI [31..0] and CI [7..0] internal buses respectively from D [31..0] and C [7..0]: 1: transparent, 0: latched.
DLE	60	I	High	Diagnosis Latch Enable to produce DIA [7..0] internal bus from D [7..0] bus: 1: transparent, 0: latched.

Name	Pin Nb.	I/O	Active	Description
Controls				
$\overline{\text{SYNCHK}}$	98	I	Low	SYNdrome & CHecKbit enable. During a read mode: 0: DO [31..24] = DIA [7..0], DO [23..16] = SY [7..0], DO [15..8] = CI [7..0], DO [7..0] = DIA [7..0]. 1: DO [31..0] = CDO [31..0].
CORRECT	8	I	High	CORRECTion enable. Only if $\overline{\text{SYNCHK}}$ = 1 (non active): 1: DO [31..0] = CDO [31..0]. 0: DO [31..0] = DI [31..0].
N39	99	I	High	Code leNgth equals 39: 1: the EDAC uses 7 check bits. 0: the EDAC uses 8 check bits.
DIAG [1]	95	I	High	DIAGnosis mode 1. Diagnosis detect & correct: 1: RCB [7..0] = DIA [7..0]. 0: RCB [7..0] = CI [7..0].
DIAG [0]	94			DIAGnosis mode 0. Diagnosis generate: 1: CO [7..0] = DIA [7..0]. 0: CO [7..0] = SY [7..0] or GCB [7..0] following the OLE/$\overline{\text{CHK}}$ value.
Power (Buffers)				
Vcc$_B$	13, 30, 41, 58, 68, 86, 96	-	-	Buffers supply (5V nominal)
Gnd$_B$	2, 18, 36, 46, 63, 73, 91	-	-	Buffers 0V reference
Power (Core)				
Vcc$_C$	53	-	-	Core supply (5V nominal)
Gnd$_C$	93	-	-	Core 0V reference

All I/O and I buffers have a pull-up resistor $\simeq$ 100 Ω.

4. Checkbit Generation

The checkbit generator produces 8 checkbits (whatever N39 value) from the incoming data DI [31..0] according the following table.

Table 1: Checkbit generation (x indicates bit of D [31..0] used in the parity calculation)

GCB [7..0]	Parity	DI [31..0]																															
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Even (XOR)	x	x	x	x				x			x	x	x				x				x	x	x	x			x	x			x	
1	Even (XOR)		x		x			x	x				x			x	x	x		x	x			x	x	x	x		x	x			
2	Odd (NXOR)	x					x				x			x	x		x	x	x				x		x		x	x	x	x	x	x	
3	Even (XOR)	x	x			x				x	x			x				x	x	x	x		x	x	x	x			x				x
4	Odd (NXOR)		x	x		x	x	x	x			x		x		x					x		x	x					x	x	x		x
5	Even (XOR)	x					x	x		x		x	x		x				x	x		x	x	x	x		x	x					x
6	Even (XOR)	x	x	x	x	x				x	x			x	x	x	x	x				x				x					x	x	
7	Odd (NXOR)					x	x	x	x		x	x				x	x		x		x	x				x	x				x	x	x

<u>Example</u>

To create GCB [3], bit 31, 30, 27, 23, 22, 19, 15, 14, 13, 12, 10, 9, 8, 7, 4 and 0 of DI [31..0] are 3ORed together.If SRAM devices 1 or 4-bit are used in a memory system controlled by the 29C532E EDAC, it is only necessary to store 39 bits (D [31..0] & C [6..0]).If SRAM devices 8-bit are used in a memory system controlled by the 29C532E EDAC, 40 bits (D [31..0] & C [7..0]) must be stored.

5. Syndrome Generation

The syndrome generator produces 8 syndrome-bits (whatever N39 value) from the incoming data DI [31..0] and the associated checkbit RCB [7..0] (via CI [7..0] or DIA [7..0] following DIAG [1] value) according the following table.

Table 2: Checkbit generation (x indicates bit of D [x1..0] used in the parity calculation)

SY [7..0]	**Parity**	**DI [x1..0]**																				
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	18	17	16	15	14	1x	12
0	Even (XOR)	x	x	x	x				x			x	x	x					x			
1	Even (XOR)		x		x			x	x				x				x	x	x		x	x
2	Odd (NXOR)	x					x				x			x	x	x		x	x	x		
3	Even (XOR)	x	x			x				x	x			x					x	x	x	x
4	Odd (NXOR)		x	x		x	x	x	x			x		x			x					x
5	Even (XOR)	x					x	x		x		x	x		x	x				x	x	
6	Even (XOR)	x	x	x	x	x				x	x			x	x	x	x	x	x			
7	Odd (NXOR)					x	x	x	x		x	x					x	x		x		x

Table 2: (continue)

SY [7..0]	Parity	DI [x1..0]												Parity	RCB [7..0]							
		11	10	9	8	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
0	Even (XOR)	x	x	x	x			x	x			x		Evn (XOR)								x
1	Even (XOR)			x	x	x	x		x	x				Even (XOR)							x	
2	Odd (NXOR)		x		x		x	x	x	x	x	x		Even (XOR)						x		
3	Even (XOR)		x	x	x	x			x				x	Even (XOR)					x			
4	Odd (NXOR)		x	x					x	x	x		x	Even (XOR)				x				
5	Even (XOR)	x	x	x	x		x	x					x	Even (XOR)			x					
6	Even (XOR)	x				x					x	x		Even (XOR)		x						
7	Odd (NXOR)	x				x	x				x	x	x	Even (XOR)	x							

The syndrome bit SY[x] is the XOR of the received checkbit RCB[x] and the parity calculation on DI [31..0].

Example:

To create SY [1], bit 30, 28, 25, 24, 20, 17, 16, 15, 13, 12, 9, 8, 7, 6, 4 and 3 of DI [31..0] are NXORed together. Then, the result is XORed with the associated checkbit RCB [1] of the checkbit byte read at the same address than the data word DI [31..0].

If SRAM devices 1 or 4-bit are used in a memory system controlled by the 29C532E EDAC, only 39 bits (D [31..0] & C [6..0]) are checked and the generated syndrome word is 7-bit width.

If SRAM devices 8-bit are used in a memory system controlled by the 29C532E EDAC, 40 bits (D [31..0] & C [7..0]) are checked, the generated syndrome word is 8-bit width.

6. Syndrome Decoding

The syndrome decoder generates the error flags $\overline{\text{CERR}}$ (Correctable ERror) and $\overline{\text{NCERR}}$ (Non-Correctable ERror). It mainly provides corrected data word to the system bus if a correctable error occurs.

In case of single bit-error, using the syndrome value, this block decodes which bit is in error and complements it to correct the data word. This correction is only made on the 32 bits of data not on the checkbit word.

The inputs of the syndrome decoder are:

- the 32 bits of data coming from the system data bus,
- the syndrome coming from the syndrome generator,
- the control signal N39. N39 signal controls if 39 or 40 bits will be decoded from the entire word.

Table 3: 7-bit syndrome word to bit-in-error (N39=1)

Syndrome bit SY [7..0]				hex	0	1	2	3	4	5	6	7
				7	0	0	0	0	0	0	0	0
				6	0	0	0	0	1	1	1	1
				5	0	0	1	1	0	0	1	1
hex	3	2	1	4 0	0	1	0	1	0	1	0	1
0	0	0	0	0	N.E.D	C [4]	C [5]		C [6]		D[11]	
1	0	0	0	1	C [0]			D[21]		D[29]		
2	0	0	1	0	C [1]			D[25]		D[17]		
3	0	0	1	1		D[24]	D[20]		D[28]			
4	0	1	0	0	C [2]			D[26]		D[2]	D[18]	
5	0	1	0	1			D[5]		D[1]			
6	0	1	1	0		D[3]	D[6]		D[16]			
7	0	1	1	1								
8	1	0	0	0	C [3]			D[0]		D[27]	D[23]	
9	1	0	0	1								
A	1	0	1	0		D[12]	D[13]		D[7]			
B	1	0	1	1				D[9]		D[30]		
C	1	1	0	0			D[14]		D[22]			
D	1	1	0	1				D[10]		D[19]	D[31]	
E	1	1	1	0								
F	1	1	1	1		D[4]	D[8]		D[15]			

Note: N.E.D = No Error Detected,

D [x] = Data bit–in–error,

C [x] = Check bit–in–error

▨ = Multi–bit–in–error

Table 4: 8-bit syndrome word to bit-in-error (N39=0)

Syndrome bit SY [7..0]				hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
hex	3	2	1	4 0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	0	0	0	0	N.E.D	C [4]	C [5]	▨	C [6]	▨	▨	▨	C [7]	▨	▨	▨	▨	▨	D[11]	▨
1	0	0	0	1	C [0]	▨	▨	▨	▨	D[29]	▨	▨	▨	▨	▨	D[21]	▨	▨	▨	▨
2	0	0	1	0	C [1]	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	D[25]	▨	D[17]	▨	▨
3	0	0	1	1	▨	▨	D[20]	▨	D[28]	▨	▨	▨	▨	D[24]	▨	▨	▨	▨	▨	▨
4	0	1	0	0	C [2]	▨	▨	▨	▨	▨	D[18]	▨	▨	▨	▨	D[26]	▨	D[2]	▨	▨
5	0	1	0	1	▨	▨	D[5]	▨	▨	▨	▨	▨	▨	▨	▨	▨	D[1]	▨	▨	▨
6	0	1	1	0	▨	D[3]	▨	▨	▨	▨	▨	▨	▨	▨	D[6]	▨	D[16]	▨	▨	▨
7	0	1	1	1	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨
8	1	0	0	0	C [3]	▨	▨	▨	▨	▨	D[23]	▨	▨	▨	▨	D[0]	▨	D[27]	▨	▨
9	1	0	0	1	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨
A	1	0	1	0	▨	▨	D[13]	▨	▨	▨	▨	▨	▨	D[12]	▨	▨	D[7]	▨	▨	▨
B	1	0	1	1	▨	▨	▨	D[9]	▨	D[30]	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨
C	1	1	0	0	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	D[14]	▨	D[22]	▨	▨	▨
D	1	1	0	1	▨	▨	▨	D[10]	▨	D[19]	D[31]	▨	▨	▨	▨	▨	▨	▨	▨	▨
E	1	1	1	0	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨
F	1	1	1	1	▨	D[4]	D[8]	▨	D[15]	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨

Note : N.E.D = No Error Detected,
D [x] = Data bit–in–error,
C [x] = Check bit–in–error
▨ = Multi–bit–in–error

7. 7-Bit Syndrome Word

This feature is available when the N39 pin is driven at a high level.

7.1. No Error

If there is no error in the read data or checkbit, all the syndrome word is ”00”. The EDAC flags are inactive.

No Error	SY= 0x00

7.2. Single Bit-In-Error

When the Memory Data word (D [31..0] & C[6..0]) read has one bit-in-error, the 20C532E EDAC develops a code (syndrome) which indicates the bit in error (each bit have its own syndrome value). In this case, the syndrome decoder sets low the correctable error flag $\overline{\text{CERR}}$, but $\overline{\text{NCERR}}$ flag remains at high level.

In case of single bit-error on D [31..0], if the control lines $\overline{\text{SYNCHK}}$ = non active and CORRECT = active, the corrected value (CDO [31..0]) is available on DO [31..0] internal bus and the syndrome word is available on CO [6..0]. The corrected value is obtains to complement the bit-in-error.

In same conditions, if a single bit-error occurs on C [6..0], the corrected value of the checkbit is not available in the device.

Table 5: 7-bit syndrome word for single bit-error.

D[31..16]	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SY	0x6D	0x5B	0x51	0x4x	0x58	0x34	0x32	0x13	0x68	0x4C	0x31	0x23	0x5D	0x64	0x52	0x46
D[15..0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SY	0x4F	0x2C	0x2A	0x1A	0x60	0x3D	0x3B	0x2F	0x4A	0x26	0x25	0x1F	0x16	0x54	0x45	0x38

C[7..0]	-	6	5	4	3	2	1	0
SY	- -	0x40	0x20	0x10	0x08	0x04	0x02	0x01

7.3. Double Bit-In-Error

When the Memory Data word (D [31..0] & C[6..0]) read has two bit-in-error, the 20C532E EDAC develops a syndrome different of 0x00. The syndrome value generated by a double bit-in-error never takes place of a syndrome value generated by a single bit-in-error. In this case, the syndrome decoder sets low the non correctable error flag $\overline{\text{NCERR}}$ and $\overline{\text{CERR}}$ flag remains at high level.

Example :

If data D [12] and D [9] are incorrect, syndrome bit SY [5] and SY [0] are set to one (SY= 0x21), $\overline{\text{NCERR}}$ flag is set low ($\overline{\text{CERR}}$ flag remains at high level).

7.4. Triple Bit-In-Error

When the Memory Data word (D [31..0] & C[6..0]) read has three bit-in-error, the 20C532E EDAC develops a syndrome different of 0x00. The syndrome value generated by a triple bit-in-error can have any value, even a syndrome value normally generated by a single bit-in-error. $\overline{\text{NCERR}}$ flag or $\overline{\text{CERR}}$ flag can be activated following the value of the generated syndrome.

Example :
If data D [28], D [18] and D [1] are incorrect, syndrome bit SY [6], SY [5] and SY [1] are set to one (SY= 0x62), $\overline{\text{NCERR}}$ flag is set low ($\overline{\text{CERR}}$ flag remains at high level).

Fault example :
If data D [24], D [12] and D [3] are incorrect, syndrome bits SY [4..0] are set to one (SY= 0x1F). The syndrome is decoded by the 29C532E EDAC has being a correctable error on D [4]. Then, $\overline{\text{CERR}}$ flag is set low and $\overline{\text{NCERR}}$ flag remains at high level. A correction would cause more errors.

7.5. Multi Bit-In-Error

When the Memory Data word (D [31..0] & C[6..0]) read has four or more bit-in-error, the 20C532E EDAC develops a non controlled syndrome. This syndrome can take any value, from 0x00 (No Error Detected) to specific syndrome value of single bit-in-error .

Example :
If the data read = 0x00000000 instead of 0xFFFFFFFF, the generated syndrome is 0x00. Then, no error flag is actived.

7.6. 4-Bit Wide Memory Error

The 7 checkbit code can be used to provide error detection for up to four errors occuring in the following fields:

- D [31..28],
- D [27..24],
- D [23..20],
- D [19..16],
- D [15..12],
- D [11..8],
- D [7..4],
- D [3..0],
- C [6..4],
- C [3..0].

The 29C532E EDAC can flag any number of errors in 4-bit wide memory chip. If the one device returns from one to four bit-in error, the $\overline{\text{CERR}}$ and $\overline{\text{NCERR}}$ flags are generated following the error type and the generated syndrome takes a value which never overlaps the code of a single bit-in-error. This is a restriction to triple and multi bit-in-error.

Example :
If the device controlling D [23..20] generates error, the 15 possible codes are different of 0x00 and of those describing a single bit-in-error.

Bit in error	23	22	21	20	23 22	23 21	23 20	22 21	22 20	21 20	23 22 21	23 22 20	23 21 20	22 21 20	23 22 21 20
SY	0x68	0x4C	0x31	0x23	0x24	0x59	0x4B	0x7D	0x67	0x12	0x15	0x07	0x00	0x7A	0x36
$\overline{\text{CERR}}$	x	x	x	x	-	-	-	-	-	-	-	-	-	-	-
$\overline{\text{NCERR}}$	-	-	-	-	x	x	x	x	x	x	x	x	x	x	x

8. 8-Bit Syndrome Word

This feature is available when the N39 pin is driven at a low level.

8.1. No Error

If there is no error in the read data or checkbit, all the syndrome word is ”00”. The EDAC flags are inactive.

No Error	SY= 0x00

8.2. Single Bit-In-Error

When the Memory Data word (D [31..0] & C[7..0]) read has one bit-in-error, the 20C532E EDAC develops a code (syndrome) which indicates the bit in error (each bit have its own syndrome value). In this case, the syndrome decoder sets low the correctable error flag $\overline{\text{CERR}}$, but $\overline{\text{NCERR}}$ flag remains at high level.

In case of single bit-error on D [31..0], if the control lines $\overline{\text{SYNCHK}}$ = non active and CORRECT = active, the corrected value (CDO [31..0]) is available on DO [31..0] internal bus and the syndrome word is available on CO [7..0]. The corrected value is obtains to complement the bit-in-error.

In same conditions, if a single bit-error occurs on C [7..0], the corrected value of the checkbit is not available in the device.

Table 6: 8-bit syndrome word for single bit-error.

D[31..16]	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SY	0x6D	0x5B	0x51	0x43	0xD8	0xB4	0xB2	0x93	0x68	0xCC	0xB1	0x23	0x5D	0x64	0xD2	0xC6
D[15..0]	15	14	1x	12	11	10	9	8	7	6	5	4	3	2	1	0
SY	0x4F	0xAC	0x2A	0x9A	0xE0	0x3D	0x3B	0x2F	0xCA	0xA6	0x25	0x1F	0x16	0x54	0xC5	0xB8

C[7..0]	7	6	5	4	3	2	1	0
SY	0x80	0x40	0x20	0x10	0x08	0x04	0x02	0x01

8.3. Double Bit-In-Error

When the Memory Data word (D [31..0] & C[7..0]) read has two bit-in-error, the 20C532E EDAC develops a syndrome different of 0x00. The syndrome value generated by a double bit-in-error never takes place of a syndrome value generated by a single bit-in-error. In this case, the syndrome decoder sets low the non correctable error flag $\overline{\text{NCERR}}$ and $\overline{\text{CERR}}$ flag remains at high level.

Example:
If data D [24] and D [3] are incorrect, syndrome bit SY [7, 2, 0] are set to one (SY= 0x85), $\overline{\text{NCERR}}$ flag is set low ($\overline{\text{CERR}}$ flag remains at high level).

8.4. Triple Bit-In-Error

When the Memory Data word (D [31..0] & C[7..0]) read has three bit-in-error, the 20C532E EDAC develops a syndrome different of 0x00. The syndrome value generated by a triple bit-in-error can have any value, even a syndrome value normally generated by a single bit-in-error. $\overline{\text{NCERR}}$ flag or $\overline{\text{CERR}}$ flag can be activated following the value of the generated syndrome.

Example :
If data D [25], D [20] and D [6] are incorrect, syndrome bit SY [5, 4, 2, 1, 0] are set to one (SY= 0x37), $\overline{\text{NCERR}}$ flag is set low ($\overline{\text{CERR}}$ flag remains at high level).

Fault example: If data D [30], D [15] and D [0] are incorrect, syndrome bits SY [7, 5, 3, 2] are set to one (SY= 0xAC). The syndrome is decoded by the 29C532E EDAC has being a correctable error on D [14]. Then, $\overline{\text{CERR}}$ flag is set low and $\overline{\text{NCERR}}$ flag remains at high level. A correction would cause more errors.

8.5. Multi Bit-In-Error

When the Memory Data word (D [31..0] & C[7..0]) read has four or more bit-in-error, the 20C532E EDAC develops a non controlled syndrome. This syndrome can take any value, from 0x00 (No Error Detected) to specific syndrome value of single bit-in-error .

Example:
If the data read = 0x00000000 instead of 0xFFFFFFFF, the generated syndrome is 0x00. Then, no error flag is actived.

8.6. 4-Bit Wide Memory Error

The 8 checkbit code can be used to provide error detection for up to four errors occuring in the following fields:

- D [31..28],
- D [27..24],
- D [23..20],
- D [19..16],
- D [15..12],
- D [11..8],
- D [7..4],
- D [3..0],
- C [7..4],
- C [3..0].

The 29C532E EDAC can flag any number of errors in 4-bit wide memory chip. If the one device returns from one to four bit-in error, the $\overline{\text{CERR}}$ and $\overline{\text{NCERR}}$ flags are generated following the error type and the generated syndrome takes a value which never overlaps the code of a single bit-in-error. This is a restriction to triple and multi bit-in-error.

Example :
If the device controlling D [7..4] generates error, the 15 possible codes are different of 0x00 and of those describing a single bit-in-error.

Bit in error	7	6	5	4	7 6	7 5	7 4	6 5	6 4	5 4	7 6 5	7 6 4	7 5 4	6 5 4	7 6 5 4
SY	0xCA	0xA6	0x25	0x1F	0x6C	0xEF	0xD5	0x83	0xB9	0x3A	0x49	0x73	0xF1	0x9C	0x56
$\overline{\text{CERR}}$	x	x	x	x	-	-	-	-	-	-	-	-	-	-	-
$\overline{\text{NCERR}}$	-	-	-	-	x	x	x	x	x	x	x	x	x	x	x

8.7. 8-Bit Wide Memory Error

The 8 checkbit code can be used to provide error detection for up to eight errors occuring in the following fields:

- D [31..24],
- D [23..16],
- D [15..8],
- D [7..0],
- C [7..0].

The 29C532E EDAC can flag any number of errors in 8-bit wide memory chip. If the one device returns from one to eight bit-in error, the $\overline{\text{CERR}}$ and $\overline{\text{NCERR}}$ flags are generated following the error type and the generated syndrome takes a value which never overlaps the code of a single bit-in-error. This is a restriction to triple and multi bit-in-error.

9. Transactions

9.1. Control

The controller guides The data flow in the 29C532E EDAC. This data flow control defines the value of the output buses DO [31..0] & CO [7..0] and the checkbit bus RCB [7..0]:

- $\overline{\text{SYNCHK}}$ and CORRECT control flow on DO [31..0],
- OLE/$\overline{\text{CHK}}$ and DIAG [0] control flow on CO [7..0],
- DIAG [1] controls flow on RCB [7..0].

Table 7: Data Flow Control

	$\overline{\text{SYNCHK}}$	CORRECT	Connected to ...
DO [31..0]	High	High	CDO [31..0]
	High	Low	DI [31..0]
	Low	x	DIA [7..0] // SY [7..0] // CI [7..0] // DIA[7..0]

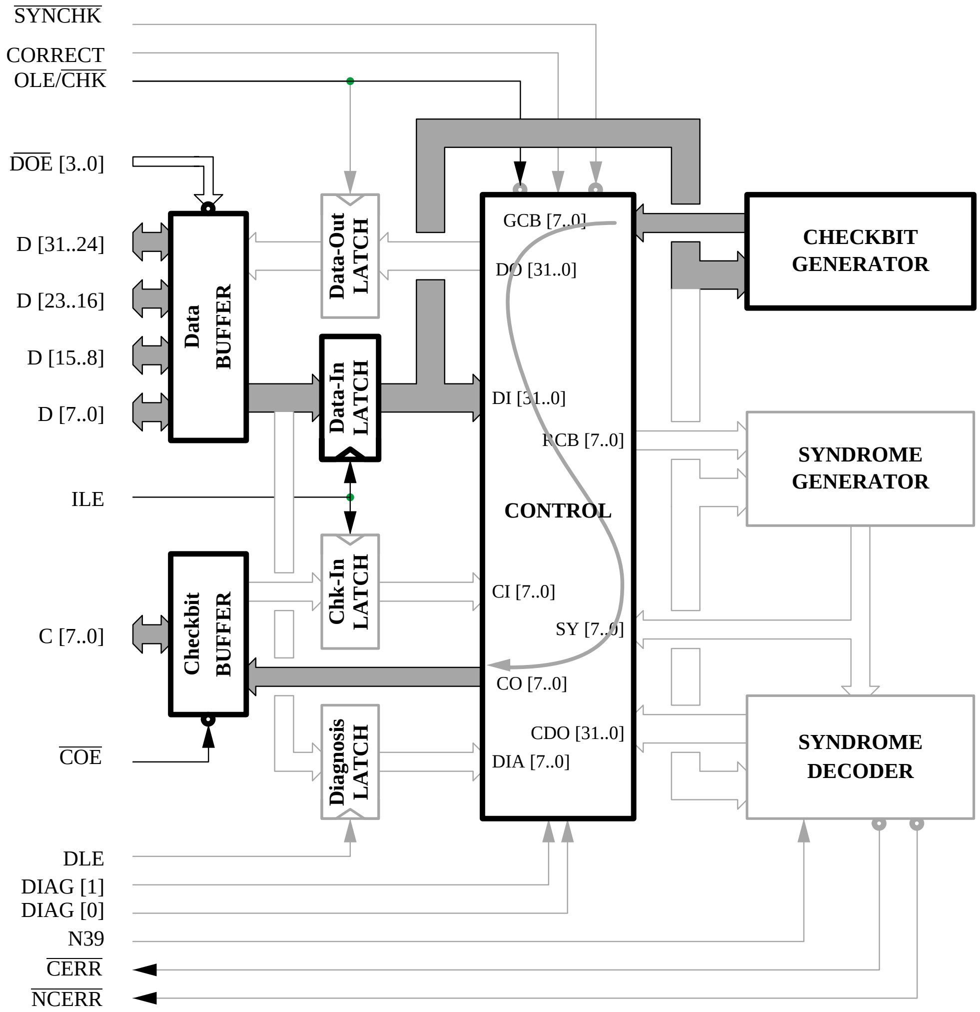
	OLE/$\overline{\text{CHK}}$	DIAG [0]	Connected to ...
CO [7..0]	Low	Low	GCB [7..0]
	High	Low	SY [7..0]
	x	High	DIA [7..0]

	DIAG [1]	Connected to ...
RCB [7..0]	Low	CI [7..0]
	High	DIA [7..0]

Eight signals are used to supervise the transactions :

- $\overline{\text{DOE}}$ [3..0] control Data Output Buffers,
- $\overline{\text{COE}}$ control Checkbit Output Buffer.
- OLE/$\overline{\text{CHK}}$ controls Data Output Latch,
- ILE controls Checkbit and Data Input Latchs,
- DLE controls Diagnostic Input Latch.

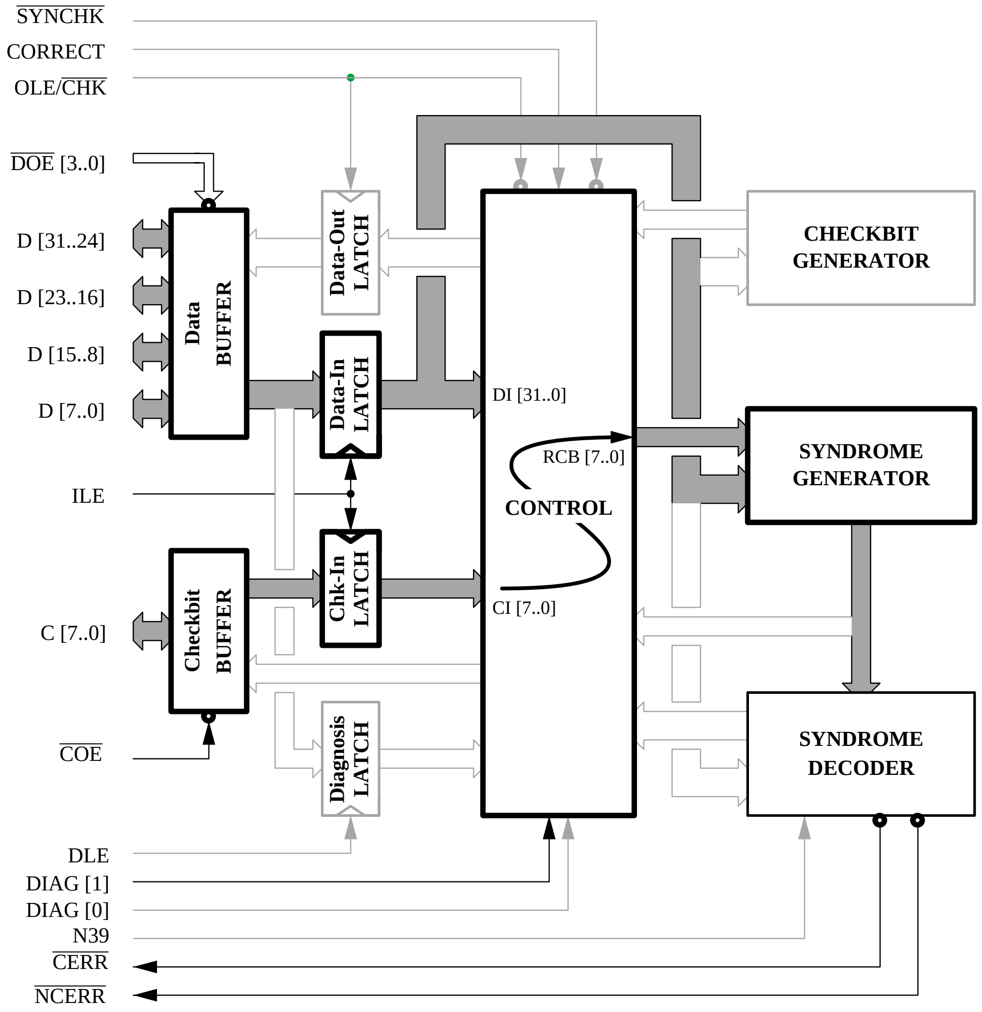
9.2. Memory Write



$\overline{\text{SYNCHK}}$	CORRECT	OLE/$\overline{\text{CHK}}$	$\overline{\text{DOE}}$ [3..]	ILE	$\overline{\text{COE}}$	DLE	DIAG [1]	DIAG [0]	N39
High	High	Low	High	H ⇒ L	Low	Low	Low	Low	H or L

9.3. Memory Read

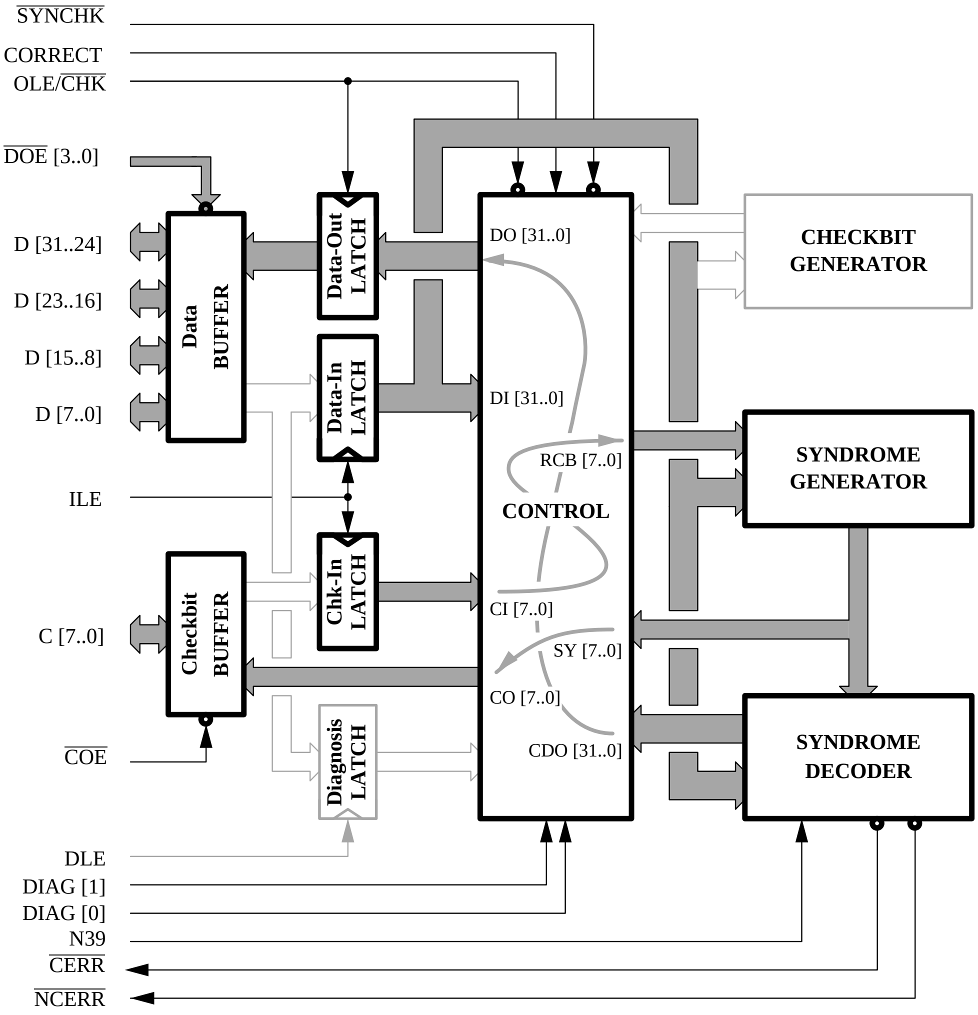
... Till Error Generation



$\overline{\text{SYNCHK}}$	CORRECT	OLE/$\overline{\text{CHK}}$	$\overline{\text{DOE}}$ [3..]	ILE	$\overline{\text{COE}}$	DLE	DIAG [1]	DIAG [0]	N39
High	High	Low	High	H ⇒ L	High	Low	Low	Low	H or L

9.4. Memory Read (continue)

... With Correction - Single Bit-in-error



$\overline{\text{SYNCHK}}$	CORRECT	OLE/$\overline{\text{CHK}}$	$\overline{\text{DOE}}$ [3..]	ILE	$\overline{\text{COE}}$	DLE	DIAG [1]	DIAG [0]	N39
High	High	L⇒M(*)	High	Low	Low	Low	Low	Low	H or L

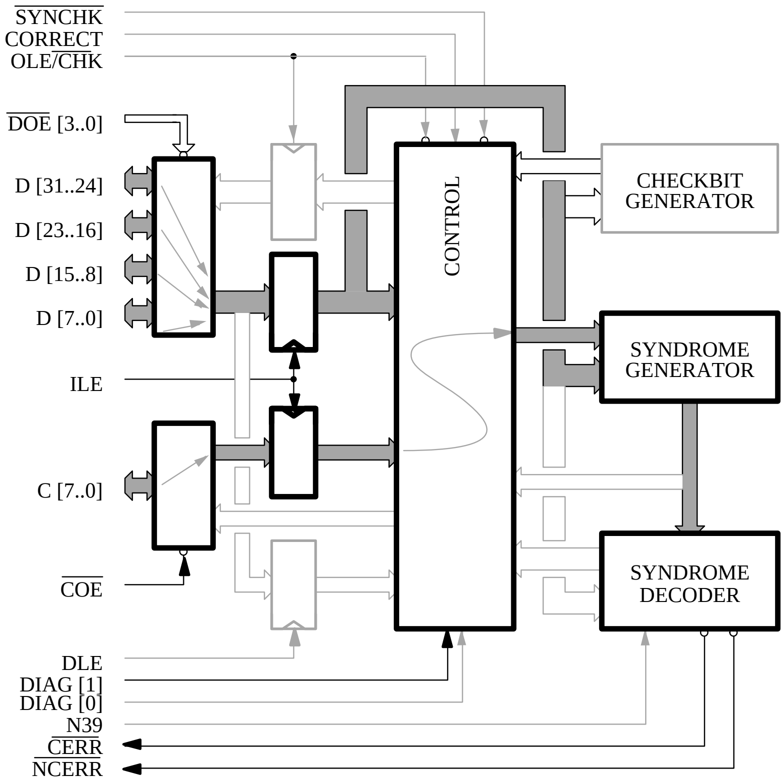
(*) when OLE/$\overline{\text{CHK}}$ = H, then CO [7..0] = SY [7..0] (placed in schematic),
when OLE/$\overline{\text{CHK}}$ = I, then CO [7..0] = GCB [7..0]

9.5. Byte Memory Write - Read Modify Write

A) 32-bit Data Memory + Checkbit Read

$\overline{\text{SYNCHK}}$	CORRECT	OLE/$\overline{\text{CHK}}$	$\overline{\text{DOE}}$				ILE	$\overline{\text{COE}}$	DLE	DIAG		N39
			[3]	[2]	[1]	[0]				[1]	[0]	
H	H	L	H	H	H	H	H↓L	H	L	[0]	[0]	X

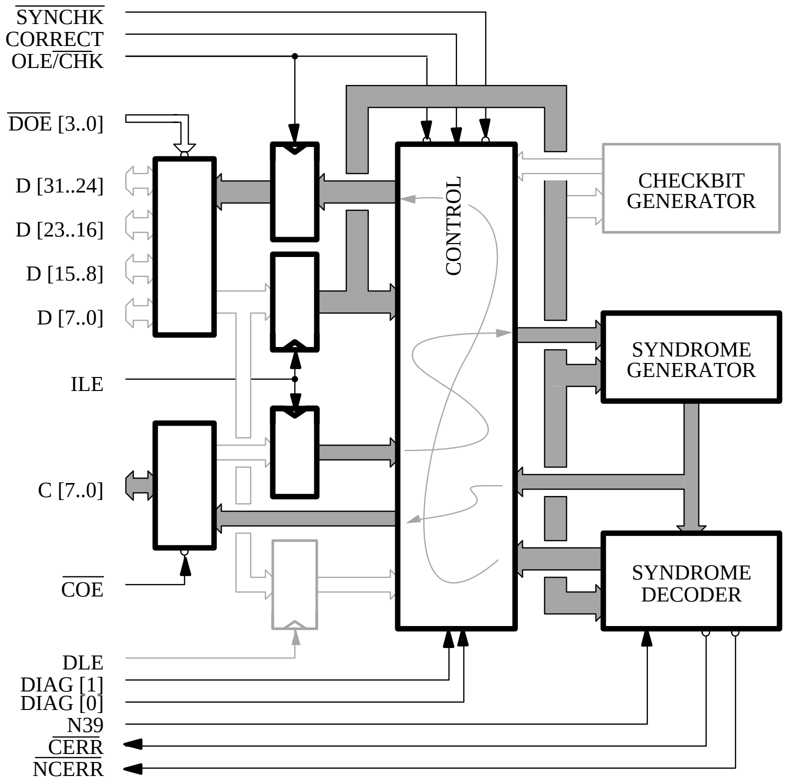
D				C
[31..24]	[23..16]	[15..8]	[7..0]	[7..0]
In	In	In	In	In



B) Preparing of 32–bit Corrected Data

$\overline{\text{SYNCHK}}$	CORRECT	OLE/$\overline{\text{CHK}}$	$\overline{\text{DOE}}$				ILE	$\overline{\text{COE}}$	DLE	DIAG		N39
			[3]	[2]	[1]	[0]				[1]	[0]	
H	H	L↗H	H	H	H	H	L	H	L	[0]	[0]	X

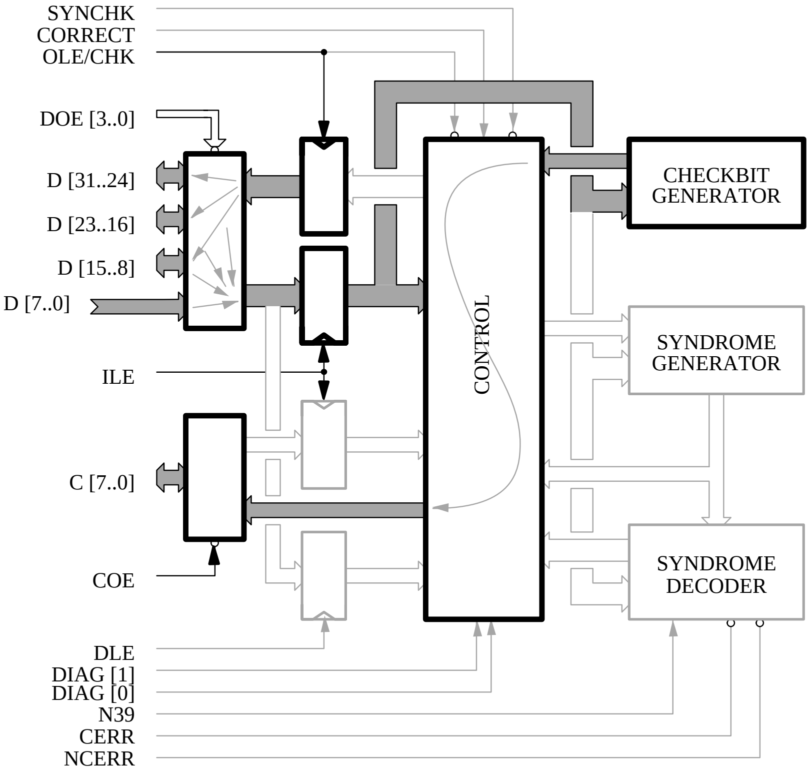
D				C
[31..24]	[23..16]	[15..8]	[7..0]	[7..0]
In	In	In	In	In



C) 8-bit Data Memory + Checkbit Write

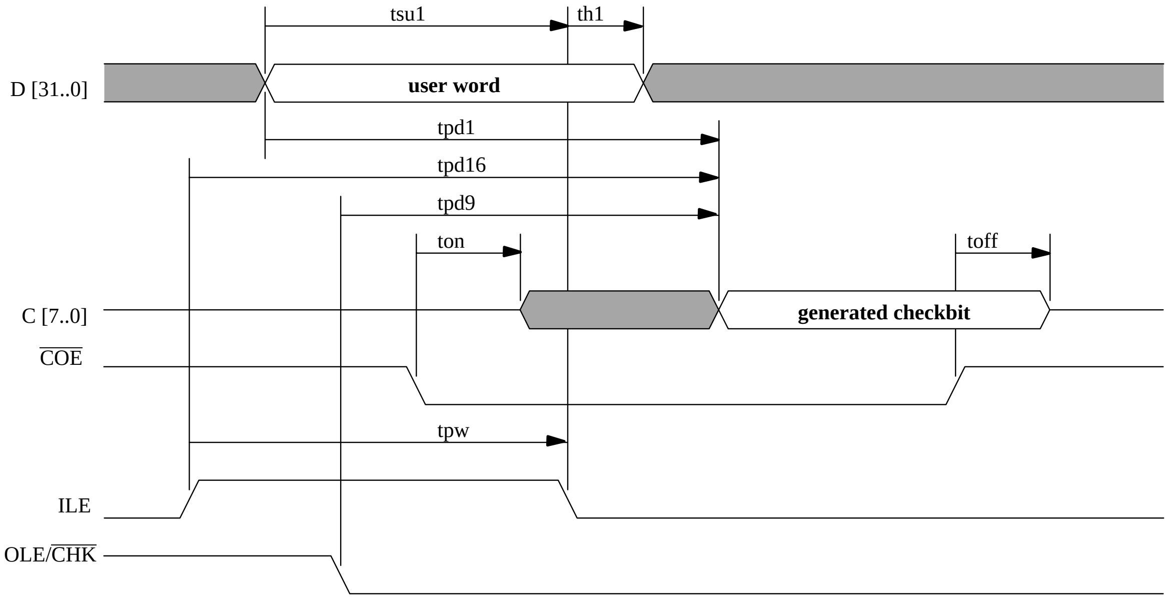
$\overline{\text{SYNCHK}}$	CORRECT	OLE/$\overline{\text{CHK}}$	$\overline{\text{DOE}}$				ILE	$\overline{\text{COE}}$	DLE	DIAG		N39
			[3]	[2]	[1]	[0]				[1]	[0]	
H	H	H↘L	L	L	L	H	H↘L	L	L	[0]	[0]	X

D				C
[31..24]	[23..16]	[15..8]	[7..0]	[7..0]
In-Out	In-Out	In-Out	In	Out



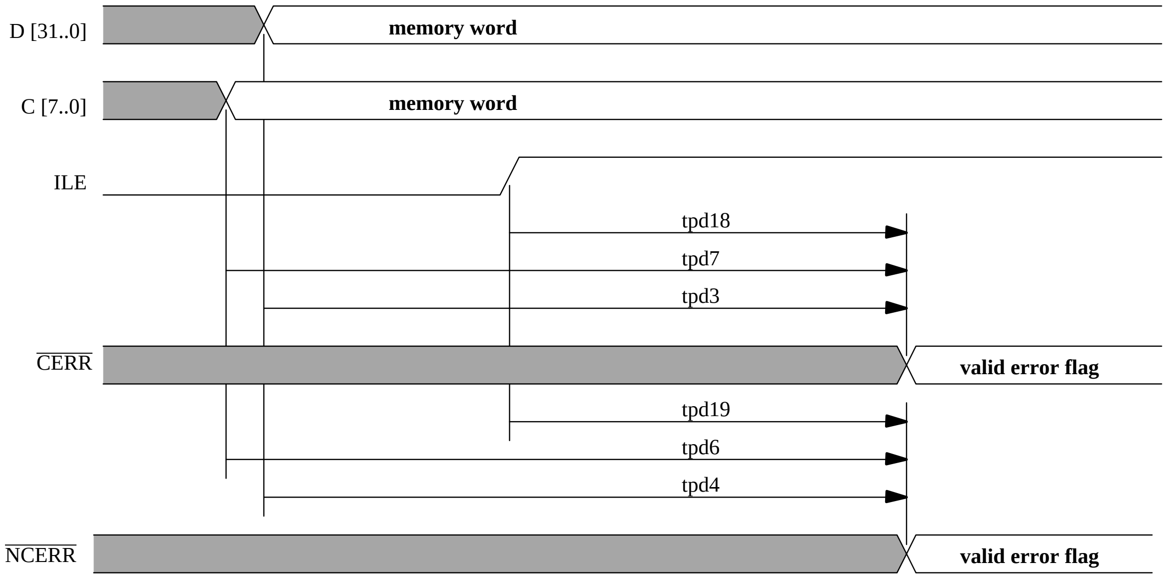
10. Signal Timing

10.1. Memory Write



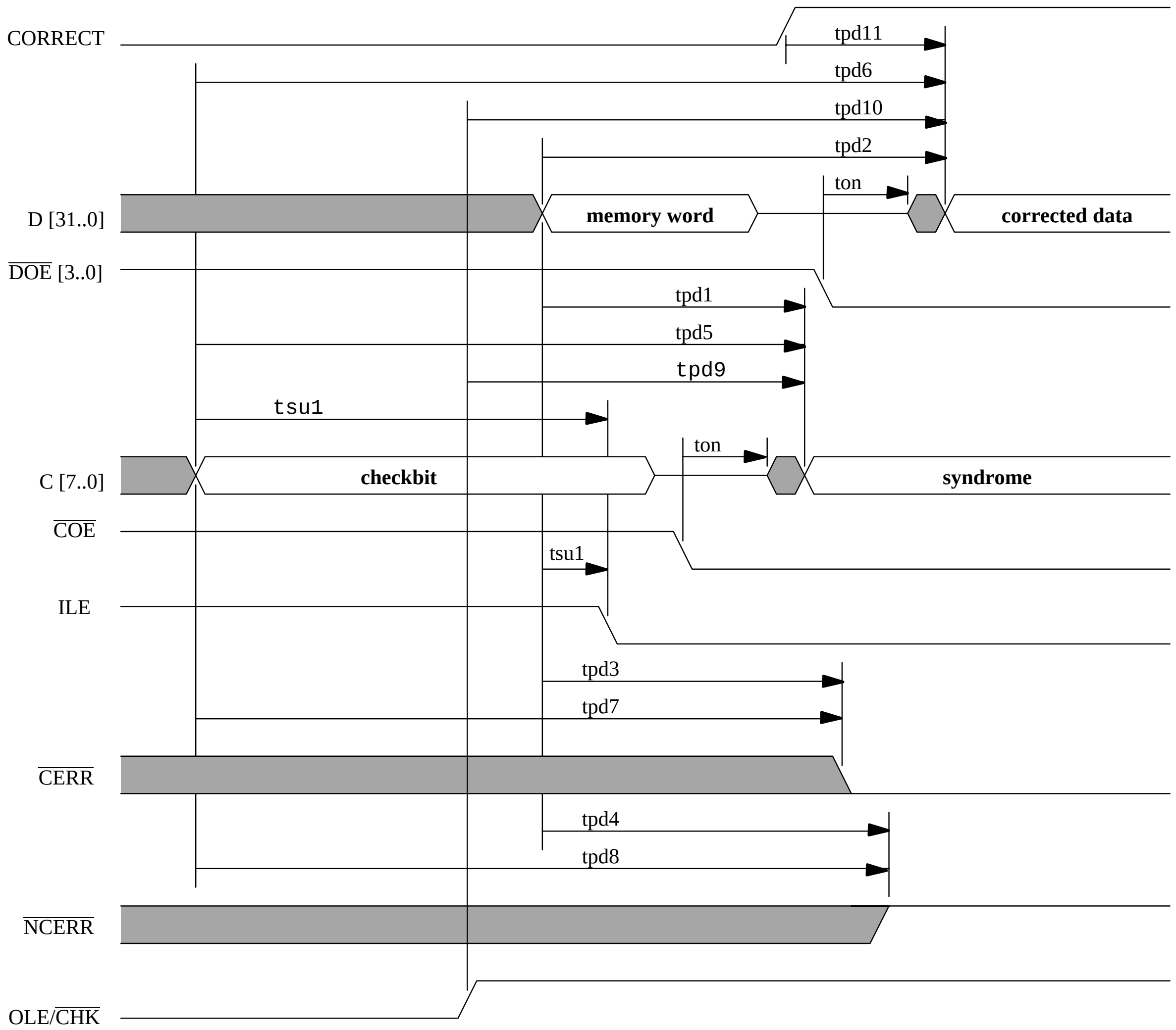
	tsu 1	th 1	tpd 1	tpd 16	tpd 9	ton	toff	tpw
Max (ns)			30	38	20	14	14	
min (ns)	6	5						5

10.2. Memory Read



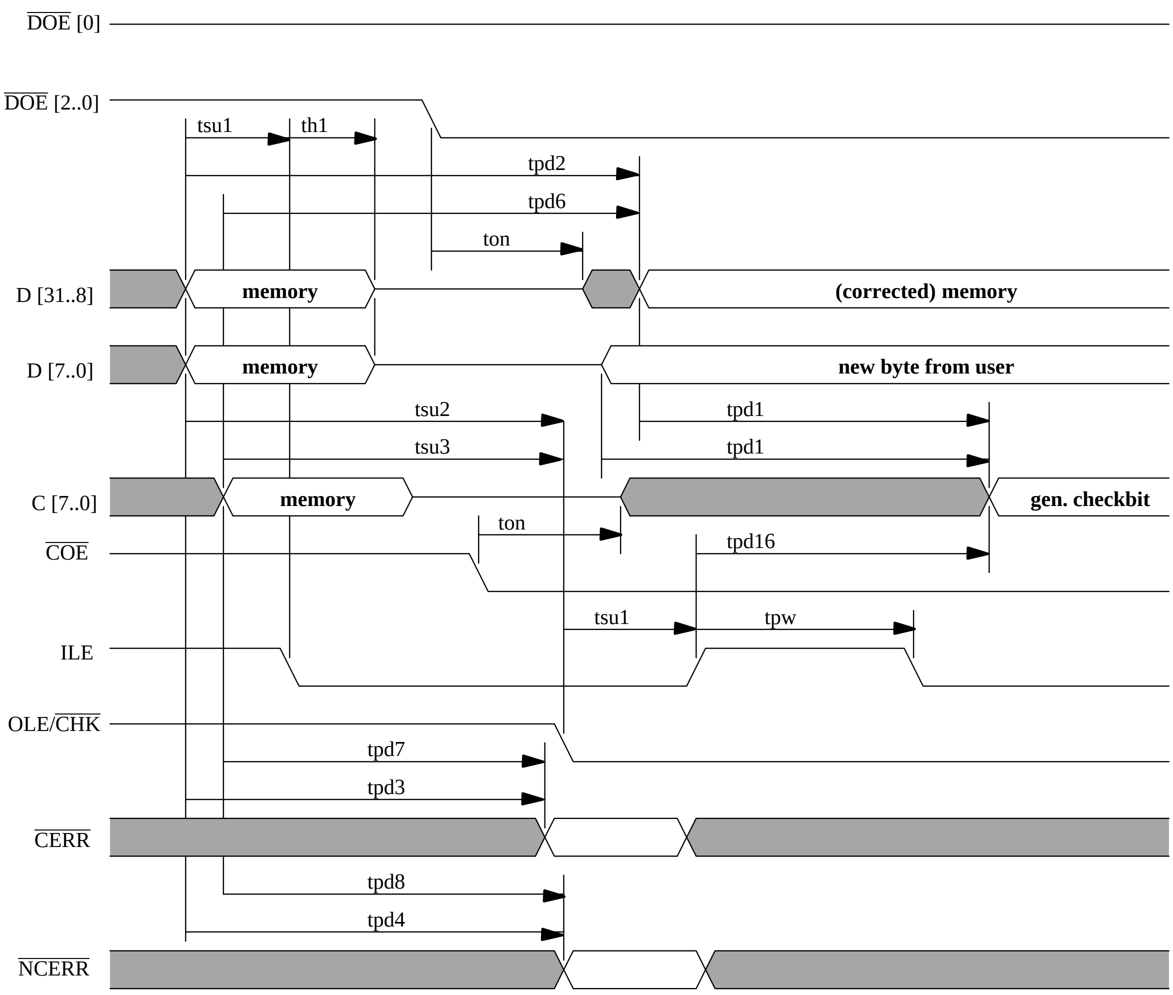
	tpd 18	tpd 7	tpd 3	tpd 19	tpd 8	tpd 4
Max (ns)	41	32	34	45	35	37
min (ns)						

10.3. Memory Read With Correction



	tpd 11	tpd 6	tpd 10	tpd 2	ton	tpd 1	tpd 5	tpd 9	tsu 1	tpd 3	tpd 7	tpd 4	tpd 8
Max (ns)	20	38	18	39	14	30	29	20		34	32	37	35
min (ns)									6				

10.4. Memory Byte Write (Read Modify Write)



	tsu 1	th 1	tpd 2	tpd 6	ton	tsu 2	tsu 3
Max (ns)			39	38	14		
min (ns)	6	5				34	32

	tpd 1	tpd 16	tpw	tpd 7	tpd 3	tpd 8	tpd 4
Max (ns)	30	38		32	34	35	37
min (ns)			5				