PM5351

S/UNI-® 155-TETRA

S/UNI-TETRA

SATURN USER NETWORK INTERFACE (155-TETRA)

ERRATA

ISSUE 8: JUNE 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
8	June 2000	This document contains errata information corresponding to the issue 7 datasheet and device revision G. Corrected datasheet document errors in Register 0x91. Added a section on interfacing the S/UNI-TETRA to ODLs with internal termination. Added a section stating that the S/UNI-TETRA needs to reset their receive FIFO when a receive FIFO overrun occurs.
7	November 1999	This document contains errata information corresponding to the issue 5 datasheet and device revision G.
6	July 1999	This document contains errata information corresponding to the issue 5 datasheet and device revision E.
5	June 1999	This document contains errata information corresponding to the issue 5 datasheet and device revision E.
4	May 1999	This document contains errata information corresponding to the issue 5 datasheet and device revision E.
3	Feb 1999	This document contains errata information corresponding to the issue 5 datasheet and device revision C.
2	Jan 1999	This document contains errata information corresponding to the issue 5 datasheet and device revision C.
1	Nov 1998	This document contains errata information corresponding to the issue 4 datasheet and device revision C.

CONTENTS

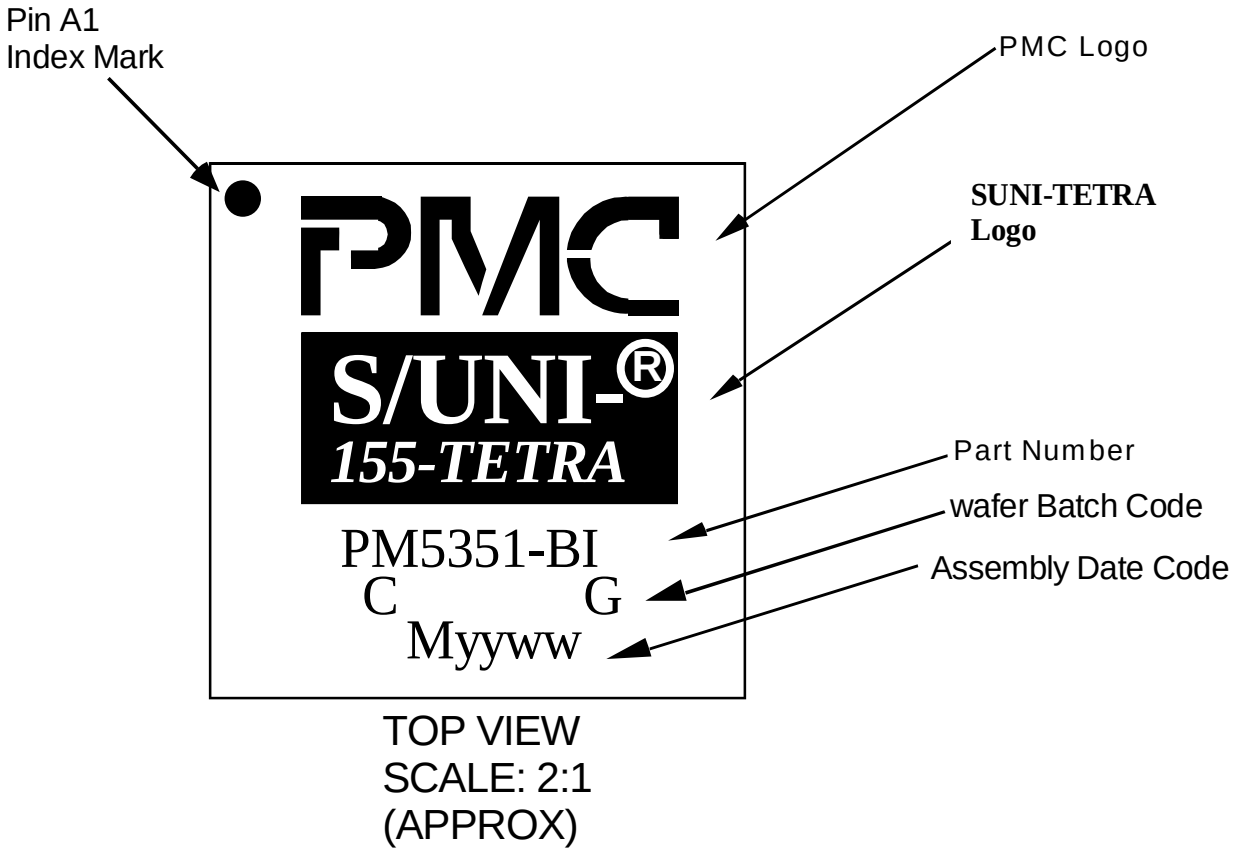
1 ISSUE 8 ERRATA

This issue 8 contains errata applied to the PMC-971240 S/UNI-TETRA Issue 7 datasheet. The issue 7 datasheet and issue 8 errata supersede all prior editions and versions

1.1 Device Identification

The information contains in this document applies to the PM5351 S/UNI-TETRA revision G device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). The PM5351 S/UNI-TETRA revision G is packaged in a 304 pin Super BGA package.

Figure 1: PM5351 S/UNI-TETRA Branding Format



2 S/UNI-TETRA DATASHEET DISCREPANCIES

Legend

1. unaltered text is unchanged to add context to changes

2. new material is bold and Italicized

~~3. obsolete material is struck out~~

4. comments specific to this document are in italics

5. A vertical bar in left margin indicates that this is a new item which was not present in the previous issue of this document.

2.1 Page 225: S/UNI-TETRA Channel Auto Path RDI Control Register Discrepancies

Register 0x91: S/UNI-TETRA Channel Auto Path RDI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDPRDI	0
Bit 6	R/W	ALRMPRDI	0
Bit 5	R/W	PAISPRDI	1
Bit 4	R/W	PSLMPRDI	1
Bit 3	R/W	LOPPRDI	1
Bit 2	R/W	LOPCONPRDI	1
Bit 1	R/W	PTIUPRDI	1
Bit 0	R/W	PTIMPRDI	1

This register controls the auto assertion of path RDI (G1 bit 5) in the local TPOP. Since the S/UNI-TETRA provides STS-3c (STM-1/AU4) mappings, this register controls the assertion of path RDI for the entire SONET/SDH stream. See also the S/UNI-TETRA Channel Auto Enhanced Path RDI register.

RTIMPRDI:

The Receive Trace Identifier Mismatch PRDI (RTIMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When RTIMPRDI is set to logic one, the transmit ~~line~~ ***path*** RDI will be inserted. When RTIMPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

PTIUPRDI:

The Path Trace Identifier Unstable PRDI (PTIUPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PTIUPRDI is set to logic one, the transmit ~~line~~ ***path*** RDI will be inserted. When PTIUPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

LOPCONPRDI:

The Loss of Pointer Concatenation Indication PRDI (LOPCONPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When LOPCONPRDI is set to logic one, the transmit ~~line~~ ***path*** RDI will be inserted. When LOPCONPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

LOPPRDI:

The Loss of Pointer PRDI (LOPPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When LOPPRDI is set to logic one, the transmit ~~line~~ ***path*** RDI will be inserted. When LOPPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

PSLMPRDI:

The Path Signal Label Mismatch PRDI (PSLMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PSLMPRDI is set to logic one, the transmit ~~line~~ ***path*** RDI will be inserted. When PSLMPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

PAISPRDI:

The Path Alarm Indication Signal PRDI (PAISPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PAISPRDI is set to logic one, the transmit ~~line~~ ***path*** RDI will be inserted. When PAISPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

ALRMPRDI:

The Line Alarm Indication Signal PRDI (ALRMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of one of the following alarm conditions: Loss of Signal (LOS), Loss of Frame (LOF) and Line Alarm Indication Signal (LAIS). When ALRMPRDI is set to logic one, the transmit ~~line~~ ***path*** RDI will be inserted. When ALRMPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

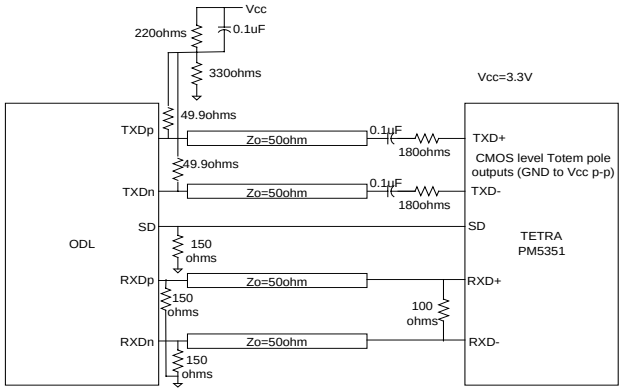
LCDPRDI

The Loss of ATM Cell Delineation Signal PRDI (LCDPRDI) controls the insertion of Path RDI in the transmit data stream upon detection of this alarm. When LCDPRDI is set to logic one, the transmit ~~line~~ ***path*** RDI will be inserted. When LCDPRDI is set to logic zero, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set to logic one.

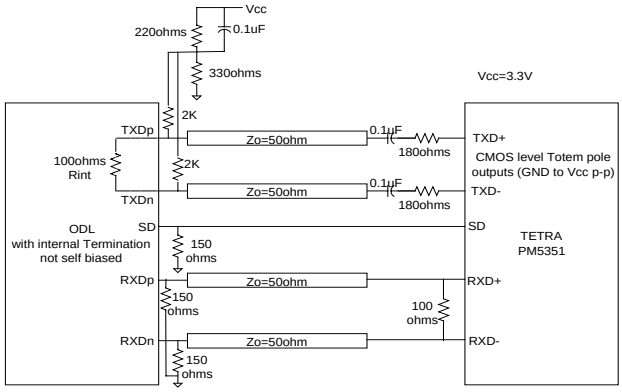
2.2 Interfacing S/UNI-TETRA To ODLs With Internal Termination

ODL to TETRA PECL INTERFACE

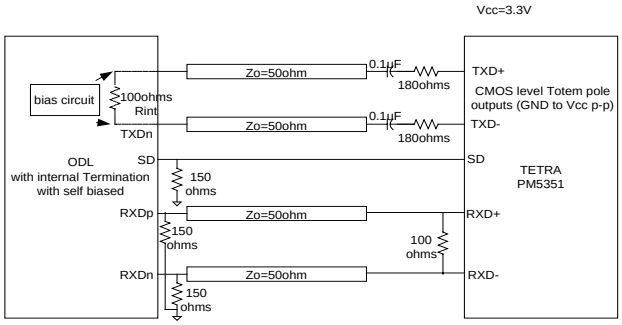
ODL without Internal Termination



ODL with 100Ohms Internal Termination not self biased



ODL with 100Ohms Internal self biased Termination



3 S/UNI-TETRA FUNCTIONAL DISCREPANCIES

3.1 Receive FIFO Overrun Requires Reset When Operating In Packet Over SONET (POS) Mode

In packet over sonet (POS) mode, the S/UNI-TETRA requires that the receive FIFO to be reset after a receive FIFO overrun occurs. The receive FIFO can be reset by setting bit 0 of Register 0x62 to logic 1 and back to logic 0.

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