PM5342

SPECTRA-155

ANSWERS TO FREQUENTLY-ASKED QUESTIONS REGARDING THE SPECTRA-155

APPLICATION NOTE

ISSUE 2: JULY 2000

REVISION HISTORY

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2	July 2000	Material updated.
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CONTENTS

1 BACKGROUND

PMC-Sierra's PM5342 SONET/SDH Payload Extractor/Aligner (SPECTRA-155) terminates the transport and path overhead of STS-1 (STM-0/AU-3) and STS-3/3c (STM-1/AU-3/AU-4) streams.

Due to the versatility of the SPECTRA-155, its data book (PMC-970133) is quite lengthy. In order to help customers quickly find the answers to their questions, the following list of answers to frequently-asked questions has been compiled. If further clarification is required, please contact PMC-Sierra's technical support team via the PMC-Sierra website (http://www.pmc-sierra.com) or at apps@pmc-sierra.com.

2 GENERAL QUESTIONS

Q1) Are there any reference designs available for the SPECTRA-155?

A1) Yes. The SNOW Board Reference Design (PMC-970285) shows a basic implementation of the SPECTRA-155 with optics and a CPU. A ring expansion connector allows two SNOW boards to be connected back-to-back for ring applications. A second connector provides access to the system-side interface. Reference design documentation includes design descriptions, schematics, and PCB plots.

The SPECTRA-155 POS Reference Design (PMC-971113) shows the implementation of a packet-over-SONET transmission system using the SNOW Board Reference Design and a daughtercard containing an FPGA-based HDLC controller.

Another useful document is the SARD Reference Design (PMC-951036) which shows an add/drop mux (ADM) node consisting of STXC, SPTX, TUPP-PLUS, and TUDX devices. Although this reference design does not contain a SPECTRA-155, the system-side interface of the SPTX is almost identical to that of the SPECTRA. The front-end of this design (CRU, STXC) can be ignored because the front-end components have been integrated within the SPECTRA.

All documents are available from your PMC-Sierra sales representative or from the PMC-Sierra website (http://www.pmc-sierra.com).

Q2) Are there any application notes available for the SPECTRA-155?

A2) Yes. Several application notes relate to the SPECTRA-155. In the following list, the first two application notes relate directly to the SPECTRA-155 and are useful for all SPECTRA-155 designs. The remaining notes provide background information on various topics but are not specific to the SPECTRA.

- *Suggestions for SPECTRA-155 PECL Terminations* (PMC-970938)
- *SPECTRA-155 Programmer's Reference* (PMC-980901)
- *SONET/SDH Bit Error Threshold Monitoring* (PMC-950820)
- *Technique for Measuring Jitter Tolerance, Jitter Transfer, and Intrinsic Jitter* (PMC-951002)
- *Handling of Moisture Sensitive Plastic IC Packages* (PMC-951041)

- *Network Survivability Using Automatic Protection Switching (APS) over SONET/SDH Point-to-Point & Ring Networks* (PMC-960505)

- *LAN and WAN Timing Considerations for PMC-Sierra ATM PHY Devices* (PMC-960629)

- *Surface Mount Assembly of PBGA/TEGBA Packages* (PMC-970951). This document describes a TEBGA package which is the same as the SBGA package used for the SPECTRA-155.

All documents are available from your PMC-Sierra sales representative or from the PMC-Sierra website (http://www.pmc-sierra.com).

Q3) Are there other PMC-Sierra chips designed to work with the SPECTRA-155?

A3) Yes. The following list gives PMC-Sierra devices commonly interfaced to the SPECTRA-155:

- PM5312 STTX. SPECTRA-155's Add bus pointer interpreter allows the STTX and four SPECTRA-155s to be connected "back-to-back" to create a compact OC-12 to OC-3 multiplexer.

- PM5344 SPTX. SPECTRA-155 has a standard Telecom bus interface that will interface directly to the SPTX.

- PM5362 TUPP-PLUS. This device interfaces to the SPECTRA-155's Drop Telecom bus (or to the Add Telecom bus in some applications) to provide tributary pointer processing and tributary overhead monitoring.

- PM5371 TUDX. In conjunction with the TUPP or TUPP-PLUS, the TUDX will perform tributary-level cross connects on the Telecom bus.

- PM8315 TEMUX. The TEMUX will connect directly to the SPECTRA-155's Telecom bus to provide tributary mapping into SONET/SDH payloads. The TEMUX will also connect directly to the DS3 mapper in SPECTRA-155 to mux/demux DS1s or DS2s from DS3 tributaries

- PM7345 S/UNI-PDH. The S/UNI-PDH will connect directly to the SPECTRA-155's DS3 mapper to provide ATM in a DS3 tributary.

- PM7346 S/UNI-QJET. Connects to the SPECTRA-155's DS3 mapper to provide ATM in a DS3 tributary, or to frame DS3 tributaries.

- PM7364/PM7366 FREEDM-8 and FREEDM-32. These devices will connect to the SPECTRA-155's DS3 mapper via a PM7346 S/UNI-QJET to provide

HDLC over DS3. In addition, the FREEDM devices interface directly to the SPECTRA-155's section- and line-DCC ports.

- PM8313 D3MX. The D3MX will connect directly to the SPECTRA-155's DS3 mapper to demultiplex the DS3 tributaries down to DS1 or DS2.

Q4) Are there models (Verilog, VHDL, Bus Functional, IBIS) available for the SPECTRA-155?

A4) An IBIS model of SPECTRA-155 input and output pin behaviour is available from PMC-Sierra. See the PMC-Sierra web site to register (http://www.pmc-sierra.com) or contact your PMC-Sierra sales representative.

At the time of issuance of this document, there are no other models available for the SPECTRA-155.

3 LINE-SIDE INTERFACE QUESTIONS

Q5) What Optical Interface Modules are recommended for use with the SPECTRA-155?

A5) PMC-Sierra does not recommend specific optical modules for use with the SPECTRA-155. In general, any optical interface module that has a PECL system-side interface, with or without clock recovery, should be suitable.

During lab testing of the SPECTRA-155 we have had success with several optical interface modules. The following list of devices is for informational purposes only and is not an exhaustive list of suitable devices:

- Hewlett-Packard: HFBR5205, SDX1155B
- Sumitomo: SDM7201-XC

Q6) What Electrical Interface Modules are recommended for use with the SPECTRA-155?

A6) PMC-Sierra does not recommend specific electrical modules for use with the SPECTRA-155.

At the STS-1/STM-0 data rate, a 51.84Mb/s electrical line interface with a CMOS or PECL system-side interface, with or without clock recovery, should be suitable. These devices are often sold as T3 line interfaces, with the capability of also terminating STS-1. Generally, some level translation will be required to interface to the SPECTRA-155.

At the STS-3/STM-1 data rate, a 51.84Mb/s electrical line interface with a PECL system-side interface is required. Because the SPECTRA-155 does not provide a 155Mb/s transmit clock, the line interface must be capable of transmit clock recovery.

Q7) PMC's recommended PECL interface is different than the one recommended by my optical transceiver manufacturer. Which should I use?

A7) SPECTRA-155's PECL interface is not true PECL. In the transmit direction, outputs are CMOS levels (0-5V swing) and must be attenuated and shifted to PECL levels (nominally 750mV centered at 3.68V). In the receive direction, inputs are a form of comparator which must, in most cases, be AC-coupled to find the correct bias voltage.

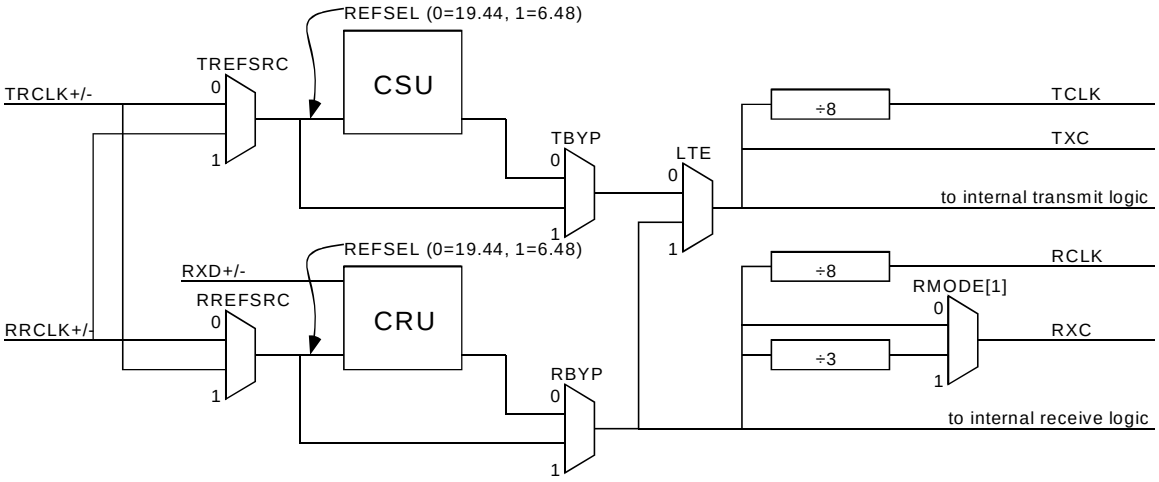
If the optics have a true PECL interface, then our recommended interface configurations will work. Refer to the application note, *Suggestions for SPECTRA-155 PECL Terminations* (PMC-970938), for more details. This document is available from your PMC-Sierra sales representative or from the PMC-Sierra website (http://www.pmc-sierra.com).

Other interface configurations are also possible. Contact PMC-Sierra's technical support team at apps@pmc-sierra.com to discuss any non-standard optical interface configurations.

Q8) How do the SPECTRA-155's line side clock inputs and outputs relate?

A8) Figure 1 shows the clock flow on the SPECTRA-155 line side interface.

Figure 1 - SPECTRA-155 Line-Side Clocking



4 SYSTEM-SIDE INTERFACE QUESTIONS

4.1 Overhead and Alarm Interfaces

Q9) The SPECTRA-155 has a lot of pins dedicated to inserting and extracting different types of overhead and alarms. What should I do with them?

A9) In most applications, it is not necessary to use any of the overhead insertion or extraction interfaces. All common overhead functions are handled automatically, or require only software intervention. A summary of the various overhead ports follows. Not shown in the list are the clocks and framing pulses associated with each overhead port. Unless otherwise noted, all unused inputs must be tied to GND, and unused outputs may be left unconnected.

- RTOH, TTOH. These ports provide access to the entire transport overhead. Normally, you'll only need to use these if you have a non-standard application like test equipment.

- RPOH[3:1], TPOH[3:1]. These ports provide access to the entire path overhead. Normally, you'll only need to use these if you have a non-standard application like test equipment.

- RSLD, RLD, RSUC, RSOW, RLOW, TSLD, TLD, TSUC, TSOW, TLOW. These can be ignored unless you specifically need to terminate section/line DCC, section user channel, or section/line orderwire. Unused inputs may be tied to GND or VCC, depending on what steady-state value should appear in the associated overhead byte.

- RTCOH[3:1]. These ports provide access to the Tandem Connection data link and may be ignored if you are not using Tandem Connection.

- Ring Control Port (RRCPDAT, TRCPDAT). The Ring Control Ports exchange protection switch, error, and alarm information between two SPECTRA-155s in an ADM ring node. Other applications need not use this port.

- Alarm Port (RAD, TAD). The Alarm Ports provide a mechanism for communicating alarm information with external hardware. Normally, you will only need to use these ports if there are special requirements for monitoring or transmitting alarms.

4.2 Telecom Bus Interface

Q10) Where can I find the Telecom Bus standard?

A10) The Telecom bus was originally going to be defined in IEEE P1396, but the Telecom bus standards group was disbanded without ever producing a formal specification. Although no formal standard exists, PMC-Sierra products and related third party devices (mappers, for example) have similar bus implementations that trace to the P1396 standardization efforts.

Designers using the SPECTRA-155 should review the Telecom Bus interfaces of other components to verify compatibility.

Q11) What is the data delay through the SPECTRA-155?

A11) Table 1 gives the minimum and maximum round-trip payload delay through the SPECTRA-155 at STS-1 (STM-0) and STS-3 (STM-1) data rates.

Table 1 - SPECTRA-155 Round-Trip Payload Delay

Rate	Delay (µs)		
	Minimum	Nominal	Maximum
STS-1 (STM-0)	7.7	9.0	10.2
STS-3c (STM-1/AU-4)	4.0	5.2	6.5

Notes:

- Nominal delay values assume no pointer justifications. Frequency offsets will increase or decrease the average delay value, depending on the direction of the offset.
- Delays for STS-3 (STM-1/AU-3) and STS-3c (STM-1/AU-4) are roughly equivalent.
- The delays given are for byte Telecom bus mode. Other Telecom bus modes and the Datacom bus modes will vary slightly. DS-3 mappers will add to the round-trip data delay.
- The delays given in Table 1 are based on simulation results. Measured delays may vary considerably depending on measurement technique and the test equipment used.

Q12) Does PMC-Sierra recommend a T1 (or E1, or T3, or …) mapper for use with the SPECTRA-155?

A12) PMC-Sierra does not recommend specific mappers for use with the SPECTRA-155. Because the Telecom bus is a defacto industry standard, most third party mappers will interface to the SPECTRA with little or no glue logic. Contact PMC-Sierra's technical support team at apps@pmc-sierra.com to discuss interface requirements for specific mappers.

Q13) What, exactly, is indicated by the V1 pulse in the C1J1V1 signal on the Telecom Bus?

A13) The V1 pulse indicates the position of the V1 byte of the first tributary in an STS-1 (STM-0/AU-3) or STS-3 (STM-1/AU-3) multiframe. In other words, the V1 pulse will, with one exception, follow the J1 pulse in every fourth transport frame. The exception comes when the J1 pulse falls at the end of a row; in this case, the V1 pulse will appear in the next SPE byte following the transport overhead. There is only one V1 pulse per multiframe—V1 does not indicate the position of the remaining tributaries.

During STM-1/AU-4 operation, the V1 pulse position will continue to indicate the position of an AU-3 V1, even though the AU-4/TUG-3 mapping actually places the first V1 position in a different column.

Q14) How should I generate the 6.48 or 19.44MHz clock to feed to the SPECTRA-155's DCK or ACK pins?

A14) In order for the SPECTRA-155 to operate correctly, the ACK and DCK clocks must be within about 300ppm of the transmit and receive clock frequencies, respectively. For example, a 19.44MHz (20ppm) crystal oscillator would suffice for STS-3/STM-1 operation. Although the ACK and DCK timing domains are independent of each other and of the line-side clocks, it is often convenient to drive both ACK and DCK from the same source so that the entire system-side interface is synchronous.

If new SPE timing is being generated on the Add bus, then the ACK source must meet stratum-traceable accuracy and stability requirements. In this case, a crystal oscillator is not sufficient and a system-level timing circuit must be used.

Q15) Will transport overhead pass through on the SPECTRA-155's Add and Drop buses?

A15) No. All transport overhead (section and line, or regenerator section and multiplex section) will be overwritten in both the Add and Drop directions. On the Drop bus all transport overhead, except for the H1 H2 pointer, will be 00h. The H1 H2 pointer contains a new pointer value that reflects the Drop-side AU/SPE

alignment. In the Add direction, all transport overhead is overwritten by the SPECTRA-155.

SPECTRA-155 may be configured to pass path overhead and payload transparently.

Q16) Do I need to provide the J1 pulses on AC1J1V1?

A16) SPECTRA-155 uses the J1 pulse on AC1J1V1 to identify the start of the payload on the Add bus. However, SPECTRA-155 can also interpret H1, H2 pointers to locate the payload. If the application provides valid H1, H2 pointers on the Add bus, then the J1 pulse need not be provided. The DISJ1V1 bit in register 100h should be set high to configure SPECTRA not to expect J1 (or V1) pulses on AC1J1V1, and to enable the Add bus pointer interpreter.

Q17) How does SPECTRA-155 handle multiframe alignment?

A17) In the Transmit direction, SPECTRA-155 uses the V1 pulse on AC1J1V1 to identify the tributary multiframe alignment on the Add bus. The multiframe alignment dictated by the V1 pulse is passed through to the Transmit stream. It is not necessary to provide the V1 pulse, though. In some applications, the system-side device may not generate a V1 pulse, or SPECTRA-155 may be programmed to ignore J1 and V1 pulses (DISJ1V1 bit in register 100h). In such cases, there are two possible ways to treat the multiframe alignment.

If the H4BYP bit is set high in register 140h, the H4 byte on the Add bus will be passed through unchanged. If H4BYP is set low, and there is no V1 pulse on AC1J1V1, SPECTRA-155 will generate an arbitrary multiframe alignment on the Transmit stream.

In the receive direction, SPECTRA-155 interprets the H4 byte in the received data stream. If the H4BYP bit in register 128h is set low, SPECTRA-155 regenerates the H4 byte on the Drop bus based on the multiframe alignment in the receive stream. If H4BYP is set high, the H4 byte is passed through unchanged from the receive stream to the Drop bus.

Q18) What is the SPECTRA-155's Generated bus for?

A18) The Generated bus simplifies the interface between SPECTRA-155 and other Telecom bus devices by providing frame timing signals (GC1J1V1, GPL) which would otherwise be generated in glue logic. Although it is useful in many applications, the Generated bus is not required for any mode of operation.

With the exception that the Generated bus outputs are clocked by ACK, the Generated bus is completely independent of the Add and Drop busses. The Generated bus creates timing signals for a SDH/SONET frame with arbitrary

frame and multiframe alignment (controlled by GFP and GMFP), and with arbitrary AU/SPE alignment and pointer justifications (controlled with register settings).

4.3 DS3 Interface

Q19) I would like to use the built-in DS3 mapper on the SPECTRA-155 to interface directly to a DS3 line. What external circuitry do I need?

A19) In many applications, no external circuitry is required to use the SPECTRA-155's DS3 mapper. For example, both the PM8313 D3MX and the PM7345 S/UNI-PDH may be connected directly to the DS-3 mapper without any additional circuitry.

In applications where the DS3 mapper is driving a line through a DS3 LIU, external circuitry is required to interface to the LIU. For these applications, the DS3 mapper should be connected to a DS3 LIU as follows:

- In the optical transmit (Add) direction, the SPECTRA-155 may interface directly to a DS3 LIU.
- In the optical receive (Drop) direction, gaps in the DS3ROCLK signal must be smoothed. De-gapping can be achieved with a PLL to smooth the clock and a small FIFO to smooth the data. The smoothed clock and data may be connected directly to the DS3 LIU.

In applications where the transmitted DS3 signal must meet jitter template specifications, the SPECTRA-155's internal DS3 mapper is not recommended. While the de-gapping circuitry described above is able to smooth out gaps in DS3ROCLK, it is unable to fully attenuate jitter due to SONET/SDH pointer justifications.

Note that the DS3 demapping jitter is only of concern when a SPECTRA-155 is directly connected to a DS3 line. If the demapped DS3 feeds immediately into a datacom device like the PM7345 S/UNI-PDH, jitter is irrelevant. If the demapped DS3 is immediately demultiplexed into lower-rate streams (using the PM8313 D3MX, for example), any jitter will be attenuated below the template of the lower-rate streams.

Q20) Is it possible to use the SPECTRA-155's internal DS3 mapper and the Telecom Bus at the same time?

A20) No. Use an external DS3 mapper if you also require access to the SPECTRA-155's Telecom bus.

Q21) When should I use the SPECTRA-155's external DS3RICLK pin instead of the internal 51.84MHz clock?

A21) You should use the external DS3RICLK in two occasions: when the downstream equipment cannot handle an instantaneous clock rate of 51.84MHz (such as the PM8313 D3MX), and when the DS3 is being de-gapped and transmitted out a DS3 line interface. In the latter case, using the 44.928MHz DS3RICLK will result in a DS3ROCLK gapping pattern with much less spectral noise. This "clean" DS3ROCLK will be easier to de-jitter.

5 BOARD LAYOUT AND POWER SUPPLY QUESTIONS

Q22) What are the suggestions for power supply bypassing for the SPECTRA-155?

A22) The SNOW Board Reference Design (PMC-970285) shows a very robust supply bypassing scheme. However, it requires a large number of components and is excessive for most applications. A reduced bypassing scheme is as follows:

- Bypass digital supply pins (VDD) as you would any other CMOS components: bulk capacitance somewhere on the board, with 0.1µF capacitors providing high-frequency bypassing near the device pins.
- Bypass analog supply pins (TAVD, RAVD, QAVD) from the +5V power plane with five separate RC filters consisting of a series resistance and bypass capacitance. Groupings and values are as follows:
    - QAVD1,2,3: 5.1Ω series; 10µF, 0.1µF, 0.01µF capacitor to ground
    - RAVD1,3,4: 5.1Ω series; 10µF, 0.1µF, 0.01µF capacitor to ground
    - TAVD1,3: 10Ω series; 10µF, 0.1µF, 0.01µF capacitor to ground
    - RAVD2: 5.1Ω series; 47µF, 0.1µF, 0.01µF capacitor to ground
    - TAVD2: 5.1Ω series; 47µF, 0.1µF, 0.01µF capacitor to ground

Other bypassing schemes are also possible. Contact PMC-Sierra's technical support team at apps@pmc-sierra.com to discuss.

Q23) What are the suggestions for board layout for the SPECTRA-155?

A23) Refer to section 12.4, "Board Design Recommendations," in the SPECTRA-155 datasheet.

Q24) Are the SPECTRA-155 solder balls eutectic?

A24) Yes. Full details about the SPECTRA-155's TEBGA package are given in *Surface Mount Assembly of PBGA/TEGBA Packages* (PMC-970951). This document is available from your PMC-Sierra sales representative or from the PMC-Sierra website (http://www.pmc-sierra.com).

6 CONFIGURATION AND SOFTWARE QUESTIONS

Q25) Are there software drivers available for the SPECTRA-155?

A25) Yes. A basic software driver package is available under a zero-cost license from PMC-Sierra. Drivers are written in ANSI C and provide an API into device configuration and diagnostic functions. See the PMC-Sierra web site to register for the drivers (http://www.pmc-sierra.com) or contact your PMC-Sierra sales representative.

A more advanced driver set, including standards-compliant failure monitoring and performance monitoring, is available for a fee from a third party developer, Applied Telecom (http://www.apptel.com).

Q26) How powerful a CPU do I need to run the SPECTRA-155?

A26) A slow 8-bit microcontroller can easily configure and supervise a single SPECTRA-155 in any standard applications not requiring DCC access:

- All consequential actions requiring fast turnaround times (125µs or faster), like REI counts and RDI or AIS insertion, are handled automatically by the SPECTRA-155 and do not require processor intervention.
- Significant overhead bytes are captured and debounced in hardware. Optionally, interrupts may be generated to inform the CPU when overhead values have changed.
- Performance monitoring registers (BIP and REI counts, for example) may be read as slow as once a second without overflowing.

DCC access may require additional processing power to handle the 768kb/s data rates of the DCC channels and the complex DCC protocol stack. A more powerful CPU with integrated HDLC communications controller may be preferable for such applications. If multiple SPECTRA-155s are populated on one board, a HDLC controller (such as PMC's FREEDM products) may be more appropriate.

Q27) How do I configure the SPECTRA-155 for SONET?

A27) There is no one register that will configure the SPECTRA-155 for SONET operation. Instead, each functional block (such as the pointer interpreter) is configured independently.

The default SPECTRA-155 configuration is essentially a SONET configuration. A description of the major configuration differences between SONET and SDH

applications is given in the *SPECTRA-155 Programmer's Reference* (PMC-980901). This document is available from your PMC-Sierra sales representative or from the PMC-Sierra website (http://www.pmc-sierra.com).

Q28) How do I configure the SPECTRA-155 for SDH?

A28) There is no one register that will configure the SPECTRA-155 for SDH operation. Instead, each functional block (such as the path overhead processor) is configured independently.

A description of the major configuration differences between SONET and SDH applications is given in the *SPECTRA-155 Programmer's Reference* (PMC-980901). This document is available from your PMC-Sierra sales representative or from the PMC-Sierra website (http://www.pmc-sierra.com).

Q29) Are there any register bits I have to set to make SPECTRA-155 work?

A29) The basic operating mode of SPECTRA-155 can be configured in register 00h. Also, bit 7 of register 40h should be set to logic 1 to ensure correct operation of the CRU. Other register settings to enable alarms, consequential actions, or diagnostics are very applications specific. Please consult the *SPECTRA-155 Programmer's Reference* (PMC-1980901) or contact PMC Applications for assistance with configuring the device for a particular application.

Q30) How do I configure the SPECTRA-155 for automatic enhanced path RDI consequent actions?

A30) The SPECTRA-155 may be configured to automatically report either standard or enhanced path RDI (RDI-P) codes as a consequent action to certain defects. Although both SONET and SDH define standard RDI-P codes (bit 5 of G1), the enhanced codes (bits 5-7 of G1) are applicable only in SONET.

Configuration of standard RDI-P codes is straightforward: simply set the bits corresponding to the desired defects in registers 102, EF, F2, and F3h. Configuration of enhanced RDI-P codes is not quite as simple because bit 5 of the RDI-P is treated independently of bits 6 and 7. Table 2 gives register configurations to enable automatic reporting of enhanced path RDI (RDI-P) in response to defect conditions. The generated RDI-P codes are compliant with Bellcore GR-253-CORE Issue 2 requirements.

Table 2 - Enhanced RDI-P Configuration Values

Defect	Configuration	RDI-P Code
LOS, LOF, or AIS-L	ALMPRDI=1 (reg 102, F2, F3h) NOALMEPRDI=1 (reg F4, F5, F6h)	101

Defect	Configuration	RDI-P Code
AIS-P	PAISPRDI=1 (reg 102, F2, F3h) NOPAISEPRDI=1 (reg F4, F5, F6h)	101
AISC-P	PAISCONPRDI=1 (reg EFh) NOPAISCONEPRDI=1 (reg EFh)	101
LOP-P	LOPPRDI=1 (reg 102, F2, F3h) NOLOPEPRDI=1 (reg F4, F5, F6h)	101
LOPC-P	LOPCONPRDI=1 (reg 102h) NOLOPCONEPRDI=1 (F4h)	101
UNEQ-P	UNEQPRDI=1 (reg EFh, F2, F3h) UNEQEPRDI=1 (reg EFh, F5, F6h)	110
TIM-P†	TIMPRDI=1 (reg 102, F2, F3h) TIMEPRDI=1 (reg F4, F5, F6h)	110
TIU-P†	TIUPRDI=1 (reg 102, F2, F3h) TIUEPRDI=1 (reg F4, F5, F6h)	110
PLM-P	PSLMPRDI=0 (reg 102, F2, F3h) PSLMEPRDI=1 (reg F4, F5, F6h)	010

†TIM-P is not currently defined in Bellcore standards. However, when implemented, it will be considered a connectivity defect (as is UNEQ-P). TIU-P is not defined in Bellcore, but would be treated the same as TIM-P.

For the above RDI-P codes to be inserted in the transmit stream, the SPECTRA-155 must be configured to insert enhanced RDI by setting EPRDIEN=1, EPRDISRC=1 (reg 130h, 170h, 1B0h).

To disable automatic enhanced RDI-P assertion due to any of the defects in column 1 of Table 2, clear all of the associated bits from column 2.

Q31) How do I configure the SPECTRA-155 to pass path overhead transparently?

A31) In the Telecom bus modes, SPECTRA-155 will be completely transparent to path overhead and payload when configured as follows:

- Register 106h=38h (TDIS1=TDIS2=TDIS3=1). This will disable all path overhead insertion (except for H4).
- Register 128h=40h, 168h=40h, 1A8=40h (H4BYP=1). This will disable regeneration of H4 and clearing of fixed stuff in the transmit direction.

- Register 140h=40h, 180h=40h, 1C0h=40h (H4BYP=1). This will disable regeneration of H4 and clearing of fixed stuff in the receive direction.

Q32) How should software process SPECTRA-155's interrupts, interrupt enables, and auxiliary interrupts?

A32) A complete description of the SPECTRA-155 interrupt hierarchy is given in the *SPECTRA-155 Programmer's Reference* (PMC-980901). This document is available from your PMC-Sierra sales representative or from the PMC-Sierra website (http://www.pmc-sierra.com).

7 DEBUGGING QUESTIONS

Q33) When I configure the SPECTRA-155 for line loopback, it passes data perfectly. But in system-line loopback I get errors. What is wrong?

A33) In line loopback mode (LLE, register 00h) the SPECTRA-155 directly connects the received signal to the transmit without any processing. In system-line loopback (SLLBEN, register 107h) the SPECTRA loops the Drop bus to the Add bus, performing all overhead and pointer processing functions on the datastream.

The most likely reason you are seeing AIS is that the SPECTRA-155 is generating AIS as a consequent action to a trail-trace identifier (TTI) mismatch. For debug purposes, the easiest solution is to turn off all default consequent actions by writing 00h to registers F0h, F1h, F2h, F3h, 101h, and 102h. This configuration also turns off the default RDI consequent action.

Alternate solutions are to update the expected TTI message buffer in the SPECTRA-155 to match the message sent by the test equipment, or to update the transmitted message in the test equipment to match the default expected message (all 00h).

Q34) I've configured the SPECTRA-155 to pass path overhead transparently (TDIS=1), but I get continuous B3 errors. What is wrong?

A34) The TDIS bit disables overwriting of all path overhead bits except H4. If H4 bypass is not also enabled, the SPECTRA-155 will modify H4 but will not make the corresponding changes to the B3 value, resulting in B3 errors. Bypass H4 by setting H4BYP=1 in registers 128, 168, 1A8, 140, 180, and 1C0.

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