PM6388

PM6388™ EOCTL

EOCTL

Octal E1 Framer

Device Errata

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Legal Information

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PMC-1980835 (R2)

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Patents

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Revision History

Issue No.	Issue Date	ECN #	Details of Change
1	July 27, 1998	None	Notification of additional information and errors to EOCTL Data Sheet Issue P4.
2	May 2001	3984	HDLC controller bit (section 2.1 – 2.3) Transmit Backplane Configuration (section 3.1), CEFP pin description (section 3.2)

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1 Introduction

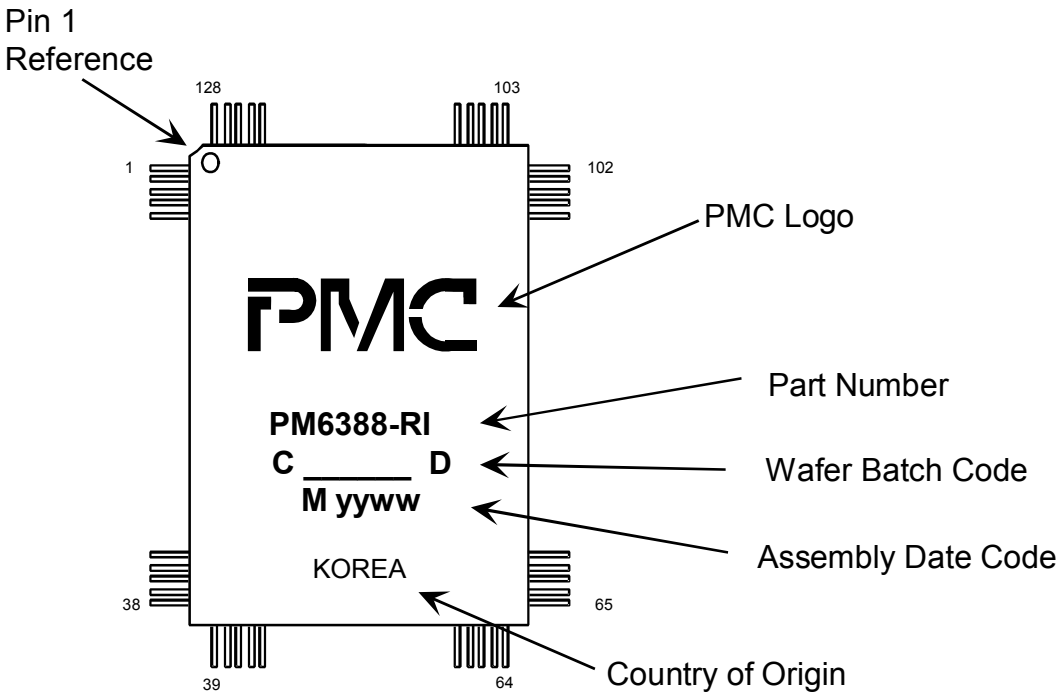
In this document:

- Section 2 lists the known functional errata for Revision D of the PM6388 EOCTL.
- Section 3 lists documentation errors found in Issue 6 of the Data Sheet (PMC-1971019).

1.1 Device Identification

The information contained in Section 2 relates to Revision D of the PM6388 Device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device.

Figure 1 PM6388 EOCTL Branding Format



1.2 References

- Issue 6 of the Device PM6388 EOCTL Data Sheet (PMC-1971019).
- PM6388 EOCTL Technical Overview, Issue 1 (PMC-1971173).

2 Device Functional Deficiency List

This section lists the known functional deficiencies for Revision D of the EOCTL as of the publication date of this document. For each deficiency, the known workaround and the operating constraints, with and without the workaround, are also described.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

2.1 Use of the HDLC Controller in E1 Mode (Internal HDLC Controller and Idle Code Insertion)

2.1.1 Description

The two least significant bits of timeslot N, where N is a number between 0 and 31, can be corrupted when any of the below statements are true:

1. Timeslot N+1 is configured for HDLC transmission (via the TDPR) and timeslot N is configured for idle code insertion (via the TPSC).

2. Timeslot N is configured for both HDLC transmission and idle code insertion.

3. Timeslot 31 (N = 31) is configured for idle code insertion and the Si-bit of timeslot 0 is configured for HDLC transmission.

2.1.2 Workarounds

The following workarounds apply to the above statements respectively:

1. External insertion of idle codes or the use of an external HDLC controller will prevent idle code data corruption. We recommend you use an external HDLC controller if it is necessary to insert idle codes in a timeslot immediately preceding HDLC data.

2. Disable idle code insertion for timeslots that are also configured to transmit HDLC data.

3. External insertion of idle codes or the external insertion of HDLC data in the Si-bit position will prevent idle code data corruption.

2.1.3 Performance with workaround

Normal operation.

2.1.4 Performance without workaround

The two least significant bits of timeslot N may be corrupted.

2.2 Using the Internal HDLC Controller for Timeslot One

2.2.1 Description

If data is inserted into timeslot 1 (via the internal HDLC controller) and the Sa8-bit is configured as externally inserted (via the backplane), the Sa8-bit can be corrupted.

2.2.2 Workarounds

The Sa8 bit is not corrupted when insertion is done via the E1-TRAN National Bits Codeword register. We recommend you do not use an internal HDLC Controller for timeslot one.

2.2.3 Performance with workaround

Normal operation.

2.2.4 Performance without workaround

The Sa8-bit can potentially be corrupted.

2.3 Using the Internal HDLC Controller to Insert Data in Sa-bit Positions

2.3.1 Description

If the internal HDLC controller is used to insert HDLC data in the Sa8, Sa7, Sa6 or Sa5 bit positions, the more significant bit adjacent to the inserted bit can be corrupted. In other words, HDLC data inserted in Sa8 can corrupt Sa7 and likewise data inserted in Sa5 can corrupt Sa4.

2.3.2 Workarounds

National Use Bits (Sa-bits) inserted using the internal E1-TRAN block are always inserted correctly. Avoid using the internal HDLC controller to insert data into the Sa8, Sa7, Sa6, and Sa5 bit positions.

2.3.3 Performance with workaround

Normal operation.

2.3.4 Performance without workaround

Potential corruption of a National Use (Sa) bit.

3 Documentation Deficiency List

This section lists the known documentation deficiencies for Issue 6 of the Data Sheet (PMC-1971019) as of the publication date of this document.

For each *specific* deficiency, the location of the passage in question, the deficient text, and the replacement text are described. New text is shown in bold. Deleted text is shown as underlined.

For more *general* issues, a description of the nature of the error is given, along with a passage that correctly describes the concept or device function.

Please report any documentation deficiencies not covered in this document to PMC-Sierra.

3.1 Transmit Backplane Configuration

Registers 018H, 098H, 118H, 198H, 218H, 298H, 318H, 398H: Transmit Backplane Configuration.

3.1.1 Location

The description of the Transmit Backplane configuration registers is found in section 10 – Normal Mode Register Description - (on page 98 of the PM6388 EOCTL datasheets).

3.1.2 Original Wording

The framing edge (FE) bit determines the edge of CECLK on which the frame pulse (CEFP) pulse is sampled. If FE is a logic 0, CEFP is sampled on the falling edge of CECLK. If FE is a logic 1, CEFP is sampled on the rising edge of CECLK. In the case where FE is not equal to DE, FE is sampled or updated one clock edge before DE. This bit only has effect in clock slave mode.

3.1.3 Replacement Wording

The framing edge (FE) bit determines the edge of CECLK on which the frame pulse (CEFP) pulse is sampled. If FE is a logic 0, CEFP is sampled on the falling edge of CECLK. If FE is a logic 1, CEFP is sampled on the rising edge of CECLK. **In the case where FE is not equal to DE, EFP is sampled one clock edge before or updated three clock edges before ED and ESIG are sampled.** This bit only has effect in clock slave mode**.**

3.2 CEFP Pin Description

CEFP - Common Egress Frame Pulse.

3.2.1 Location

The CEFP pin description given in the table in section 8 (page 19).

3.2.2 Original Wording

Common Egress Frame Pulse (CEFP). CEFP may be used to frame align the framers to the system backplane. If frame alignment only is required, a pulse at least 1 CECLK cycle wide must be provided on CEFP every 256 bit times.

3.2.3 Replacement Wording

Common Egress Frame Pulse (CEFP). CEFP may be used to frame align the framers to the system backplane. If frame alignment only is required, a pulse at least 1 CECLK cycle wide must be provided on CEFP every 256 bit times.

If operating in "Mixed Mode" (some framers operating in Clock Master Mode and other framers operating in Clock Slave mode) while the Clock Master Mode PLL is referenced to RLCLK[x], you should remove CEFP after the framers in Clock Slave Mode are aligned.

Notes