

PM7346



S/UNI-QJET

**ANSWERS TO FREQUENTLY ASKED
QUESTIONS REGARDING THE
S/UNI-QJET**

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ITU-T Recommendation G.832 - "Transport of SDH Elements on PDH Networks: Frame and Multiplexing Structures", 1993.

ITU-T Recommendation Q.921 - "ISDN User-Network Interface - Data Link Layer Specification", March, 1993.

NTT Technical Reference, "NTT Technical Reference for High-Speed Digital Leased Circuit Services", 1991.

2 GLOSSARY OF TERMS

ADM	ATM Direct Mapping. This refers to the asynchronous mapping of ATM cells directly into the S/UNI-QJET DS3, E3, or J2 payload. A complete description of this mapping can be found in ITU-T G.804.
BGA	Ball Grid Array. This term refers to a type of pack for ICs. The package is electrically connected to the circuit board via conductive balls arranged in a grid pattern on the underside of the package. The QJET device is packaged in a BGA.
DS3	Digital Service Level 3. This term refers to a standardized format for digital signals which is comprised of seven DS2 signals asynchronously multiplexed plus overhead for a sum of 4760 bits sent at a 44.736 MHz bit rate. Note that the frame rate is not 8 kHz.
J2	Japanese Transmission Format Order 2. This is a generic term for a standardized format for digital signals comprised of 98 DS0s plus overhead for a sum of 789 bits repeated at an 8 kHz repetition rate for a total bandwidth of 6312 kbit/s.
PLCP	Physical Layer Convergence Protocol. This is a framing pattern and payload inserted asynchronously into the S/UNI-QJET DS3, E3, or J2 payload. The payload is filled with 53 byte ATM cells. PLCP is defined in IEEE 802.6.
T3	Transmission Format Order 3. This is a generic term that refers to transmission systems, interfaces and equipment that process DS3-formatted signals.
LIU	Line Interface Unit. This refers to a device that takes digital signals (such as a T3) from a framer and electrically formats them for transmission (for instance, over a DS3).

3 BACKGROUND AND OVERVIEW

PMC-Sierra's PM7346 S/UNI-QJET is a single chip quad ATM User Network Interface. The device has integrated J2, E3, and T3 framers that can be individually selected per channel. In addition, the framers can be bypassed to allow support of some arbitrary bit rate using an external framer. ATM functionality may also be bypassed so that the device may be used as a framer only.

In order to help customers quickly find the answers to their questions, the following list of answers to frequently asked questions has been compiled.

In this document, the term "QJET" will refer to the PM7346 S/UNI-QJET device.

4 ANSWERS TO FREQUENTLY ASKED QUESTIONS

Q1) Are there any reference designs or application notes available for the QJET?

A1) Yes. There are 2 application notes available for the QJET:

- Comparison of PLPP, S/UNI-PDH, and S/UNI-QJET register space, PMC-961125. This document is intended as an aid to assist users of the PLPP and S/UNI-PDH in migration to the PM7346 S/UNI-QJET.
- S/UNI-QJET Technical Overview, PMC-971016. This document contains an overview of the QJET, with short, concise descriptions of the various functions of the QJET.

There is not currently a reference design available for the QJET. A paper reference design using the QJET and PM7364 FREEDM-8 will be available in June 1998. Customers should regularly check our website for new and updated application notes, reference designs, and datasheet errata.

Q2) Are there any software drivers available for the QJET?

A2) Yes. Software drivers for many of PMC-Sierra's components, including the QJET, are available by accessing the following web page:
<http://www.pmc-sierra.com/softwarefiles/default.asp>

Q3) The QJET uses a 3.3 V supply and 5 V bias. What is the correct power supply sequencing for powering up the QJET?

A3) Correct power supply sequencing is important to prevent accidental damage to the QJET. The voltage applied to VDD[1:28] must never exceed the voltage on BIAS by more than 0.7 V. Therefore, BIAS must be applied before VDD. In practice, this is easily implemented by placing a 1N5817M zener diode between the +5V supply and the +3.3V supply. This will ensure that BIAS is not lower than VDD by more than 0.7V.

Q4) Do all the channels of the QJET need to be configured identically?

A4) No. Each of the four transmitters and four receivers can be configured independently.

Q5) Are there any 3.3 V Line interface units available to interface to the QJET?

A5) No. At the time this document was created, there were no 3.3V DS3, E3, or J2 LIUs available on the market.

Q6) What LIU does PMC-Sierra recommend for DS3 and E3 applications?

A6) PMC-Sierra's evaluation board uses the TSC 78P7200 DS3/E3 LIU. This is the same LIU that was used on the D3MX reference design and S/UNI-PDH reference design. Because this is a 5V LIU, level conversion must take place between the outputs from the QJET and the inputs to the LIU. This is easily accomplished using a TTL Buffer.

Q7) What LIU does PMC-Sierra recommend for J2 applications?

A7) PMC-Sierra's evaluation board uses the Transwitch TXC-02050 J2 LIU. Because this is 5V LIU, level conversion must take place between the outputs from the QJET and the inputs to the LIU.

Q8) What standards apply to the QJET?

A8) A list of relevant standards can be found in the 'references' section of the S/UNI-QJET datasheet.

Q9) What BGA socket is recommended for prototyping with the QJET?

A9) For testing and prototyping with the QJET, PMC-Sierra uses BGA sockets from:

Yamaichi Electronics U.S.A., Inc.
2235 Zanker Road
San Jose, CA 95131
U.S.A.
Phone: (408) 456-0797
Fax: (408) 456-0799
Web site: <http://www.yeu.com>

Q10) Can the QJET be interconnected with 5V devices?

A10) The inputs to the QJET are 5V tolerant if BIAS is applied correctly. Therefore nothing need be done on QJET inputs to accommodate connection with 5V devices. QJET outputs are TTL level compatible. Care must be taken to ensure that the inputs to the 5V device are also TTL compatible.

5 NOTES

6 CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Phone: (604)415-4533
Fax: (604)415-6206
Web Site: <http://www.pmc-sierra.com>

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