PM7366

FREEDM-8

FRAME ENGINE AND DATA LINK MANAGER

TECHNICAL OVERVIEW

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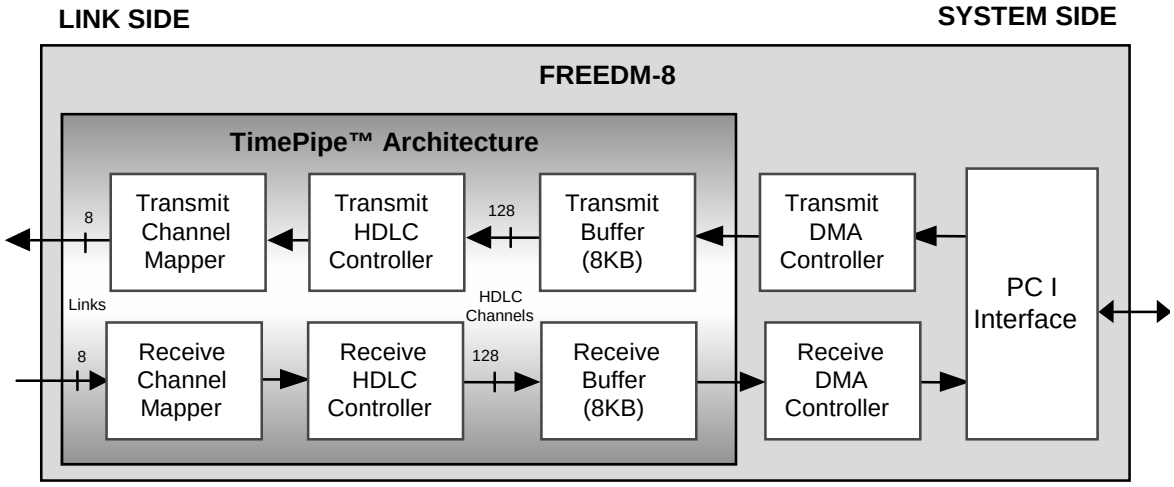
CONTENTS

1 OVERVIEW

The **FR**ame **E**ngin**E** and **D**ata Link **M**anager (FREEDM-8) is an advanced data link layer processor that is ideal for applications such as Internet access equipment, frame relay switches, ATM switches, packet-based CDMA base station controllers and Digital Subscriber Loop Access multiplexers (DSLAM).

The cornerstone of the FREEDM-8 product is the revolutionary TimePipe™ architecture (as shown in Figure 1). The TimePipe architecture enables a single FREEDM-8 device to support up to 8 full-duplex physical links, 128 HDLC channels and 8 KB of integral packet buffer in each of the transmit and receive direction. Each one of the 8 physical links can be independently timed from 56 Kbit/s to 52 Mbit/s. This unparalleled level of integration not only simplifies networking equipment designs, but also enables a new generation of line card designs that can use a common data link layer processor for a wide variety of line rates ranging from T1, E1, E3, T3 to HSSI.

Figure 1: FREEDM-8 Block Diagram and the TimePipe Architecture



Power is useful only if it can be directed to perform the intended work. The TimePipe architecture is not only powerful but also highly configurable as well. A flexible channel mapper mechanism is provided such that any link can be assigned to any HDLC channel in software. In the case of a channelized application, data carried on one or more time-slots within the same link can be grouped and assigned to a single HDLC channel.

The 8KB packet buffer can be flexibly allocated to active HDLC channels. The 8KB buffer is organized as 512 blocks of 16 byte FIFOs. The number of blocks assigned to any HDLC channel is configurable in software.

In the receive direction, the Receive HDLC Controller performs flag delineation, bit destuffing, CRC verification using either CRC-32 or CRC-CCITT algorithm and length checking. In the transmit direction, the Transmit HDLC Controller performs flag insertion, bit stuffing and FCS calculation using either CRC-32 or CRC-CCITT algorithm.

On the system side, FREEDM-8 provides a 33 MHz, 32 bit PCI 2.1 compliant bus interface. Two efficient transmit and receive DMA controllers are provided to support burst data transfers across the PCI bus.

FREEDM-8 is packaged in a 256 pin BGA package with a physical dimension of 27 mm by 27 mm.

1.1 Additional FREEDM-8 Documentation

A list of FREEDM-8 documents is provided below. Please contact PMC-Sierra for an updated list.

Document Number	Document Title
PMC-970532	FREEDM-8 Short Form Datasheet
PMC-970931	FREEDM-8 Technical Overview
PMC-970930	FREEDM-8 Datasheet
PMC-970935	FREEDM-8 Bus Utilization and Latency Test Application Note
PMC-970933	Interfacing FREEDM-8 to the ST-Bus Application Note.

2 APPLICATION EXAMPLES

FREEDM-8 is ideal for networking equipment supporting a large number of data links. Figure 2 shows the typical architecture for an Internet access concentrator.

Figure 2: Typical Architecture of an Internet Access Concentrator

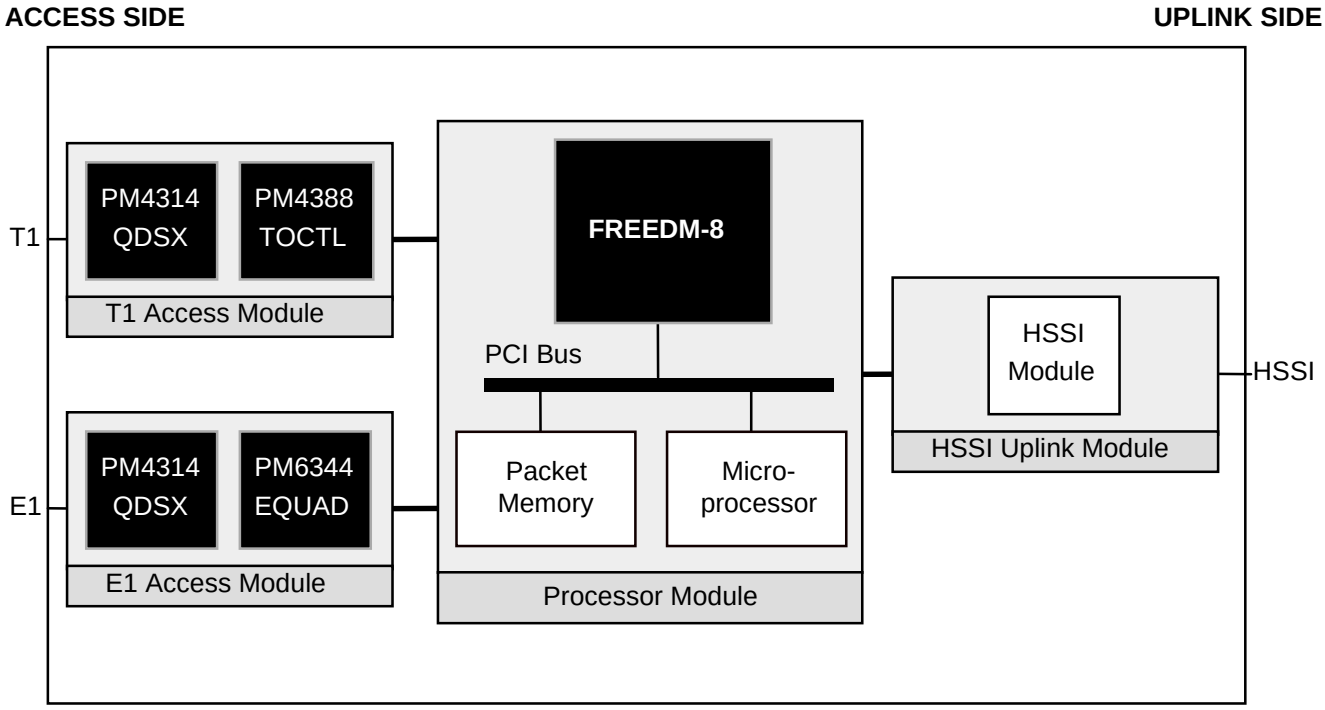
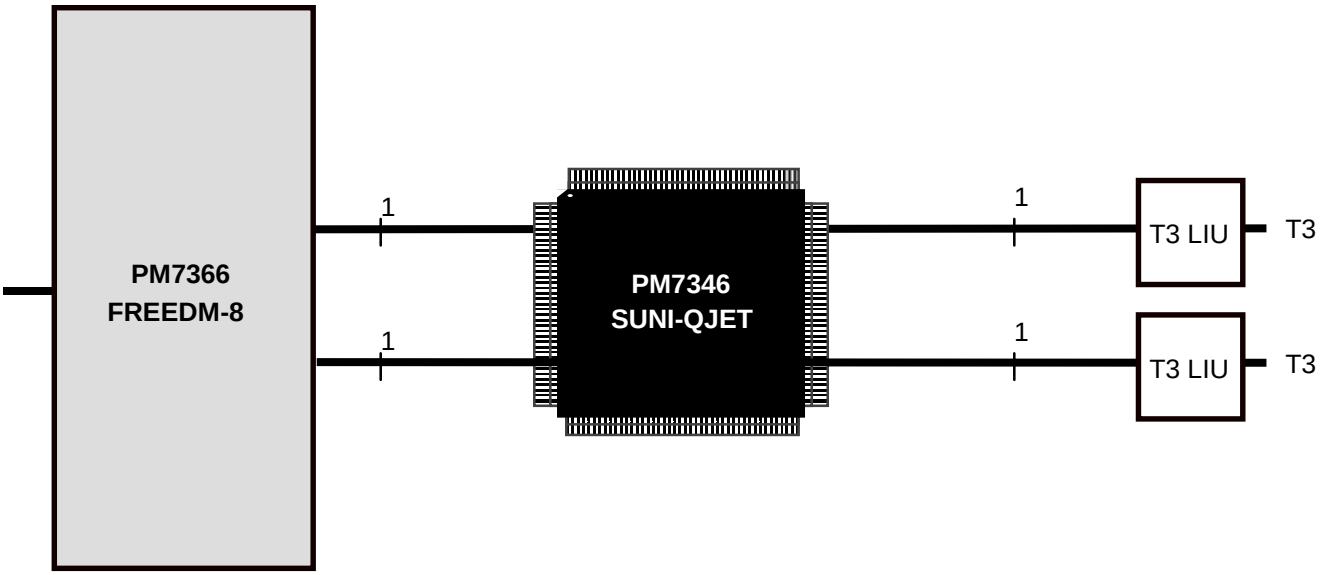
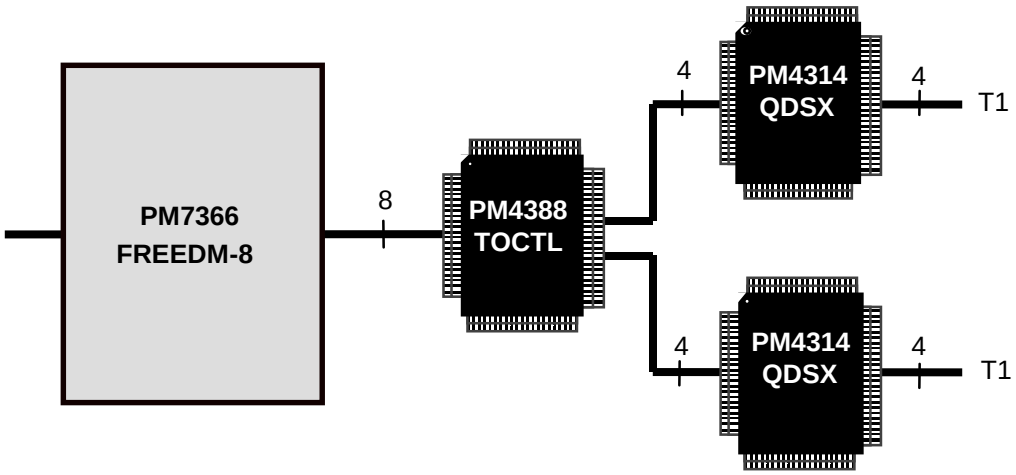


Figure 3: 2 unchannelized DS3 links using FREEDM-8 and a SUNI-QJET



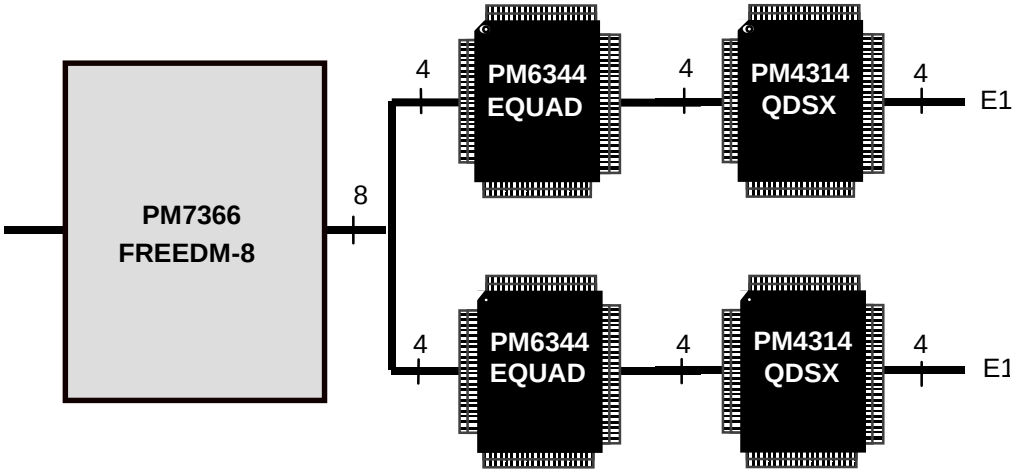
For direct T1 access, the TOCTL seamlessly interfaces to two PM4314 QDSX to support eight T1 links as shown in Figure 4. The QDSX integrates four full-featured T1/E1 duplex DSX-1 compatible line interface circuits in a single device. The QDSX is currently in production and is packaged in a 128 PQFP.

Figure 4: 8 Channel T1 Interface for Frame Relay or Internet Access



For direct E1 access, the EQUAD seamlessly interfaces to two PM4314 QDSX to support eight E1 links as shown in Figure 5. The QDSX integrates four full-featured T1/E1 duplex DSX-1 compatible line interface circuits in a single device. The QDSX is currently in production and is packaged in a 128 PQFP.

Figure 5: 8 Channel E1 Interface for Frame Relay or Internet Access

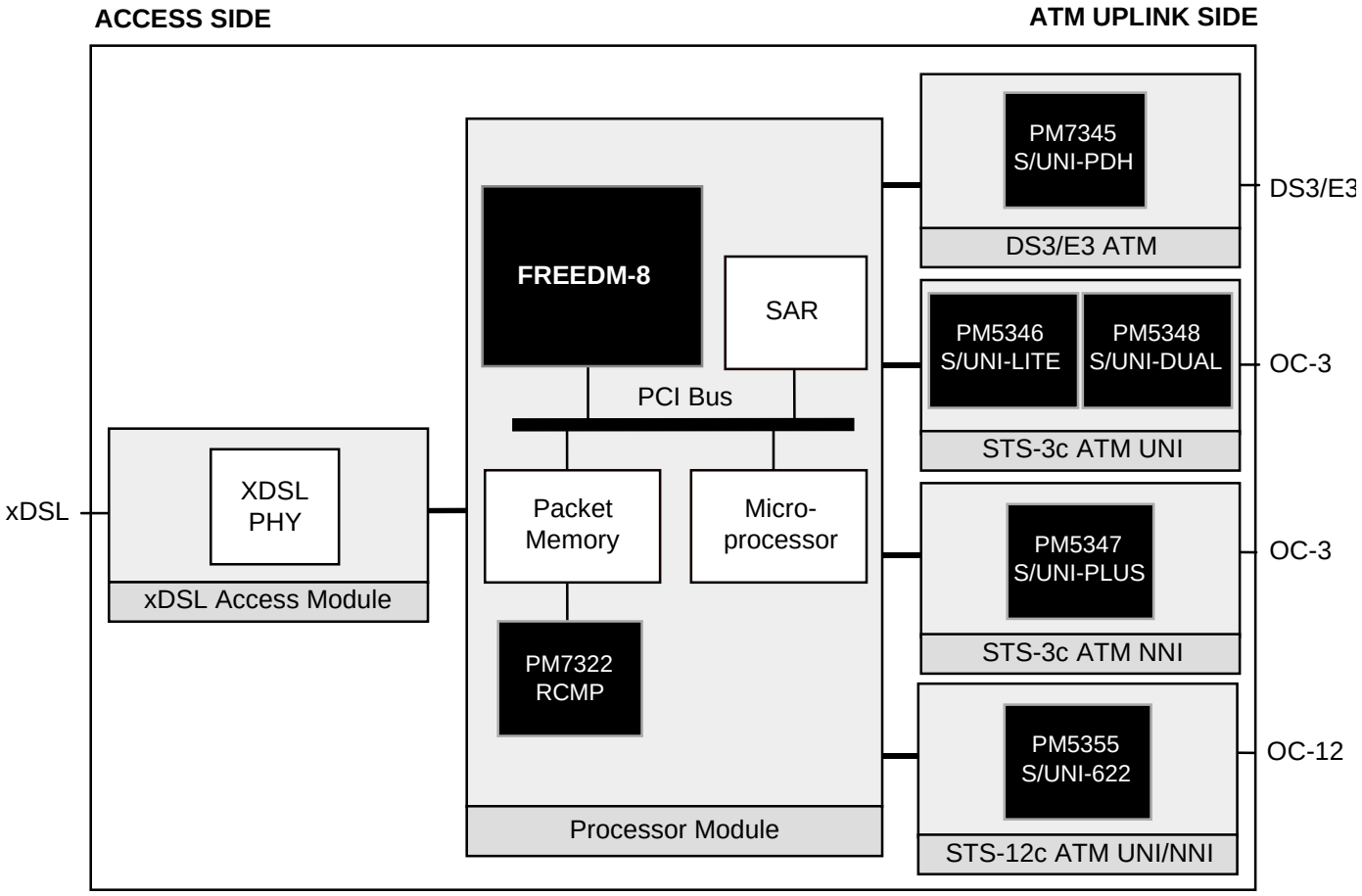


On the uplink side, FREEDM-8 can interface to two high speed links such as HSSI, DS-3 or E3.

FREEDM-8 can also be used on the access side of a packet-based DSLAM to interface with xDSL physical layer devices (as shown in Figure 6). In this application, FREEDM-8 performs data link layer processing on packet data transferred between the xDSL network and the packet memory. For a DSLAM with ATM uplinks, a segmentation and reassembly (SAR) device is required to convert packets into ATM cells. The cells are switched by an ATM switching fabric (not shown) and sent out on one of the ATM uplinks:

- The PM7346 S/UNI-PDH can be used for a DS-3/E3 ATM uplink;
- The PM5346 S/UNI-LITE or PM5348 S/UNI-DUAL can be used for an OC-3 ATM UNI uplink;
- The PM5347 S/UNI-PLUS can be used for an OC-3 ATM NNI uplink;
- The PM5355 S/UNI-622 can be used for an OC-12 ATM UNI or NNI uplink.

Figure 6: DSLAM with ATM Uplinks



3 GLOSSARY

Bit Stuffing	A process in data communications protocols where a string of "one" bits in the data payload is broken by an inserted "zero". The idea of inserting the zero is to ensure that no flag control character is found in the user payload.
CRC	Cyclic Redundancy Check: Check sums generated from recursive algorithms that can be used to determine the integrity of data by a receiver. Certain CRC algorithms allows the receiver to detect as well as correct certain number of bit errors.
DLCI	Data Link Connection Identifier (DLCI): The frame relay virtual circuit number corresponding to a particular destination which is part of the frame relay header and is usually ten bits long. The DLCI is typically associated with a particular PVC on the network.
DS-0	Digital Service, level 0: There are 24 DS-0 channels in a DS-1. Each DS-0 has a bandwidth of 64 Kbit/s.
DS-1	Digital Service, level 1: It is 1.544 Mbit/s in North America. In channelized mode, each DS-1 consists of 24 DS-0 channels. In unchannelized mode, each DS-1 has a full-duplex bandwidth of 1.544 Mbit/s.
DS-3	Digital Service, level 3: DS-3 is equivalent to 28 DS-1 channels. It operates at 44.736 Mbit/s.
DSLAM	Digital Subscriber Loop Access Multiplexer:
FCS	Frame Check Sequence: Bits added to the end of a frame for error detection. In bit-oriented protocols, a frame check sequence is a 16-bit field added to the end of a frame that contains transmission error-checking information.
Flag	In synchronous transmission, a flag is a pattern of "01111110" used to mark the beginning and end of a frame.
FRAD	Frame Relay Access Device.

Frame	A frame is also referred to as a "packet" and is a logical transmission unit. A frame consists of a group of data bits in a specific format. Generally, a flag is used at each end of the frame to delimit the start and end of the frame.
Frame Relay	The term "frame relay" is used in multiple contexts and can be used to refer to a switching technology, an interface standard or a set of data services.
Full-Duplex	Refers to simultaneous transmission in two directions.
HDLC	High Level Data Link Control: A standard bit-oriented protocol developed by ITU.
HSSI	High Speed Serial Interface
ISP	Internet Service Provider:
Multiplexor	Electronic equipment which allows two or more signals to pass over one communication circuit.
NAP	Network Access Point:
OSI	Open System Interconnect: An ISO publication that defines seven independent layers of communication protocols. Each layer enhances the communication services of the layer just below it and shields the layer above it from the implementation details of the lower layer.
OSI Model	The only internationally accepted framework of standards for communication between different systems made by different vendors. The OSI model organizes the communications process into the following seven layers: Layer 1 - Physical Layer Layer 2 - Data Link Layer Layer 3 - Network Layer Layer 4 - Transport Layer Layer 5 - Session Layer Layer 6 - Presentation Layer Layer 7 - Application Layer
Packet	A packet is also referred to as a "frame" and is a logical transmission unit.
PCI	Peripheral Component Interconnect

POP	Point of Presence: In telecommunication, POP refers to the physical place within a LATA where a long distance carrier interfaces with the network of the local exchange carrier.
UNI	User Network Interface: The physical and electrical demarcation point between the user and the public network service provider.

4 NOTES

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