PM7346

S/UNI-QJET

INTERFACING THE S/UNI-QJET TO THE RCMP-800

PRELIMINARY

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CONTENTS

1 OVERVIEW

The RCMP-800 device provides ATM Layer VPI/VCI address translation, cell appending, cell rate policing, counting and OAM functions. It supports Multi-PHY addressing for up to 32 PHY devices as outlined in Utopia Level 2 specification. The RCMP-800 is intended to be situated between a switch core and the physical layer devices in the ingress direction. The S/UNI-QJET provides the PHY transmission convergence function to the RCMP-800.

Interconnecting the S/UNI-QJET to the RCMP-800 in Multi-PHY setup can be achieved by utilizing one cell available (RCA) and one read enable (RENB) signals. As specified in Utopia Level 2, only one Multi-PHY port at a time is selected for a cell transfer. However, another Multi-PHY port may be polled for its cell available status while the selected Multi-PHY port transfers data.

2 INTERFACE CONSIDERATIONS

The S/UNI-QJET supports either a 50 MHz 8-bit wide or 16-bit wide FIFO interface to the RCMP-800. The available ATM bandwidth of the interface is reduced to 706.6 Mbps because the RCMP requires three empty clock cycles after each received cell. The total number of QJETs that can be interfaced to the RCMP-800 can be decided by the system designer based on this available bandwidth. Table 1 shows typical QJET PHY port rates and the number of ports and QJETs that can be interfaced to one RCMP-800 at full traffic payload without dropping any cell. The maximum number of QJETs that can be interfaced to a single RCMP-800 device is 31. The QJET inputs present capacitive loading of 5 to 7 pF. The timing specifications described in the data sheets for the QJET and the RCMP-800 are measured at 50 pF load. It is recommended that buffering be provided when interfacing multiple QJETs to the RCMP-800.

Table 1: QJET Interface Rates

User Network Interface	ATM Payload Bandwidth (Mbits/s)*	Number of PHY Ports	Number of QJETs	Aggregate ATM Payload Bandwidth (Mbits/s)
T1	1.536	124	31	190.46
E1	1.920	124	31	238.08
J2	6.144	112	28	688.12
T3	39.34	17	5	668.78
E3	33.92	20	5	678,40

* T1, E1, E3, J2 based on ATM Cell Mapping, T3 based on PLCP Mapping,

The logic address of each QJET is determined by its PHY_ADR[2:0] inputs. The PHY_ADR[2:0] inputs correspond to the three most-significant bits of the RCMP's Multi-PHY addressing pins, IADDR[4:0]. The lower two bits, IADDR[1:0], determine which one of the four quadrants in the QJET is selected for transmit and receive access.

The selection between 16-bit or 8-bit data bus width for interfacing the S/UNI-QJET to the RCMP-800 is generally based on the aggregate speed of the Multi-PHY bus. For applications where the aggregate PHY devices bit rate is 200 Mbps or lower, 8-bit bus width is chosen. For speed of over 200 Mbps, 16-bit wide bus is used.

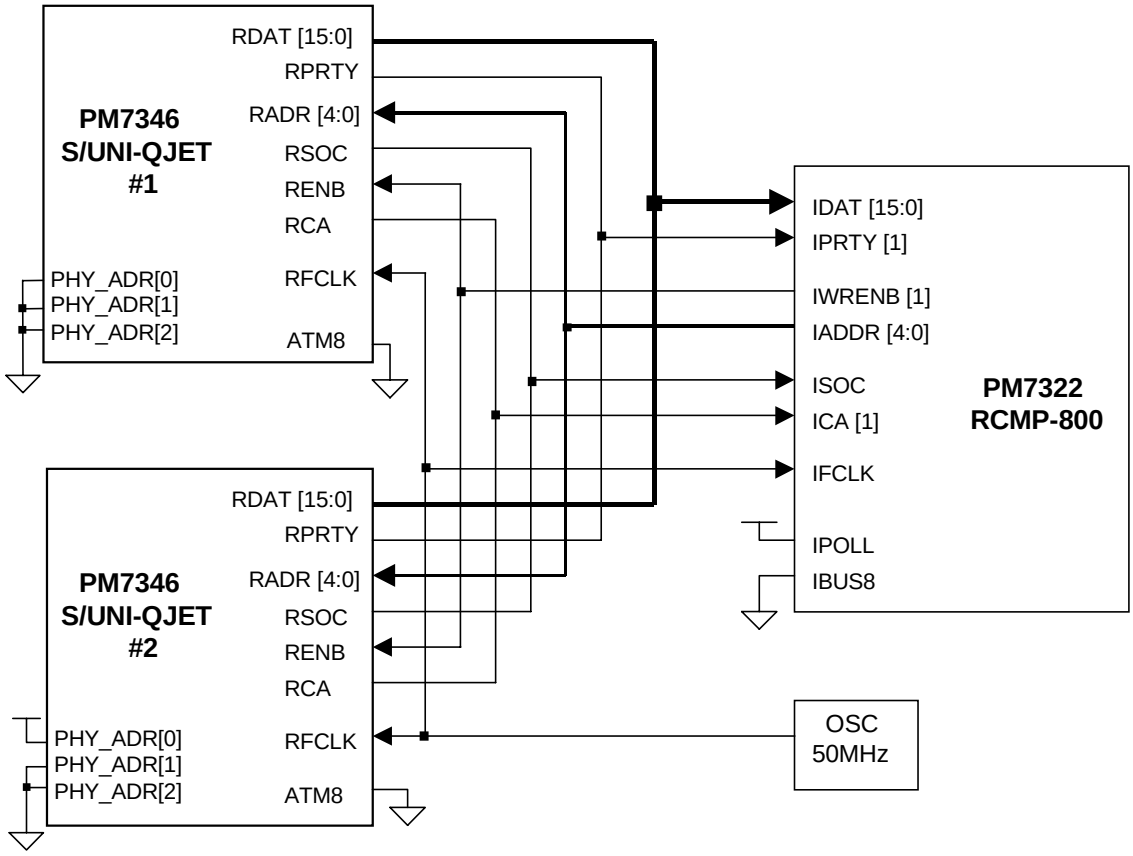
For 8-bit data bus operation, the QJET's ATM8 and the RCMP's IBUS8 pins need to be pulled high. Also, the IBYTEPRTY bit in RCMP's register 08H should be set to logic one and the RPRTY output on the QJET should be connected to the IPRTY[0] input on the RCMP.

For 16-bit data bus selection, the QJET's ATM8 and the RCMP's IBUS8 pins need to be pulled low. The IBYTEPRTY bit in RCMP's register 08H should be set to logic zero for word parity calculation and the QJET's RPRTY output should be connected to the RCMP's IPRTY[1] input.

3 CONNECTING THE S/UNI-QJET TO THE RCMP-800

Figure 1 shows the connections between 8 PHY ports on two S/UNI-QJETs and one RCMP-800. Both the ATM8 pin on the S/UNI-QJET and the IBUS8 pin on the RCMP-800 are pulled low to select the 16-bit wide data bus between the two devices. The nominal clock frequency for connecting four SCI-PHY devices to the RCMP-800 is 44.1 MHz. A 50MHz oscillator is chosen to satisfy this requirement. The IPOLL pin is pulled high to enable multi-PHY address polling function on the RCMP-800. The PHY_ADR[2:0] pins for QJET#1 and QJET#2 are tied to "000" and "001" respectively. Up to 31 QJETs can be connected to the RCMP-800 using the same connections as shown below using PHY addresses from 00H to 1EH.

Figure 1 Connections - Two S/UNI-QJETs and the RCMP-800



4 MULTI-PHY INTERFACE TIMING

The interface clock rate between the S/UNI-QJET and the RCMP-800 can be either set at 25 MHz or 50 MHz depending on the data bus size selected. The clock period is then 40 ns or 20 ns respectively. Figure 2 shows the QJET's output timings and the RCMP-800's timing requirements. For QJET outputs, the maximum time from clock high to output valid is 12 ns. This gives RCMP a minimum setup time of 28 ns at 25 MHz and 8 ns at 50 MHz. Also, for QJET outputs, the minimum time from clock high to output tristate is 1 ns. The minimum timing requirements for the RCMP Multi-PHY input pins, ICA[1], IDAT, IPRTY[1], and ISOC are 2 ns for setup and 1 ns for hold time. The S/UNI-QJET meets RCMP's setup and hold time requirements for both bus clock rate at 25 and 50 MHz with timing margins of 26 ns and 6 ns respectively. The extra timing margins will allow buffering to be provided between the QJET and the RCMP while still meeting the timing requirements. Buffers chosen to be added must contribute less than 26 ns for 25 MHz and 6 ns for 50 MHz of propagation delay to the data signals.

Figure 2: The S/UNI-QJET to the RCMP-800 timing

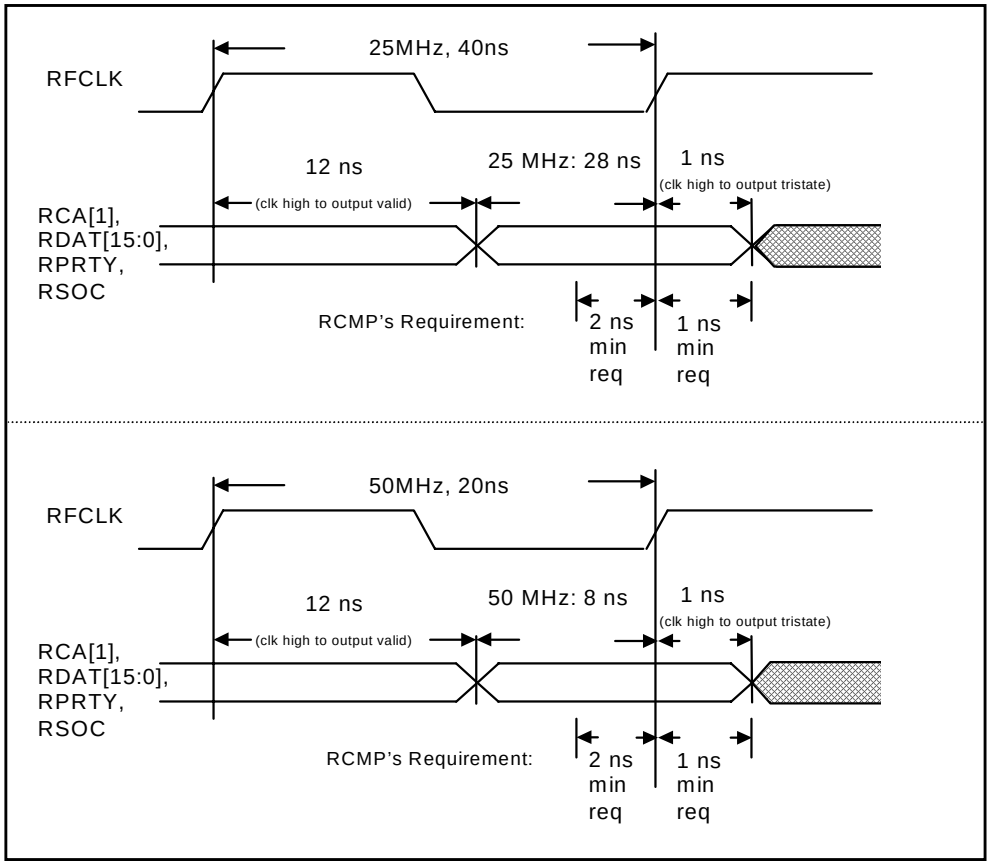
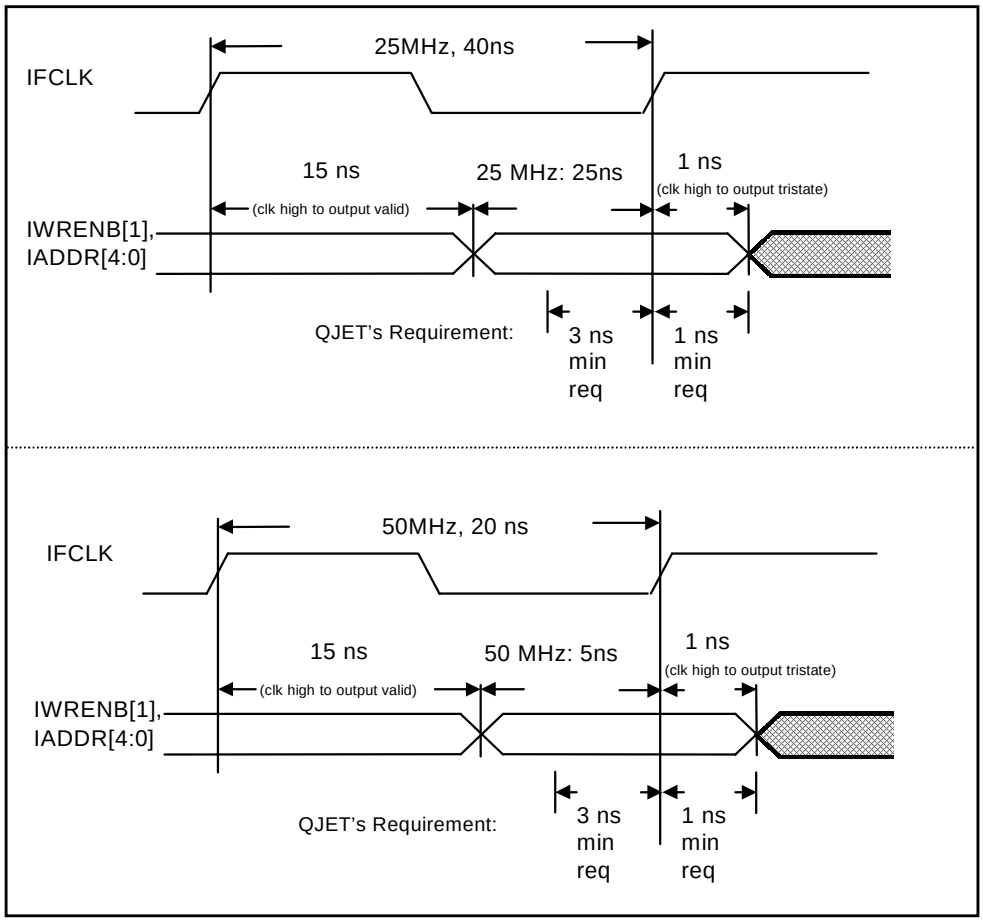


Figure 3 shows the timing requirements for the RCMP-800 to the S/UNI-QJET interface at both 25 and 50 Mhz. Since both devices conform to the Multi-PHY specs, the S/UNI-QJET has similar timing as the RCMP-800. The RCMP has a longer maximum propagation delay of 15 ns for its outputs. This still meets the timing requirements of the QJET inputs set-up time of 3 ns. So the RCMP-800 meets the timing requirements of the QJET for both the setup and hold time of RENB, and ADDR[4:0] signals.

Figure 3: The RCMP-800 to the S/UNI-QJET timing



5 REFERENCES

- PM7323 RCMP-800 Long Form Datasheet, PMC-930904, Issue 6
- PM7346 S/UNI-QJET Long Form Datasheet, PMC-960835, Issue 1
- ATM Forum, UTOPIA, An ATM-PHY Interface Specification, Level 2, Version 1.0
- ITU-T, G.804, ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH), Nov 1993

NOTES

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