PM5355

S/UNI-622™ ATM Reference Design with Multimode Optics Errata

Issue 1: August 14, 1997

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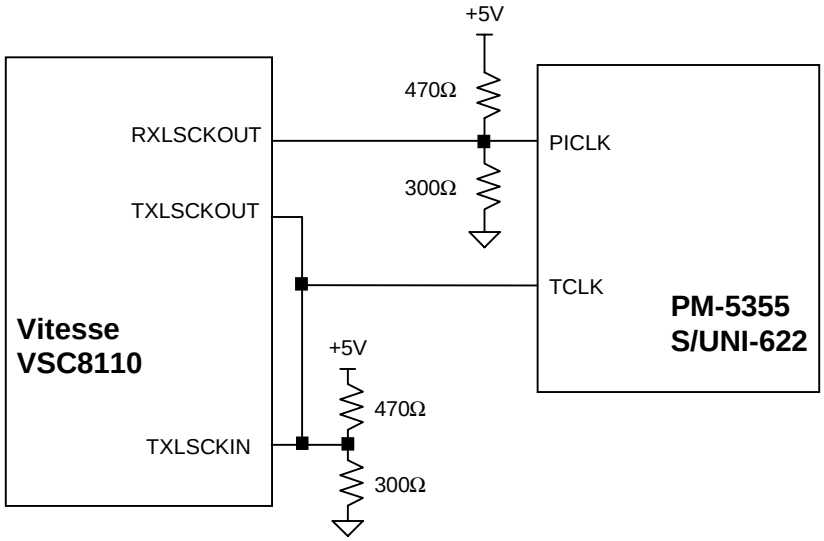
THE S/UNI-622 REFERENCE DESIGN ERRATA

This document is the errata notice for Issue 3 of the S/UNI-622 reference design with multimode optics. It addresses transmit and receive clock terminations and interfacing timing issues in the S/UNI-622 reference design.

1.0 TRANSMIT AND RECEIVE CLOCK TERMINATIONS

The Vitesse VSC8110 clock output loading presents a problem. The VSC8110 spec shows Vol = 0.5 V at 8 mA, and Voh = 2.4V at 2.4 mA. The original design has a 220Ω pullup resistor and a 330Ω pulldown resistor. Voh does not present a problem, but Vol would have to sink (3 V-0.5 V)/132Ω = 18.9 mA. This is 10.9 mA higher than what the VSC8110 can sink. To address the problem, the resistors should be changed to 470 Ω for the pullup one and 300 Ω for the pulldown one. Figure 1 shows the new pullup and pulldown resistors for both S/UNI-622's PICLK and VSC8110's TXLSCKIN terminations.

Figure 1. New values for the pullup and pulldown resistors



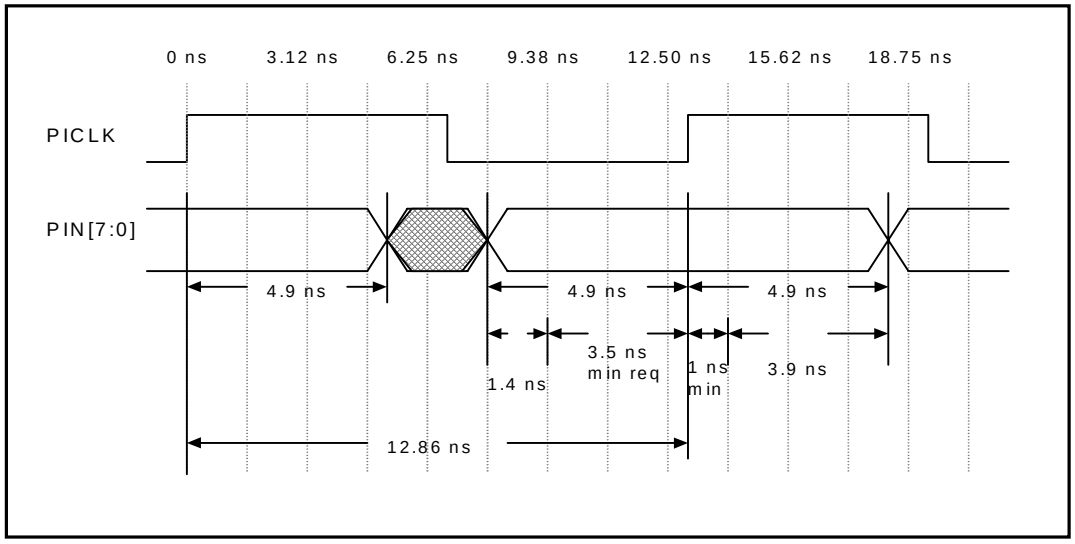
2.0 INTERFACE TIMING BETWEEN THE VSC8110 AND THE S/UNI-622

In the implementation section of sheet 2, S/UNI-622 Interconnect, on bottom of page 5, concerns were raised regarding to a 0.2 ns timing margin. This is shown as below. The entire section on the 0.2ns margin and the related timing diagram can be omitted since this timing requirement does not apply to the Vitesse VSC8110 and replaced with the following:

This identical timing exists with the FPIN input as well as the PIN[7:0]. ~~Since there is only a 0.2ns timing margin on the setup time (data valid to the rising edge of clock) on the FPIN and PIN[7:0] inputs, precautions must be taken to avoid skew between these inputs. In fact, a slight delay (in the order of 1-5ns) in the data path would be advantageous and a slight delay (greater than 0.2ns) in the clock path would be intolerable. Hold time is not a concern on this interface since only 3ns are required and there are 11.9ns available.~~ The Vitesse VSC8110 data sheet specifies that data is valid on RXOUT[7:0] at 4.9 ns before and after the rising edge of RXLSCKOUT. For the S/UNI-622, both the PIN[7:0] and FPIN has a setup time requirement of 3.5 ns and hold time of 1 ns. The Vitesse timing specification meets S/UNI-622's timing requirements with 1.4 ns margin for setup and 3.9 ns margin for hold time.

Figure 2 shows the new timing between the VSC8110 and the S/UNI-622.

Figure 2 VSC8110 and S/UNI-622 Receive Interface Timing



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