PM7375

LASAR™-155

LASAR OPTICAL NETWORK INTERFACE CARD (NIC) REFERENCE DESIGN

Preliminary Information
Issue 3: March 1996

CONTENTS

LIST OF CHANGES

The following changes have been made to the issue 2 of the document:

Document Changes

- Updated schematics
- Updated layout
- Added functional and layout description of the NIC card
- Added bill of material

Schematic Changes

- Removed all headers
- Removed U4 and its decoupling caps and pullups
- Changed regulators to 1.5 A 7805 TO220 packages
- Add additional solder bridges and decoupling caps
- Added chassis ground points

Layout Changes

- re-routed the analog portion of the PM7375 for manufacturability
- redefined the power and ground planes
- moved the location of U1 and the two bracket mounting holes

REFERENCES

PCI Special Interest Group, "PCI Local Bus Specification Revision 2.0", April 30, 1993

PMC-931127, LASAR-155 Longform Datasheet, Issue 3, March 5, 1996

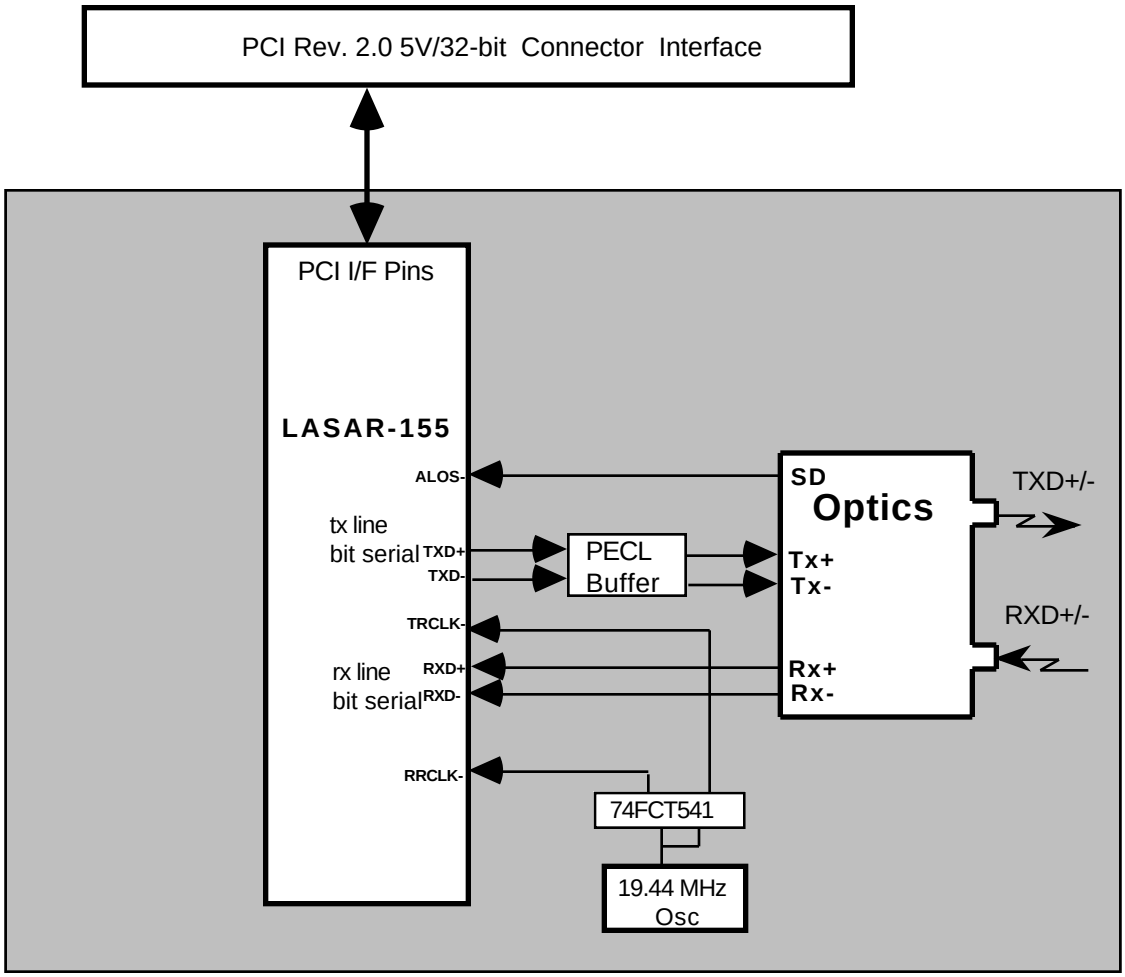
1. OVERVIEW

The PM7975 LASAR Optical Network Interface Card (NIC) is a Peripheral Component Interconnect (PCI) Bus Local ATM network interface card which contains the PM7375 Local Segmentation and Reassembly & Physical Layer device (LASAR-155) and an optical PMD to provide a local ATM network interface using SONET/SDH framing at 155.52 or 51.84 Mbit/s and ATM Adaptation Layer 5 (AAL5). The PCI bus interface is compliant with the PCI SIG Specification Rev. 2.0 and provides scatter/gather DMA of packets.

The LASAR-155 device implements SONET/SDH transmission convergence, ATM cell mapping, ATM Adaptation Layer, and PCI Bus memory management functions for a 155.52 or 51.84 Mbit/s ATM User Network Interface (UNI). The NIC is configured, monitored, and powered through a 5 Volt/32bit PCI connector. The PMD deploys a standard 9-pin single-mode or multi-mode optical transceiver module. An on-board oscillator provides a reference for the LASAR-155's integrated clock and data recovery unit on the receive side, and the clock synthesis unit on the transmit side.

2. FUNCTIONAL DESCRIPTION

2.1. Block Diagram



2.2. LASAR-155 (U2)

The LASAR-155 is a single-chip Peripheral Component Interface (PCI) Bus Local ATM Network Interface using SONET/SDH framing at 155.52 or 51.84 Mbit/s and ATM Adaptation Layer 5 (AAL-5). For a complete description of the LASAR-155, please refer to PMC-931127, LASAR-155 Longform Datasheet.

The NIC implements the following features of the LASAR:

- Implements the ATM Physical Layer according to the ATM Forum User Network Interface Specification and ITU-TS Recommendation I.432, and the ATM

Adaptation Layer Type 5 (AAL-5) for Broadband ISDN according to ITU-TS Recommendation I.363.

- Supports multimode or single mode optical modules or twisted pair wiring (UTP5) modules.
- Directly supports a 32-bit PCI compliant bus interface for configuration, monitoring and transfer of packet data, with an on-chip DMA controller with scatter/gather capabilities.
- Using the LASAR-155's on-chip 96 cell receive buffer to accommodate up to 270 µs of PCI Bus latency.
- Supports simultaneous segmentation and reassembly of 128 virtual circuits (VCs) in both transmit and receive directions.
- Provides leaky bucket peak cell rate enforcement using 8 programmable peak queues coupled with sub peak control on a per VC basis; provides sustainable cell rate enforcement using the programmable peak cell rate queues and per VC token bucket averaging; and provides aggregate peak cell rate enforcement.

2.3. Line Interface

The receive line interface consist of PECL outputs of the PMD transceiver module terminated and ac coupled into the RXD+/- inputs of the LASAR-155. To ensure that there is a clock in the absence of incoming signal, the signal detect (SD) output of the PMD transceiver is connected to the ALOS- input of the LASAR-155 while the ALOS+ input is ac coupled to ground. In normal operation (good incoming signal) the LASAR-155 recovers the clock from the incoming data. Under the loss of signal condition, the LASAR-155 will squelch the data on the receive data (RXD+/-) pins and its phase locked loop will switch to the reference clock (19.44 MHz) to keep the recovered clock in range. This technique guarantees that the LASAR-155 will generate a Loss Of Signal (LOS) indication when the PMD transceiver device loses incoming signal.

The transmit line interface consist of the LASAR-155's CMOS transmit outputs which are AC-coupled, attenuated, terminated, buffered via a PECL buffer (100EL16), and connected to the PECL inputs of the PMD transceiver module. The 100EL16 is used because the long trace length (high capacitance),which the TXD+/- CMOS outputs will otherwise have to drive, will affect the rise and fall time of TXD+/- outputs. As a result, the 100EL16 is placed near the LASAR-155 to provide buffering for the TXD+/- CMOS outputs and drive the 50 Ohm transmission lines to the PMD transceiver module's PECL inputs.

The PMD transceiver module can be a single-mode or multi-mode optical transceiver, or a UTP5 transceiver of the same footprint.

2.4. Oscillator (Y1)

The 19.44 MHz TTL oscillator provides a reference to the clock and data recovery circuitry of the LASAR-155 on the receive side, and clock synthesis circuitry of the LASAR-155 on the transmit side via a 74FCT541 8-bit buffer/line driver. The outputs of the buffer are series terminated and connected to the RRCLK- and TRCLK- inputs of the LASAR-155, while its RRCLK+ and TRCLK+ inputs are connected to their respective ground.

2.5. PCI Connector and LED

The PCI connector is configured as a 5 Volt/32-bit, PCI SIG Rev. 2.0 compliant expansion daughter card edge connector.

The on board LED is driven directly by the receive alarm (RALM) output of the LASAR-155. The LED is on when RALM output of the is high (under loss of signal, line AIS, path AIS, loss of frame, loss of pointer, or loss of cell delineation state), and off when RALM output is low. A low power LED should be deployed if a buffer is not used.

3. BOARD LAYOUT DESCRIPTION

The NIC has four layers: (from the top down) layer 1 and 4 for signals, layer 2 for ground plane, and layer 3 for power planes. The dimension of the NIC conforms to the 5V PCI Raw Short Card, with custom mounting hole locations. the NIC layout follows high speed signal layout guide lines as well as the PCI Rev. 2.0 Spec. layout restrictions. **The PCI SIG specification has stringent and detailed rules on decoupling, power consumption, trace length limits, routing, trace impedance, as well as signal loading. Therefore, it is essential to consult the latest PCI specification before proceeding with new designs and layouts**.

3.1. Power and Ground Distribution

Discrete transmit, receive, and digital power planes can be connected together using solder bridges. The power coming off the PCI bus 5 Volt power supply pins is also isolated by solder bridges or Schottky diodes from the rest of the board. In addition, the transmit and receive section can also be powered through their respective voltage regulators which draw their power from the +12 Volt supply pin on the PCI bus.

One continuous ground plane is used with cuts to isolate the transmit and receive analog grounds from each other as well as from the digital grounds.

The oscillator, the 74FCT541 buffer, the transmit analog sections of the PMD transceiver and the LASAR-155 share the same transmit analog power and ground planes. The receive sections of the PMD transceiver and the LASAR-155 share the same receive analog power and ground planes.

All of LASAR-155's analog power supply pins use ferrite beads to filter out Vcc noise. A 0.1 uF bypassing capacitor is placed near each ferrite bead supply its respective analog Vcc pin, while a 0.01 uF decoupling capacitor is placed near each analog or digital Vcc pin. In addition, ferrite beads are used on transmit and receive analog ground pins of the LASAR-155 to reduce ground noise.

The solder bridge are shown below:

Solder Bridge	Purpose	Standard Configuration
SB1, SB11, SB10, & SB9	Vcc from PCI connector to board digital Vcc plane	open
SB15	connects output of regulator U5 to the receive analog power plane	short

SB5 & SB6	connect receive analog power plane to digital power plane	open
SB14	connects output of regulator U4 to the transmit analog power plane	short
SB2 & SB4	connect transmit analog power plane to digital power plane	open
SB3 & SB7	connect PMD module (optical or utp5) mounting pins to chassis ground	short
SB12 & SB8	connect PMD module (optical or utp5) mounting pins to board ground	open

With the standard configuration, the receive and transmit analog planes are powered via regulators U5 and U4 separately. The mounting posts of the PMD transceiver is connected to the chassis ground via a chassis ground island placed under the PMD transceiver device on the ground plane and the solder bridges SB3 and SB7.

3.2. Component Placement

- The LASAR-155 device is placed such that all the PCI interface traces are within the specified length limits of the PCI Rev. 2.0 Spec., while being as close to the PMD transceiver as possible.
- The PECL buffer (U3) is placed close to the LASAR-155 TXD+/- outputs to reduce the transmission line lengths these two CMOS outputs have to drive.
- The 74FCT541 buffer is placed between the transmit and receive analog sections of the LASAR-155 so that each of its two outputs can be routed to the transmit or receive reference clock inputs without crossing any discontinuity on the power or ground planes which serve as image planes for return currents as well as to control the impedance of the transmission lines.
- The oscillator (Y1) is placed near the 74FCT541 inputs on the transmit analog section.
- LASAR-155 loop filter components are placed near the chip on the same side.
- All termination resistors are placed as close to the inputs as possible on the same side.

- All pull down resistors are placed near the LASAR-155 output pins.

3.3. Routing and Termination

- All high speed traces are routed over continuous image planes (power or ground planes)
- All traces carrying transmit and receive data are transmission lines with 50 Ohm controlled impedance. These traces should be routed on the same side and kept as short as possible.
- All differential signals are of the same length and routed close to each other.
- Reference clock signals from the 74FCT541 are 75 Ohm transmission lines with series termination.
- Two termination schemes are provided for the PECL signals to and from the PMD transceiver. One scheme is the 50 Ohm Thevenin equivalent termination (81 Ohm to Vcc in series with 130 Ohm to ground), and the other scheme uses 330 Ohm pull downs and 100 Ohm termination.
- All PCI signal traces have an impedance of 75 Ohms +/- 10%

APPENDIX A: BILL OF MATERIAL

Item	Refdes	Total	Description
1	C15	1	Capacitor, 100uF, electrolytic, Radial leads, 0.196" spacing, 25 Volts rating preferred, 16 Volts is the next preferred rating if 25 Volt caps are not available.
2.	C28 C66	2	Capacitor, 47uF, electrolytic, Radial leads, 0.196" spacing, 25 Volts rating preferred, 16 Volts is the next preferred rating if 25 Volt caps are not available.
3	P1	1	Refers to the PCB itself, no parts required.
4	Y1	1	19.44 MHz, 20 ppm, DIP Osc, 0.26" case, 14 pins DIP, TTL levels, Connor Winfield, S54R8-19.44MHz, or equivalent
5	L1 L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L13 L14 L15 L16 L17 L18 L19 L20	19	Ferrite Beads, surface mount, 0.2", Fair_rite #2743019446.
6	D2 D4	2	3.0 A max average rect. current 20 Volts max peak reverse voltage approximately 0.475 peak max. forward voltage DO-201AD package
7	U1	1	Fiber Optics transceiver, 9 Pins, HP HFBR5205
8	D1	1	Lower power LED, red, 0.1" spacing, 1 - 5 mA operating current
9	U2	1	PM7375, LASAR-155, 0.50 mm pitch, 208 pin PQFP, PMC-Sierra
10	J7 J9	2	pcb mount SMA connectors

11	C8 C17 C20 C22 C27 C33 C39 C42 C44 C47 C50 C53 C55 C58 C61 C62 C63 C67 C68 C71 C74 C76 C78 C79 C80 C81 C82	27	Capacitors, 0.1 uF MultiLayer Ceramic chip capacitor, 50V, Size 1206, Surface mount

12	C2 C3 C5 C10 C11 C12 C13 C14 C16 C18 C19 C23 C24 C25 C26 C29 C30 C31 C32 C34 C35 C36 C37 C40 C41 C43 C45 C46 C48 C51 C52 C56 C57 C59 C60 C64 C65 C69 C70 C72 C75 C77	42	Capacitors, 0.01 uF MultiLayer Ceramic chip capacitor, 50V, Size 805, Surface mount
13	C7 C21 C38	3	Capacitors, 47 pF MultiLayer Ceramic chip capacitor, 50V, Size 805, Surface mount

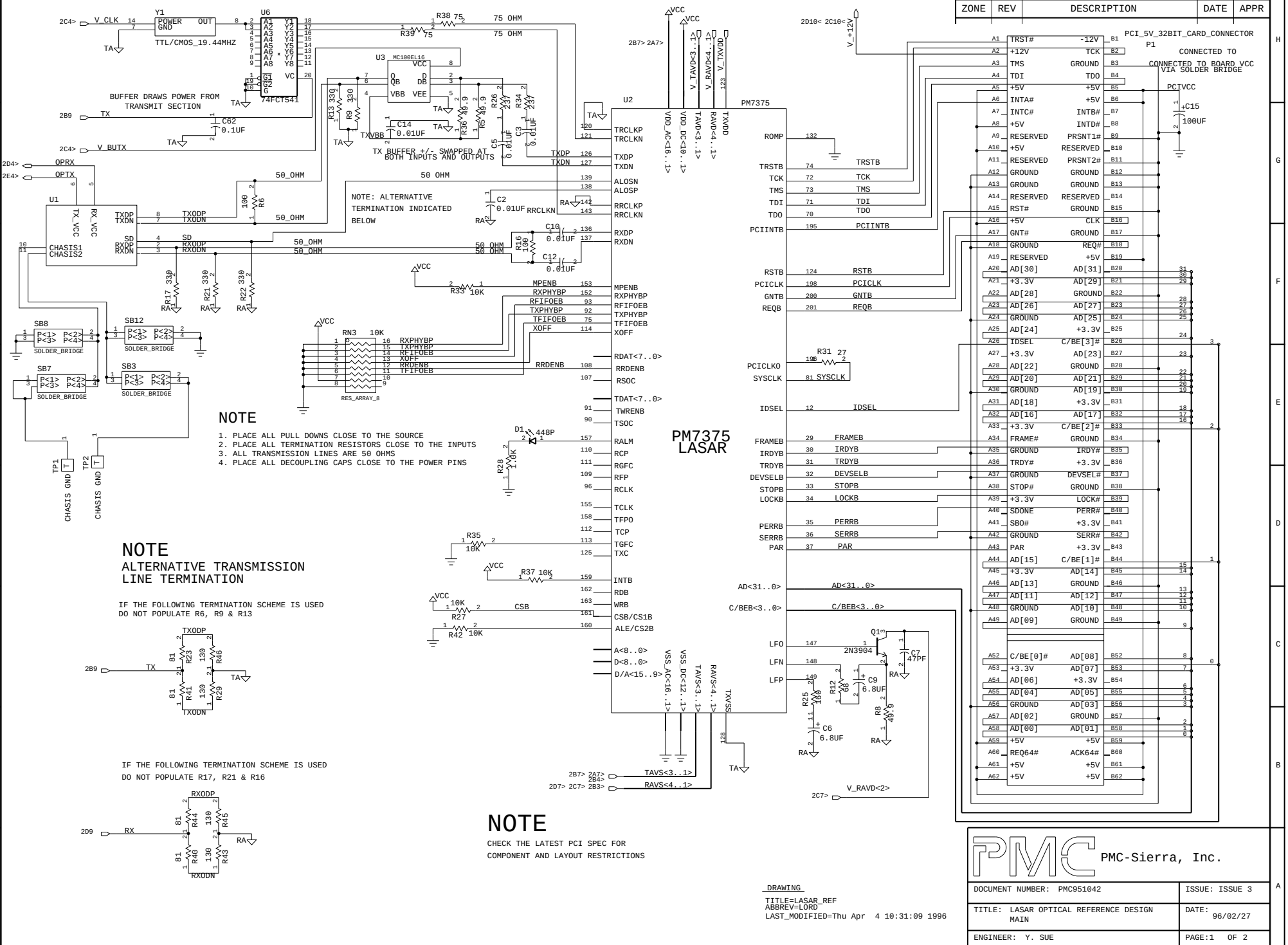
14	C1 C4	2	value to be determined
15	R31	1	Resistors, 27 ohm 1/10 watt MF 5%, Size 805, Surface mount
16	R6 R16	2	Resistors, 100 ohm 1/10 watt MF 1%, Size 805, Surface mount
17	R27 R33 R35 R37 R42	5	Resistors, 10K ohm 1/10 watt MF 5%, Size 805, Surface mount
18	R25	1	Resistor, 160 ohm 1/10 watt MF 1%, Size 805, Surface mount
19	R26 R34	2	Resistors, 237 ohm 1/10 watt MF 1%, Size 805, Surface mount
20	R28	1	Resistors, value dependent on the LED used, 1/10 watt MF 5%, Size 805, Surface mount
21	R9 R13 R17 R21 R22	5	Resistors, 330 ohm 1/10 watt MF 1%, Size 805, Surface mount
22	R5 R8 R36	3	Resistor, 49.9 ohm 1/10 watt MF 1%, Size 805, Surface mount
23	R12	1	Resistor, 68.1 ohm 1/10 watt MF 1%, Size 805, Surface mount
24	R38 R39	2	Resistors, 75.0 ohm 1/10 watt MF 1%, Size 805, Surface mount
25	R23 R40 R41 R44	4	Resistor, 81 ohm 1/10 watt MF 1%, Size 805, Surface mount
26	R29 R43 R45 R46	4	Resistors, 130 ohm 1/10 watt MF 1%, Size 805, Surface mount
27	C49 C54 C73 C83 C84	5	Capacitors Pol. 10 uF, Panasonic TEH series, Resin molded chips tantalum electrolytic capacitor, EIA Size C, surface mount, 25 Volts or 16 Volts. 25 Volt rating preferred; 16 Volt is the next preferred rating

28	C6 C9	2	Capacitors Pol. 6.8 uF, Panasonic TEH series, Resin molded chips tantalum electrolytic capacitor, EIA Size C, Surface mount, 25 Volt rating preferred; 16 Volt is the next preferred rating
29	RN3	1	Chip-resistor array, 10K ohm x 8, SOIC package, 8 resistors in 1 package
30	U6	1	non-inverting 8-bit buffers/line drivers, Cypress, CY74FCT541, 20 pin SOIC, or equivalent
31	U3	1	PECL buffer, MC100EL16 or equivalent, 8 pin SOIC
32	U4 U5	2	7805, Positive 5 Volt, 1.5 AMP voltage regulator, TO-220 package
33	Q1	1	Discrete Transistor, NPN, SOT23 package, surface mount
34	SB1 SB2 SB3 SB4 SB5 SB6 SB7 SB8 SB9 SB10 SB11 SB12 SB14 SB15	14	solder bridges
35	TP1 TP2 TP6 TP8 TP10 TP12	6	test points

APPENDIX B: SCHEMATICS

NOTE: PLACE ALL THE TERMINAL RESISTOR OR NETWORK AS CLOSE TO SIGNAL END PINS AS POSSIBLE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



NOTE

1. PLACE ALL PULL DOWNS CLOSE TO THE SOURCE
2. PLACE ALL TERMINATION RESISTORS CLOSE TO THE INPUTS
3. ALL TRANSMISSION LINES ARE 50 OHMS
4. PLACE ALL DECOUPLING CAPS CLOSE TO THE POWER PINS

NOTE

ALTERNATIVE TRANSMISSION LINE TERMINATION

IF THE FOLLOWING TERMINATION SCHEME IS USED
DO NOT POPULATE R6, R9 & R13

IF THE FOLLOWING TERMINATION SCHEME IS USED
DO NOT POPULATE R17, R21 & R16

NOTE

CHECK THE LATEST PCI SPEC FOR
COMPONENT AND LAYOUT RESTRICTIONS

DRAWING

TITLE=LASAR_REF
ABBREV=LORD
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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC951042	ISSUE: ISSUE 3
TITLE: LASAR OPTICAL REFERENCE DESIGN MAIN	DATE: 96/02/27
ENGINEER: Y. SUE	PAGE:1 OF 2

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

NOTE

FOR TESTING PURPOSE ONLY

LASAR SIDE — PCI CONNECTOR SIDE

VCC — 2H4> 1H1 — PCIVCC

SB1, SB11, SB10, SB9 — P<1> P<2> P<3> P<4> — SOLDER_BRIDGE

LASAR SIDE — PCI CONNECTOR SIDE

VCC — 2H6> 1H1 — PCIVCC

D2 1N5820

D4 1N5820

SOLDER BRIDGE ADDED TO ALLOW TX AND RX TO BE CONNECTED TO VCC AS AN OPTION

2D9 RX — SB5 — VCC

2D9 RX — SB6 — VCC

2B9 TX — SB4 — VCC

2B9 TX — SB2 — VCC

DECOUPLING FOR VDD_AC

VCC — C24 0.01UF, C30 0.01UF, C35 0.01UF, C41 0.01UF, C46 0.01UF, C52 0.01UF, C59 0.01UF, C64 0.01UF, C69 0.01UF, C72 0.01UF, C31 0.01UF, C36 0.01UF, C75 0.01UF, C70 0.01UF, C56 0.01UF, C16 0.01UF

DECOUPLING FOR VDD_DC

VCC — C19 0.01UF, C13 0.01UF, C57 0.01UF, C51 0.01UF, C45 0.01UF, C40 0.01UF, C34 0.01UF, C29 0.01UF, C23 0.01UF, C18 0.01UF, +C84 10UF, +C83 10UF, +C73 10UF, C68 0.1UF, C80 0.1UF, C63 0.1UF

DECOUPLING FOR OPTICS RECEIVE VCC

2B9 TX — L3 FB — OPTX — 1G10> — C20 0.1UF, C25 0.01UF — TA

DECOUPLING FOR OPTICS TRANSMIT VCC

2D9 RX — L2 FB — OPRX — 1G10> — C8 0.1UF, C11 0.01UF — RA

FOR TEST PURPOSES ONLY

J7, J9 — SMA — TP10 GND, TP6 GND, TP12 SIG, TP8 SIG — C1 TBD, C4 TBD

SB15 — P<1> P<2> P<3> P<4> — SOLDER_BRIDGE — C76 0.1UF, C71 0.1UF — RA

1H4> V_+12V — U5 7805 (INPUT, OUTPUT, GND) — C66 47UF, C54 10UF, C47 0.1UF

RX

DECOUPLING FOR RAVD

L8 FB — V_RAVD<4> — 1H5< — C17 0.1UF, C48 0.01UF — RAVS<4> — 2B3> 1B6<

L7 FB — V_RAVD<3> — 1H5< — C82 0.1UF, C43 0.01UF — RAVS<3> — 2B3> 1B6<

L6 FB — V_RAVD<2> — 1B4< 1H5< — C81 0.1UF, C38 47PF — RAVS<2> — 2B3> 1B6<

L4 FB — V_RAVD<1> — 1H5< — C79 0.1UF, C32 0.01UF — RAVS<1> — 2B3> 1B6<

1H4> V_+12V — C58 0.1UF, C53 0.1UF, C50 0.1UF, C42 0.1UF, C22 0.1UF

SB14 — P<1> P<2> P<3> P<4> — SOLDER_BRIDGE

1H4> V_+12V — U4 7805 (INPUT, OUTPUT, GND) — C28 47UF, C49 10UF, C33 0.1UF

DECOUPLING FOR TAVD

TX

L16 FB — V_TAVD<3> — 1H5< — C61 0.1UF, C26 0.01UF — TAVS<3> — 2B4> 1B6<

L15 FB — V_TAVD<2> — 1H5< — C55 0.1UF, C21 47PF — TAVS<2> — 2B4> 1B6<

L14 FB — V_TAVD<1> — 1H5< — C67 0.1UF, C65 0.01UF — TAVS<1> — 2B4> 1B6<

L11 FB — V_TXVDD — 1H5< — C39 0.1UF, C60 0.01UF

C74 0.1UF, C78 0.1UF — TA

DECOUPLING FOR TXVDD

2B9 TX — DECOUPLING FOR V_CLK

L5 FB — V_CLK — 1H10< — C44 0.1UF, C37 0.01UF — TA

DECOUPLING FOR V_BUTX

L9 FB — V_BUTX — 1G10< — C27 0.1UF, C77 0.01UF — TA

L20 FB, L18 FB, L13 FB — TAVS<3..1> — 2A7> 2B7> 1B6< — TA

L19 FB — RAVS<4..1> — 2C7> 2D7> 1B6<

L17 FB, L10 FB, L1 FB — RA

ONE SOLID PLANE WITH CUTS

TA RA

DRAWING

TITLE=LASAR_REF

ABBREV=LORD

LAST_MODIFIED=Mon Apr 1 09:36:41 1996

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC951042	ISSUE: ISSUE 3
TITLE: LASAR OPTICAL REFERENCE DESIGN POWER SUPPLY & DECOUPLING	DATE: 96/02/27
ENGINEER: Y. SUE	PAGE:2 OF 2

APPENDIX C: LAYOUT

Board Material Details

	Material	Layer Type	Etch Name	Film type	Thickness	Dielectric Constant
#	COPPER	CONDUCTOR	TOP	POSITIVE	2.88 mil	-----
	FR-4	DIELECTRIC	-----	-----	10 mil	4.2
	COPPER	CONDUCTOR	GND_PLANE	POSITIVE	2.88 mil	-----
	FR-4	DIELECTRIC	-----	-----	30.5 mil	4.2
	COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	2.88 mil	-----
	FR-4	DIELECTRIC	-----	-----	10 mil	4.2
#	COPPER	CONDUCTOR	BOTTOM	POSITIVE	2.88 mil	-----

Note: 50 ohm controlled impedence traces with trace width of 17 mil are on Top and Bottom layers.

Notes:

1. Copper thickness is 2 oz. on all layers.
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are specified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil mimimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white based ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in./in. per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED
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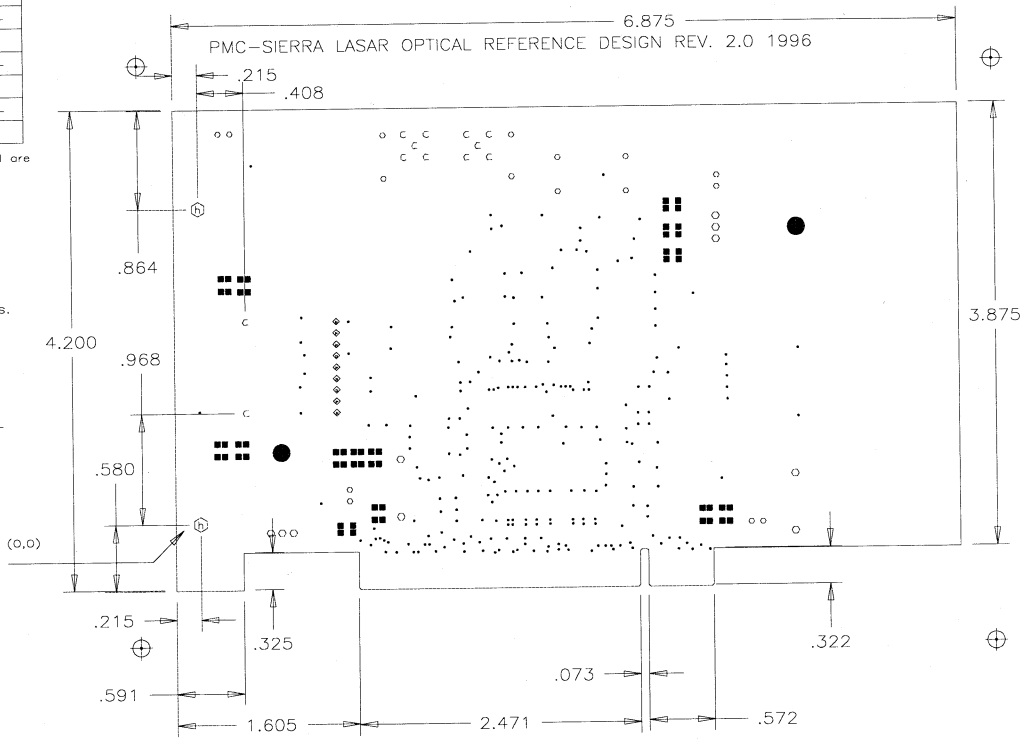
2.0	MECHANICAL DRAWING	96	02	27	



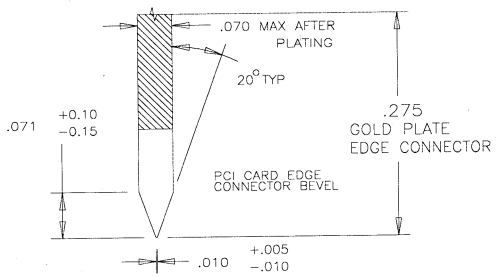
ARTWORK FILM

TOP LAYER
GROUND PLANE
VCC PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
MECH. DRAWING

Hole Chart

FIGURE	HOLESIZE	QTY
.	15.000-P	252
■	32.000-P	56
o	36.000-P	16
◈	42.000-P	9
O	55.000-P	10
c	79.000-P	12
ⓗ	125.000-P	2
●	150.000-N	2

Note: P = Plated
N = Non-Plated



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
2 PL DECIMALS +/- .03
3 PL DECIMALS +/- .005
ANGLES
FRACTIONS

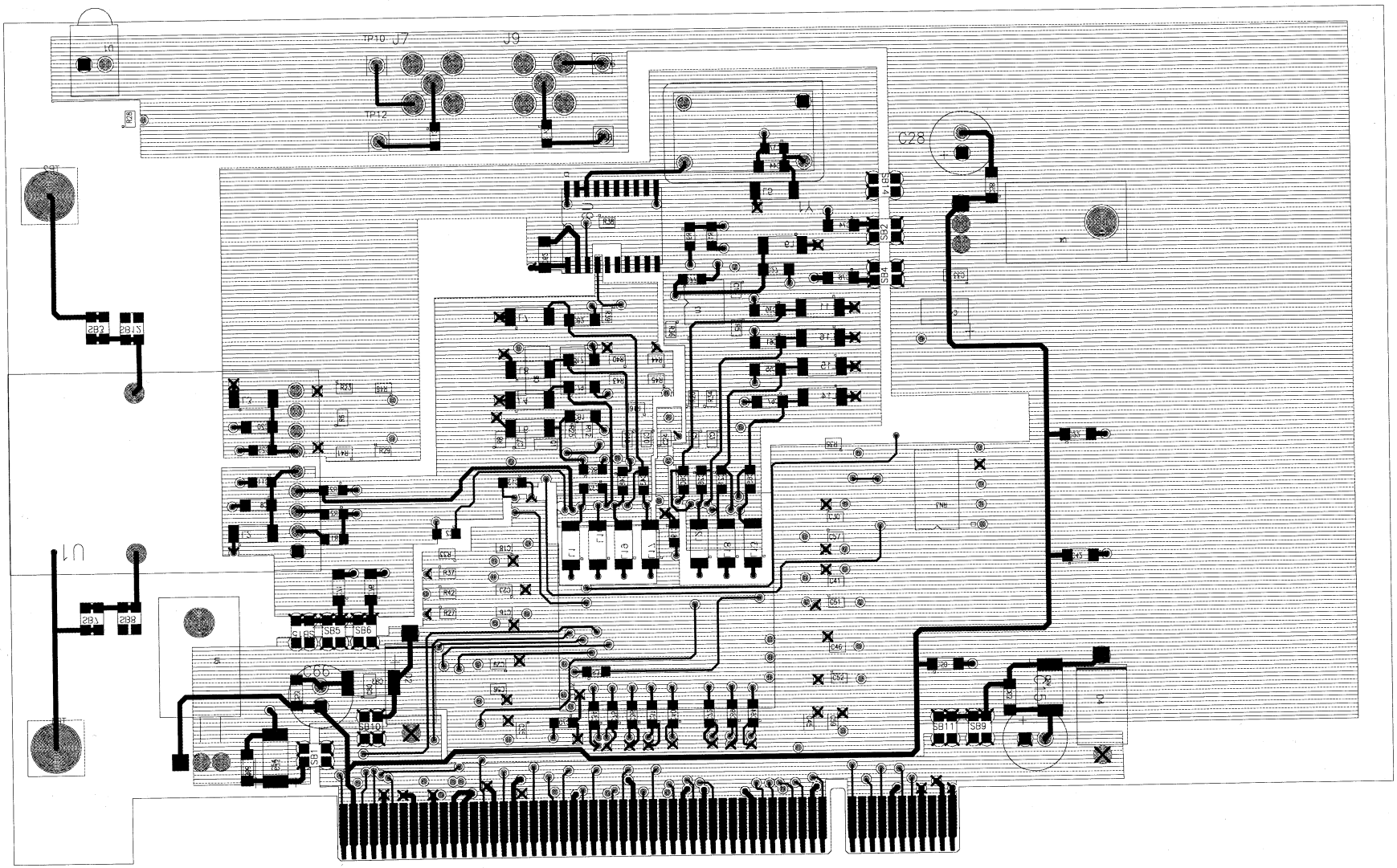
		DATE YY	MM	DD
DRAWN	Y SUE	96	02	27
CHECKED				
ENGINEER				
APPROVED				

PMC-Sierra, Inc.
8501 Commerce Court, Burnaby B.C.
Canada, V5A 4A3
Tel: 604 668 7300 Fax: 604 668 7301

SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET 1 OF 1

BOTTOM_LAYER

PMC-SIERRA LASAR OPTICAL REFERENCE DESIGN REV. 2.0 1996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J9
TP12
C28
U1
C66
SB1
SB2
SB3
SB4
SB5
SB6
SB7
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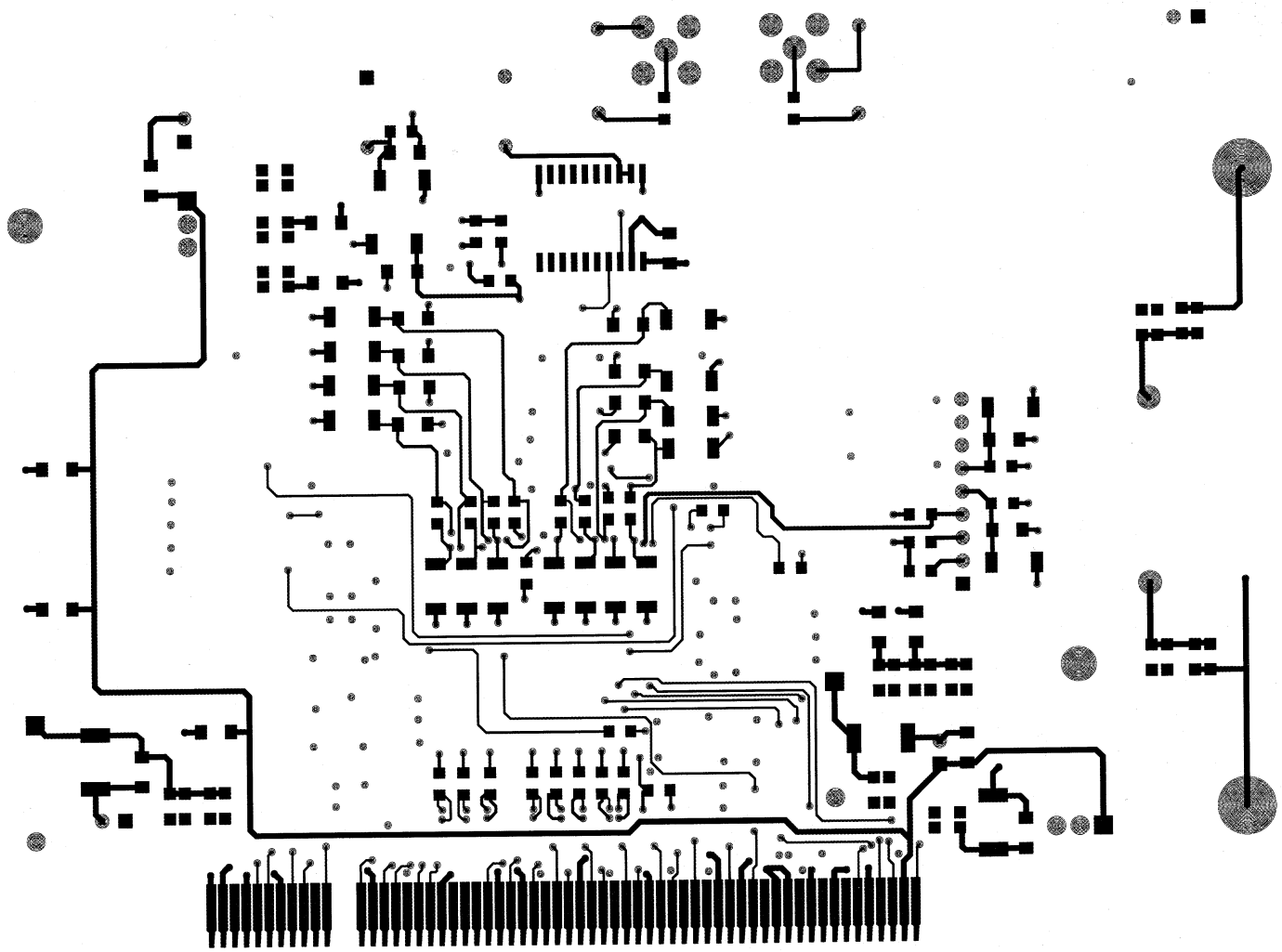
SB14
SB15
SB16

BOTTOM_LAYER



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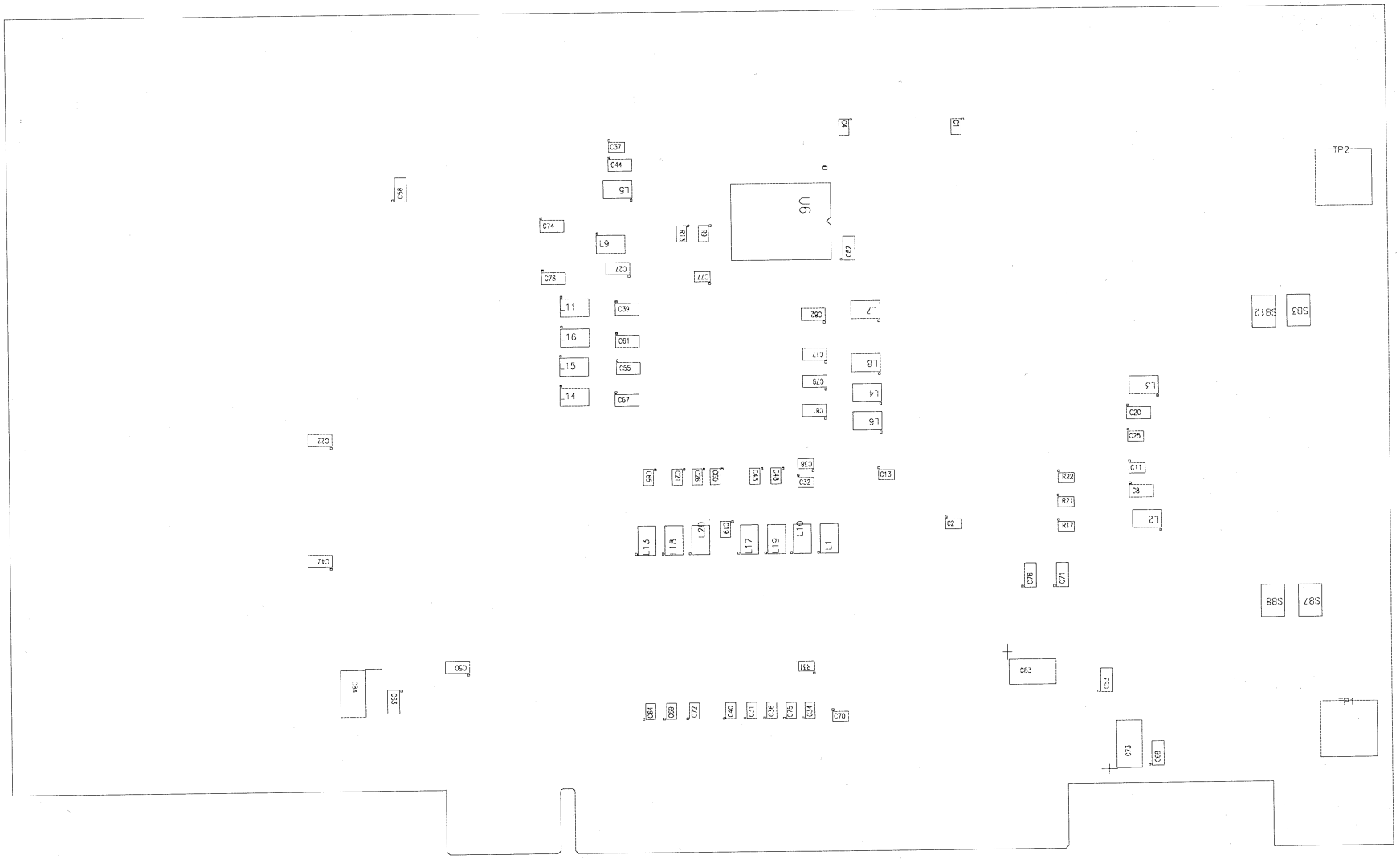
RES_DES BOTTOM

PMC-SIERRA LASAR OPTICAL REFERENCE DESIGN REV. 2.0 1996

RES_DES BOTTOM



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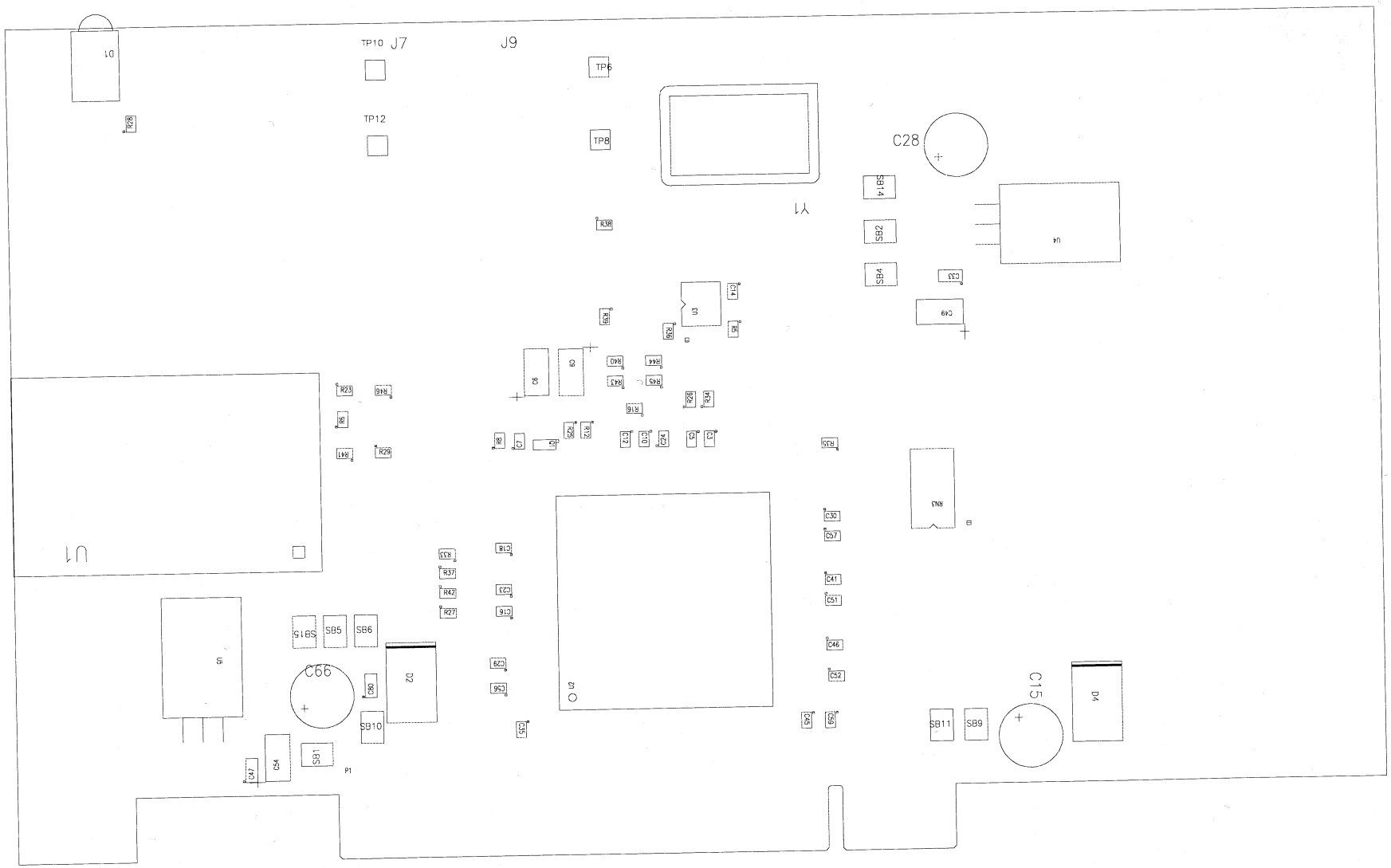

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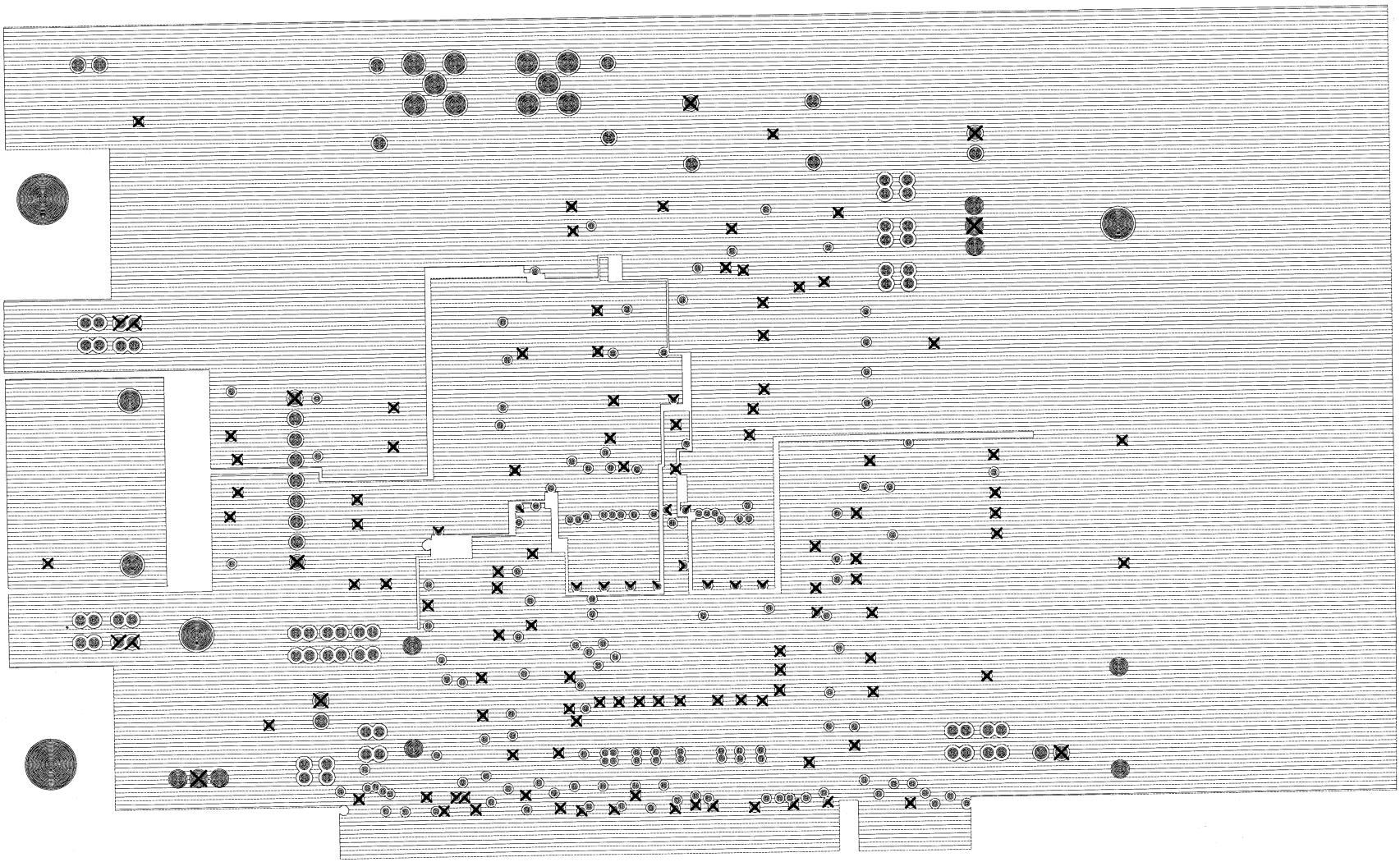
GND_PLANE



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SOLDER_MASK BOTTOM

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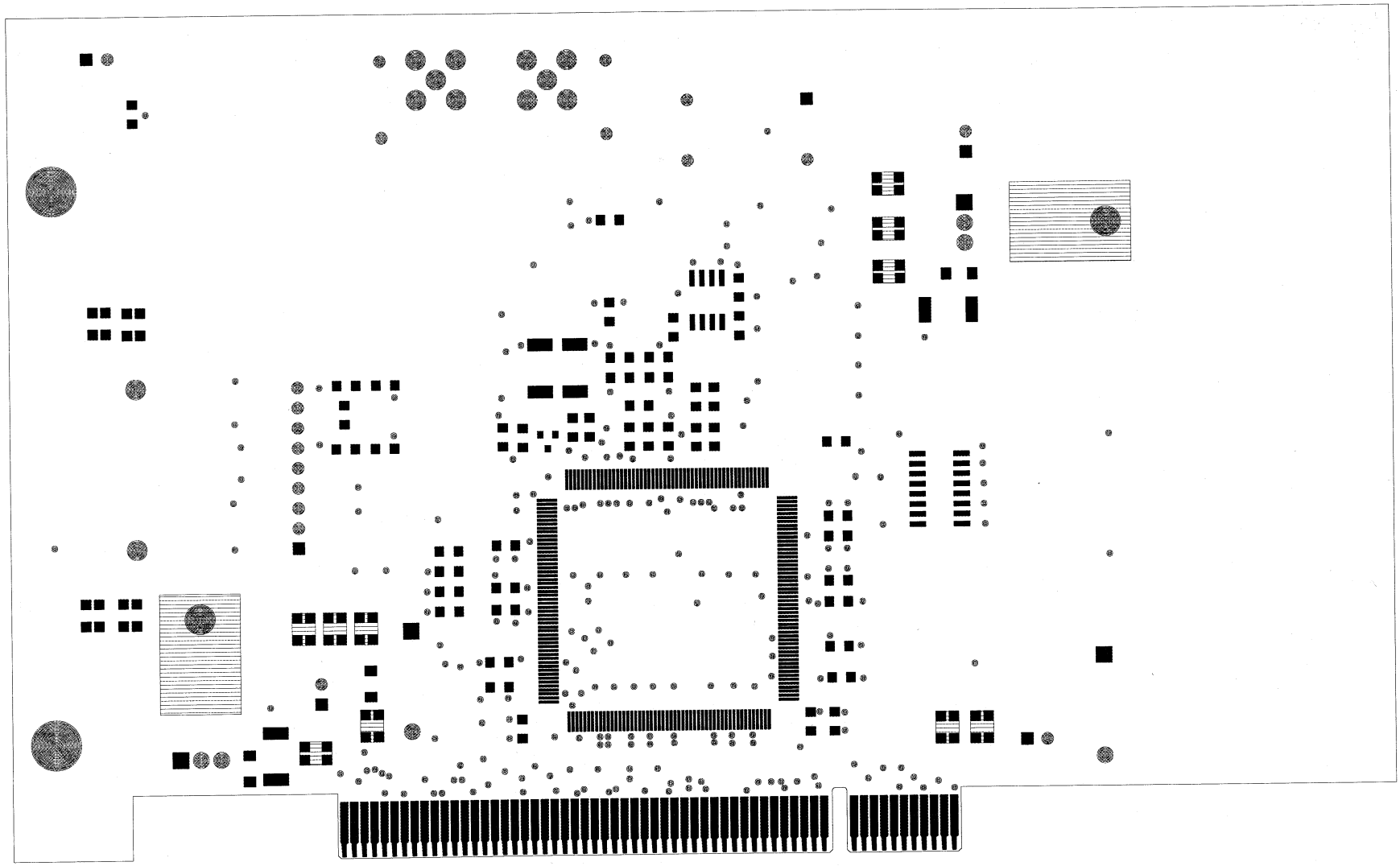
SOLDER_MASK TOP



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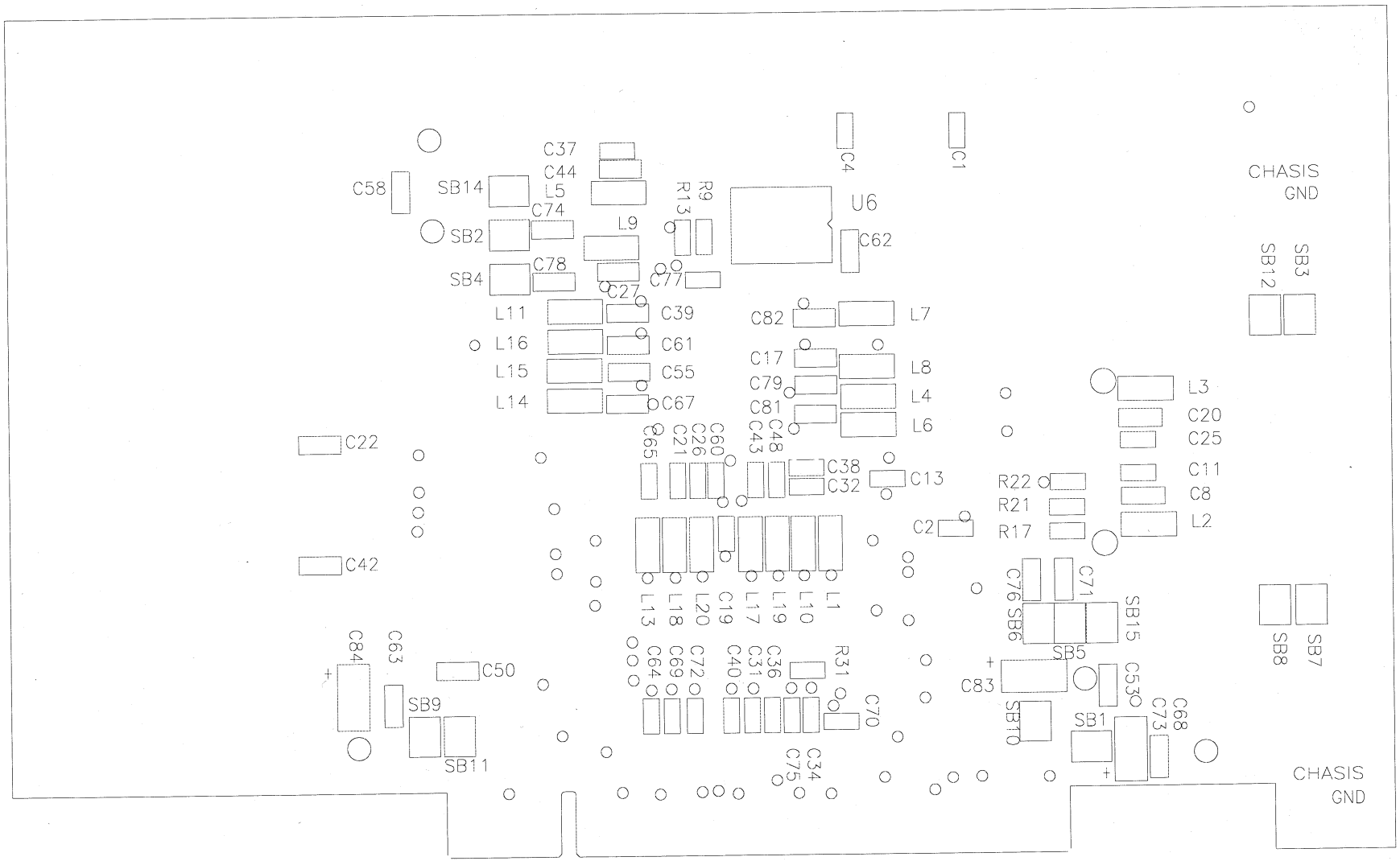
SILK SCREEN BOTTOM

PMC-SIERRA LASAR OPTICAL REFERENCE DESIGN REV. 2.0 1996

SILLK SCREEN BOTTOM



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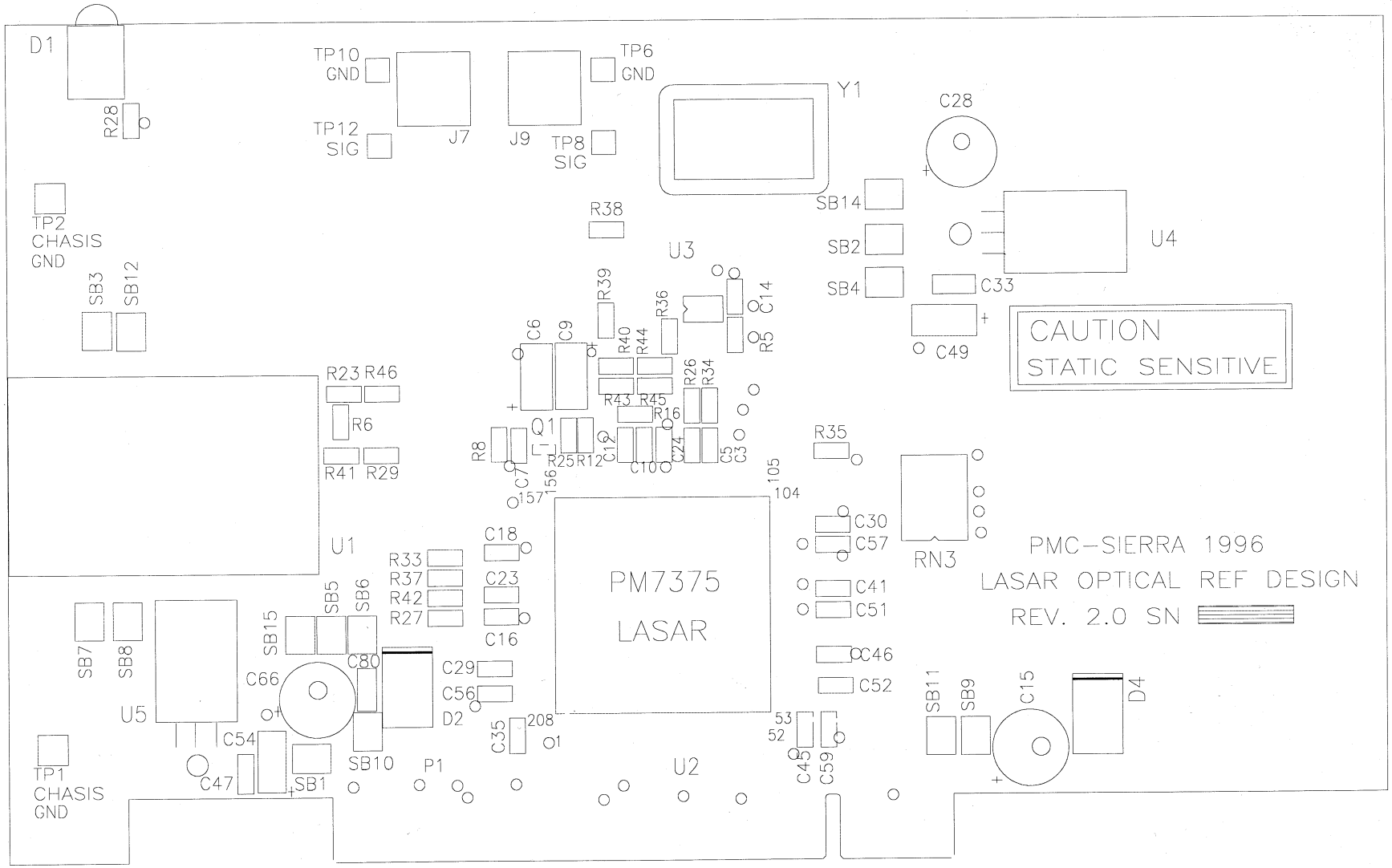

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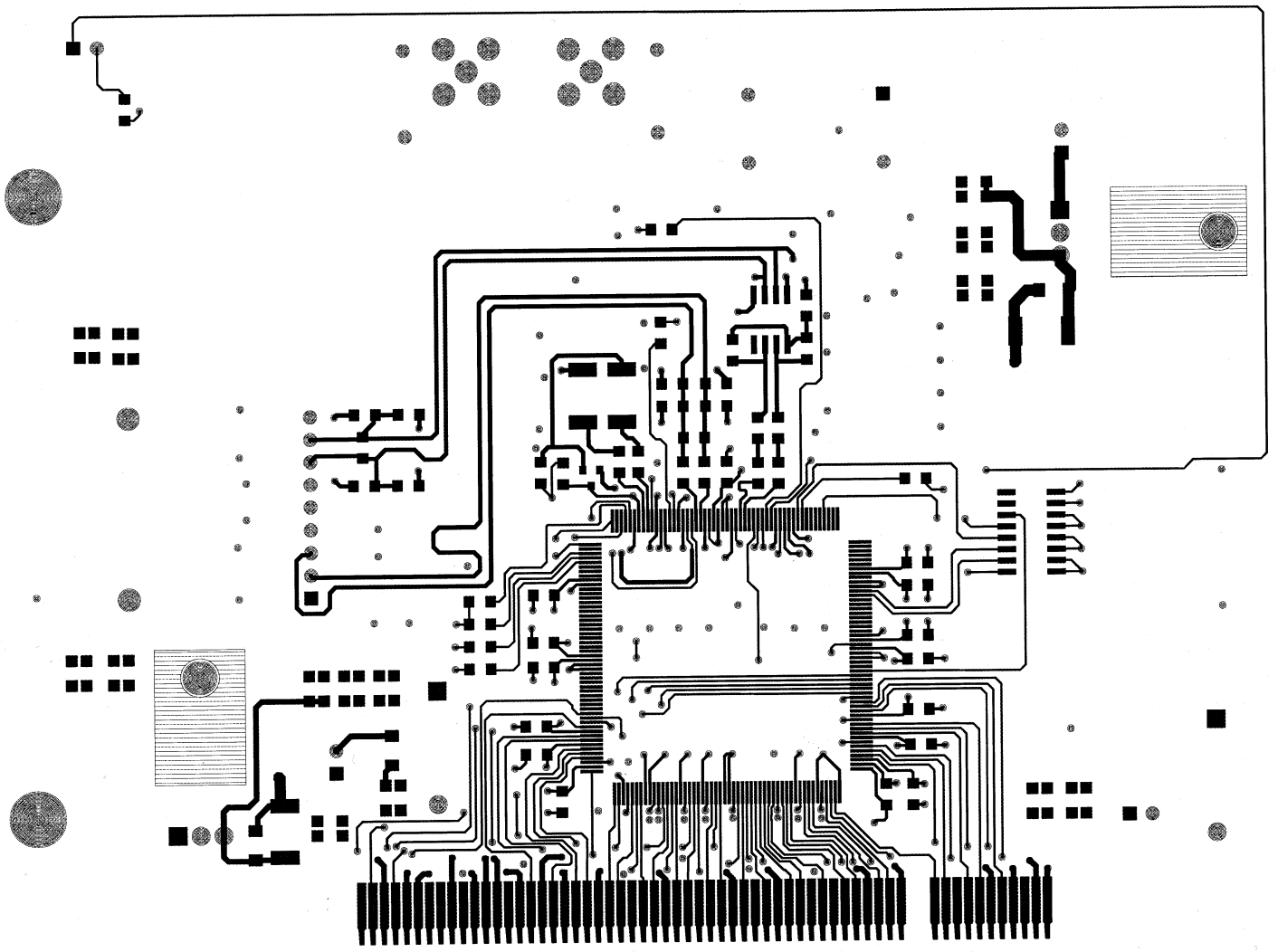
TOP LAYER



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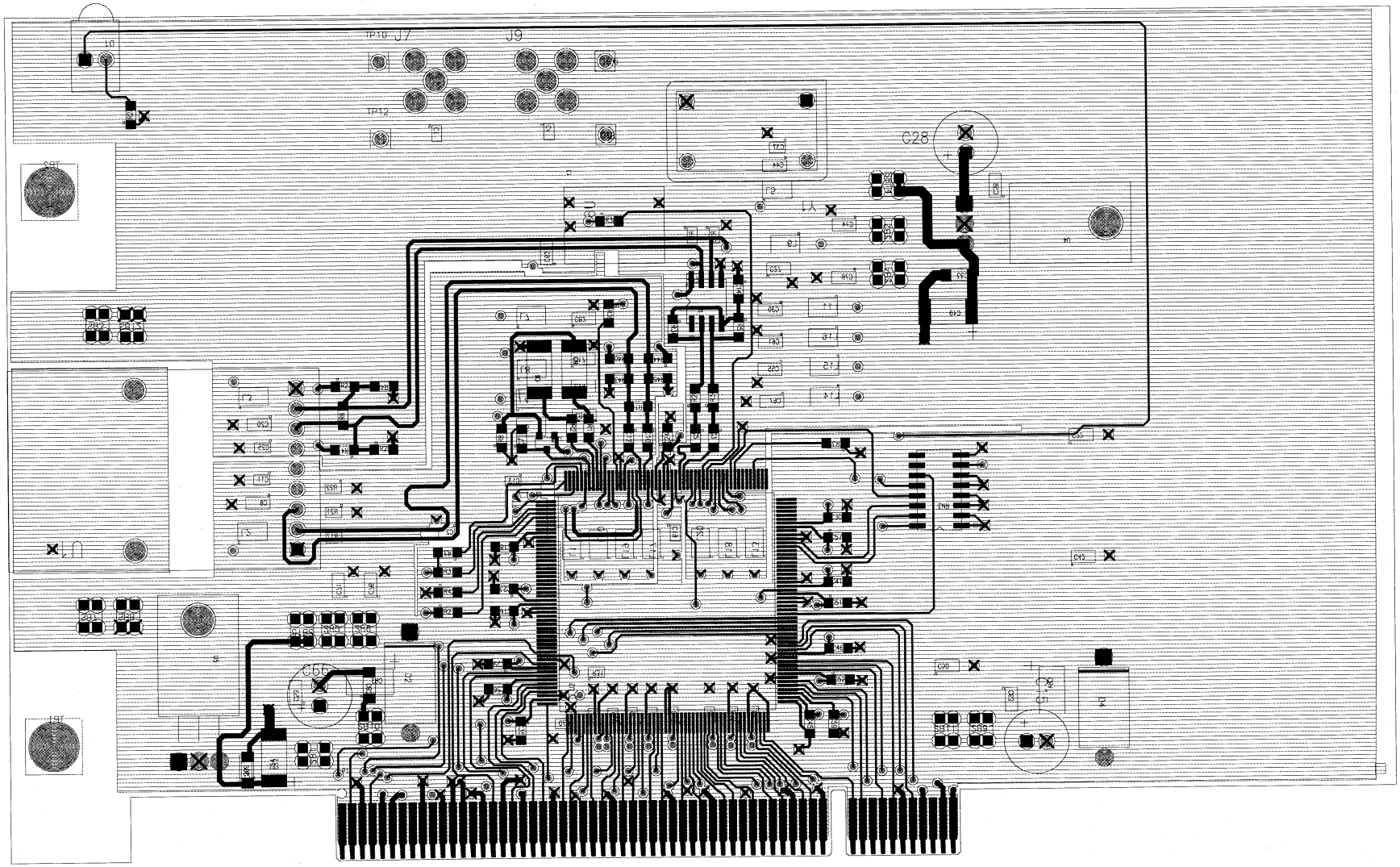

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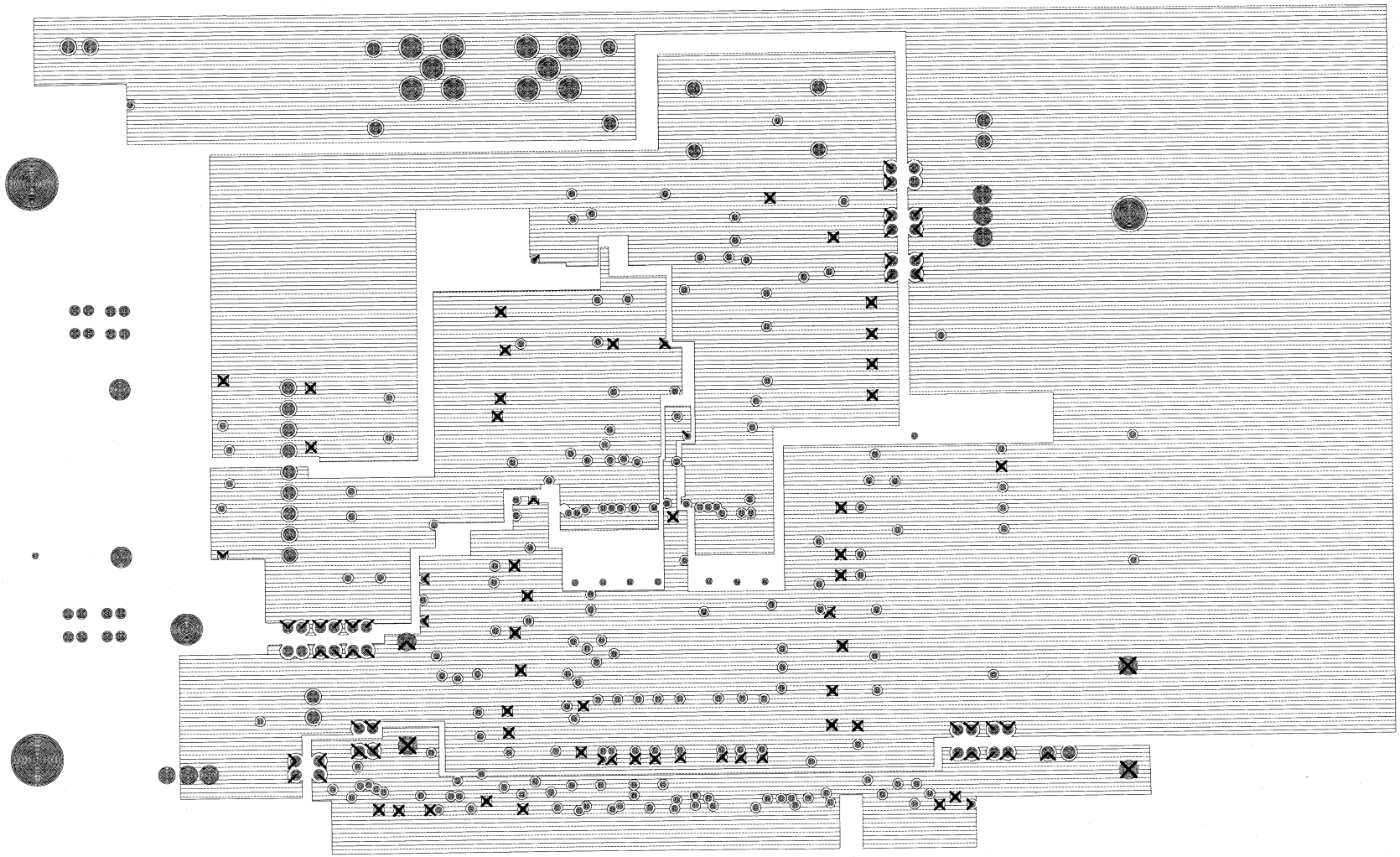
VCC_PLANE



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NOTES

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