PM8313

D3MX

INTERFACING THE D3MX TO THE SSI® 78P7200 DS-3 LIU

Preliminary Information

Issue 1: September 1995

OVERVIEW

The Silicon Systems® SSI78P7200 is a DS-3 (44.736Mbps) line interface unit commonly used with PMC-Sierra's PM8313 D3MX M13 Multiplexer device. The connections are straight-forward; however, some care has to be taken to compensate for differences in switching voltage levels between the two devices.

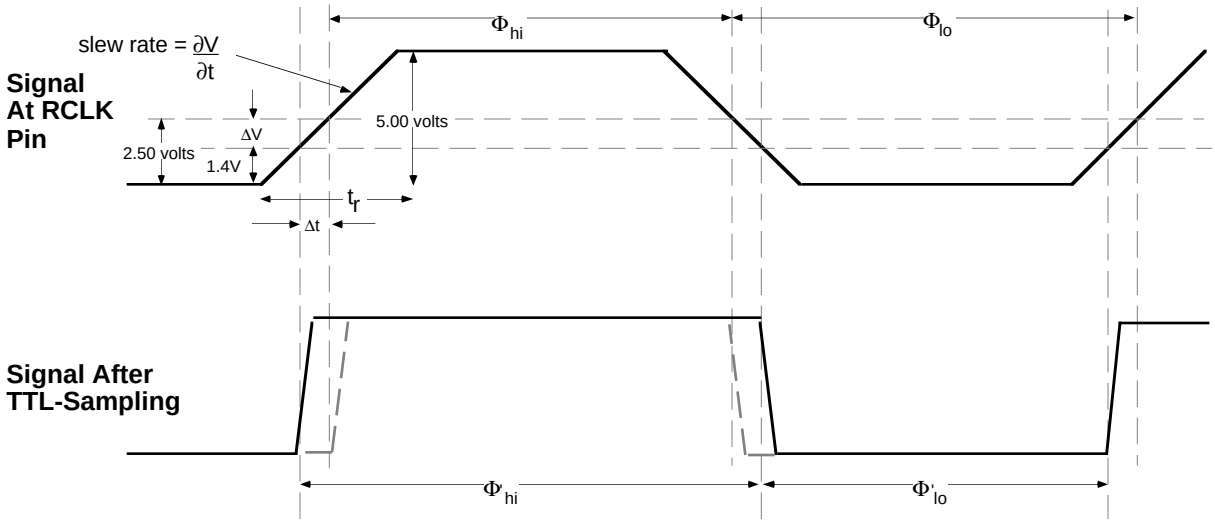
This design note details PMC-Sierra's recommendations for interfacing these two devices.

INTERFACE CONSIDERATIONS

The PM8313 D3MX's inputs are all TTL-compatible — they nominally switch at 1.4V, due to the sizing of the transistors in the input circuitry. TTL-compatibility allows direct connection to signals with a TTL voltage swing (0.8 to 2.0V). These inputs are also compatible with signals with a CMOS voltage swing (0.5 to 4.5V) *provided the rise and fall times of that signal are fast*. If the rise and fall times of the CMOS signal are slow, the difference in the CMOS and TTL switching points will cause duty-cycle distortion, as shown in Figure 1.

The SSI78P7200's outputs are CMOS. However, their drive capability (on the current version of the device) is low, resulting in slow transition times. Therefore, significant duty-cycle distortion, such as that shown in Figure1, occurs when the PM8313 D3MX inputs are connected to the SSI78P7200's outputs.

Figure 1. CMOS to TTL Duty-Cycle Distortion



In Figure 1, ΔV is the difference between the CMOS and TTL nominal switching voltage levels; Δt is the time difference between the CMOS and TTL nominal

switching points as located on a signal edge with a given slew rate. Note that symmetrical rise and fall times are assumed.

From Figure 1, and using information from the SSI78P7200 datasheet, the maximum duty-cycle distortion can be calculated:

$$\%\text{distortion}_{max} = \frac{2 \times \Delta t}{\text{bit\_period}} \times 100\%$$

$$= \frac{2 \times (\text{CMOS\_level - TTL\_level})}{\text{slew\_rate}_{min} \times \text{bit\_period}} \text{x}100\%$$

$$= \frac{2 \times (2.5\text{V} - 1.4\text{V})}{\left(\frac{4.0\text{V} - 1.0\text{V}}{6\text{ns}}\right) \times 22.4\text{ns}} \times 100\%$$

$$\%\text{distortion}_{max} = 19.6\%$$

Note: The minimum slew rate is calculated from the guaranteed output levels and the maximum Recovered Clock Transition Time specified in the SSI78P7200 datasheet.

As can be seen from the above calculations, the duty-cycle distortion can be quite large. If the D3MX is put in line loopback (using the LLBE bit in register 04H), the internal representation of RCLK is fed through to the TCLK output. In that case, TCLK will not meet the duty cycle requirements of the SSI78P7200's inputs — causing bit errors and line code violations in the transmitted DS-3 stream.

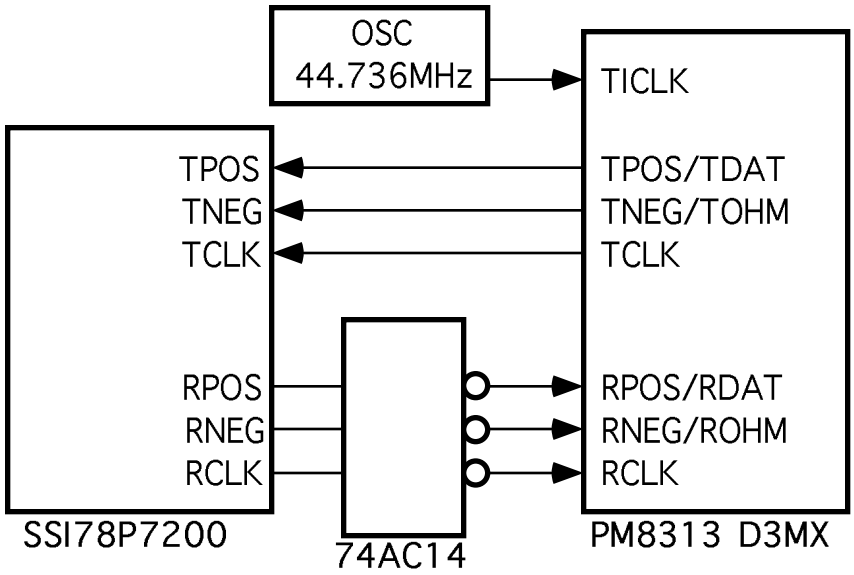
RECOMMENDED INTERFACE

The recommended solution to the duty-cycle distortion problem detailed above is to buffer the SSI outputs to increase the CMOS slew rate, thereby causing less distortion. The AC (Advanced CMOS) series of standard logic is fast enough to buffer 44.736MHz signals while making a marked improvement in slew rate.

Level-shifting the SSI CMOS outputs to TTL levels is not a recommended alternative because most simple level-shifting circuits will load the SSI outputs too much for guaranteed operation.

Figure 2 shows an 74AC14 hex inverter used to buffer the SSI outputs. Since the 74AC14 causes a logical inversion of the signals, the digital receive interface of the D3MX must be configured accordingly: the RINV and RFALL bits in Register 05H must both be set to logic one.

Figure 2. Recommended Connections — PM8313 D3MX to SSI78P7200



All other connections to the PM8313 D3MX and SSI78P7200 should be made according to the latest issues of the respective datasheets.

Note: The circuit in Figure 2 has not been tested by PMC-Sierra; it is based on published specifications of the devices involved.

REFERENCES

- PMC-Sierra PMC-920702S4 "PM8313 D3MX M13 Multiplexer" Data book, July 1994.
- Silicon Systems® "1994 Data Book — Integrated Circuits for Communication Products"

NOTES

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