

FEATURES

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 - Monolithic single-chip ATM User-Network Interface (UNI) for DS3, E3, DS1, and E1 Plesiochronous Digital Hierarchy (PDH) applications.
 - Provides on-chip DS3 (M23 or C-bit parity) and E3 (G.751 and G.832) framers.
 - Implements the ATM direct cell mapping into DS1, DS3, E1, and E3 transmission systems according to ITU-T Recommendation G.804.
 - Implements the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432.
 - Implements the Physical Layer Convergence Protocol (PLCP) for DS1 and DS3 transmission systems according to the ATM Forum User Network Interface Specification and ANSI TA-TSY-000773, TA-TSY-000772 and E1 and E3 transmission systems according to ETSI 300-269 and ETSI-270.
 - Provides UTOPIA L1-compliant ATM-PHY interface.

- Supports DS3 FEAC code insertion/detection and provides an integral HDLC transceiver for path maintenance datalink processing.
 - Supports G.832 Trail Trace and provides an integral HDLC transceiver that supports the Network Requirement or General Purpose datalinks.
 - Provides detection of DS3/E3 Loss Of Frame (LOF) and yellow alarm.
 - Accumulates BIP-8, framing and FEBE events.
 - Provides ATM cell scrambling/descrambling, HCS error detection and correction, HCS insertion, idle/unassigned ATM cell filtering and insertion, and accumulates counts of transmitted and received cells.
 - Provides DS3/E3 diagnostic loopback, line loopback, payload loopback and ATM cell loopback.
 - Provides support for an arbitrary rate external transmission line interface up to a maximum rate of 52 Mbit/s.

- Uses PMC-Sierra PM4341A T1XC T1, PM6341 E1XC E1, or PM4351 COMET framer/line interface devices for DS1, E1, and J1 ATM UNI applications.
 - Software-compatible with the PM4341A T1XC, PM6341 E1XC, PM4351 COMET, M5346 S/UNI[®] LITE, and PM7344 S/UNI-MPH.
 - Application-compatible with the PM8313 D3MX, PM4314 QDSX, and PM7323 RCMP-200.
 - Provides an 8-bit microprocessor interface for configuration, control, and status monitoring.
 - Low power CMOS technology.
 - Available in a high density 100-pin PQFP package (14 by 14 mm).

APPLICATIONS

 - ATM Switches
 - ATM Routers
 - ATM Network Interfaces
 - DSLAMs
 - ATM / SMDS Test Equipment

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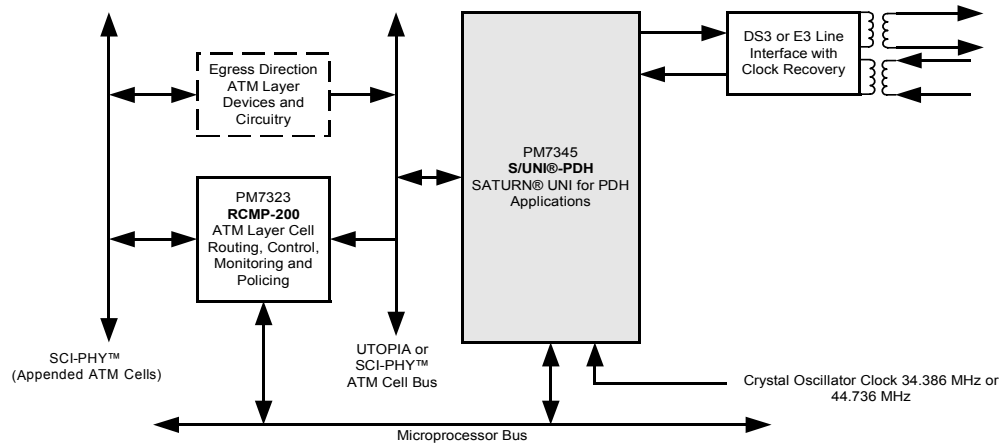
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The diagram illustrates the internal architecture of the 5.5" x 3" Block. The central components include the TRAN (Transmit DS3 or E3 Transmit Framer), FRMR (Receive DS3 or E3 Receive Framer), SPLT (Transmit ATM and PLCP Framer), and ATM/SPLR (Receive ATM and PLCP Framer). These are connected to various peripheral blocks such as XBOC, XFDL, Transmit O/H Access, 1/2 TTB Transmit Trail-Buffer, RBOC, RFDL, PMON, Receive O/H Access, and 1/2 TTB Receive Trail-Buffer. The system also includes a TXCP (Transmit Cell Processor), TXFF (Transmit 4-Cell FIFO), RXCP (Receive Cell Processor), RXFF (Receive 4-Cell FIFO), and a CCPM (PLCP/cell Performance Monitor). A MPIO (Microprocessor Interface) is connected to the System Interface. The block is shown with multiple input and output signals, including TCLK, TPOS/DAT, TNEG/TOHM, RCLK, RPOS/RDAT, RNEG/ROHM, TDLSIG, TDCLK, TOH, TOHNS, TOHCLK, TOHFP, TOHM, C13/CADDBREF, TPOHFP, TPOHCLK, TPOHNS, TPOH, TCELL, FWDATA[7:0], TFCLK, TWREN, TSOC, TCA, TXPRTY, RSOC, REOH, REOC, RCA, RXPRTY, RRDEN, RFCLK, FRDATA[7:0], TSEN, INTB, SSB, WRB, CSB, ALE, A7:0, D7:0, RPOHFP, RPOHCLK, RPOH, and RCELL.

SATURN User Network Interface for PDH Applications

TYPICAL APPLICATIONS

DS3 OR E3 ATM USER NETWORK INTERFACE



DS1 OR E1 ATM USER NETWORK INTERFACE

