SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

M3488 DIGITAL SWITCHING MATRIX

INTRODUCTION

The M3488 DIGITAL SWITCHING MATRIX device can be used as a basic component in modern digital switching systems.

This Technical Note is a guide for designers who wish to use the M3488 in their systems.

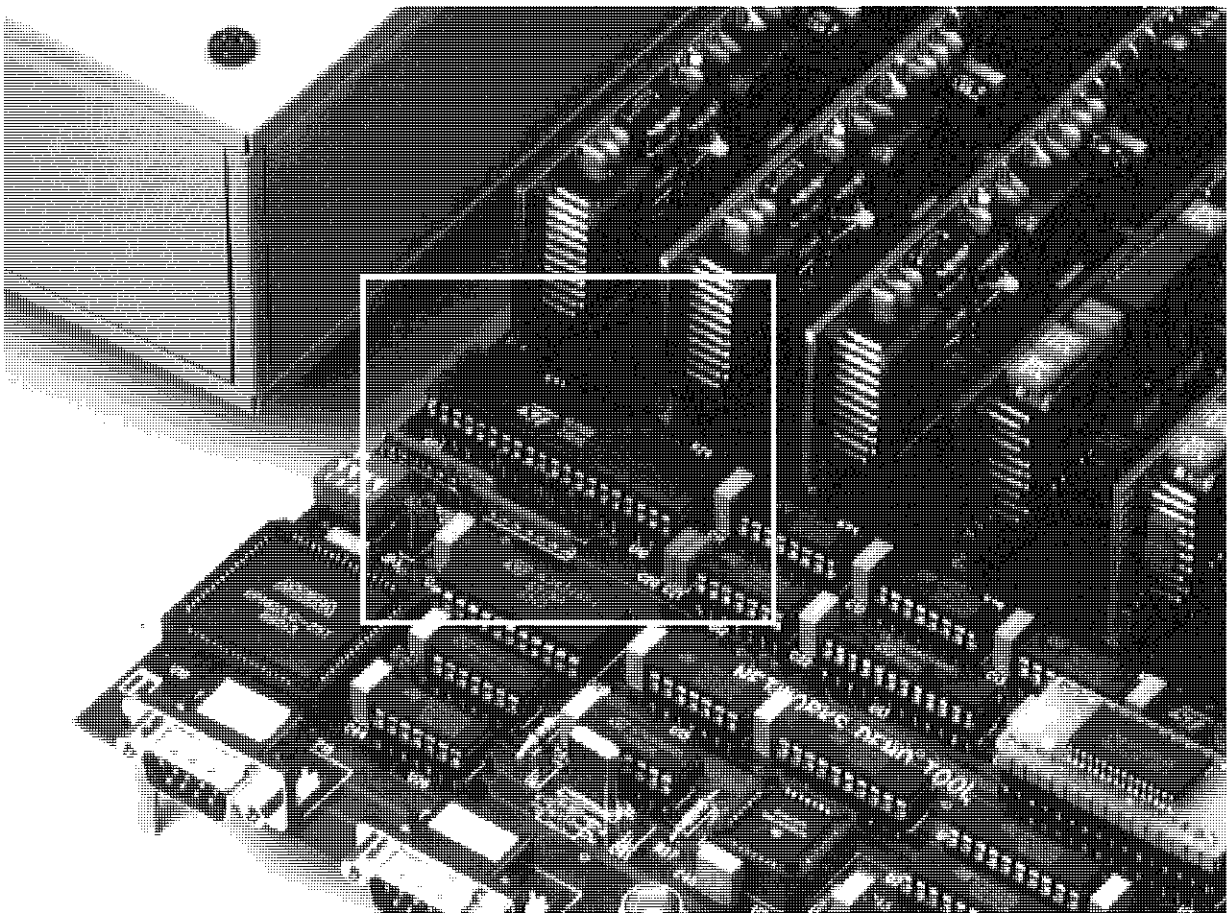
Section 1 contains introductory material in the field of digital switching and can be quickly passed over by experienced designers.

The main characteristics of the M3488 are shown in Section 2.

Sections 3 and 4 describe, respectively, the internal structure, and the various functions which may be implemented.

Some detailed material concerning timing and some important services are examined in Section 5.

Section 6 is dedicated to applications. Another component, the M3116, used in this field, is introduced in this section ; of particular note is the fact that the M3116 is a digital device which realizes conference and tone generation functions.



1. DIGITAL SWITCHING TUTORIAL

WHAT IS A DIGITAL SWITCHING MATRIX (DSM) ?

A Digital Switching Matrix is a device which permits switching a certain number of signals among themselves.

The signals to be switched can either be digital or analog ; in the latter case, digitalization of these signals must be provided before switching takes place.

Digitalization takes place in three stages :

a) band limiting (by a low pass filter) ;

b) sampling ;

c) digital coding.

PULSE CODE MODULATION (PCM)

The technique of digitalizing signals used in telephonic applications is called PCM.

The signal to be digitalized is sampled every 125 µs, in other words, with a frequency equal to 8 KHz since, according to the Nyquist law, the sampling frequency must be greater or equal to twice the maximum frequency of the analog signal being sampled. As is well known in telephony, this frequency is less than 4 KHz.

Based on input signal sampling (see fig. 1-1), the coding links a given sample to an 8-bit binary number.

Thus, the number of discrete levels becomes $2^8 = 256$.

Non-linear coding laws are used. The main ones are the two following :

- Mu law used in the USA, Canada and Japan ;
- A law used in Europe, South America, Australia and Africa (see fig. 1-2).

Since the sampling frequency is 8 KHz, the digitalized signal will be made up of a number of bits per second equal to (8 · 8000) = 64000 bit/s.

TIME DIVISION MULTIPLEXER (TDM)

TDM is a technique which permits merging various digital signals into a single high velocity signal. Many stages of switching will, thus, become easier.

Fig. 1-3 presents a diagram of the TDM principle.

TDM is based on the serializer, which accepts PCM signals at the input, and provides them at the output, accessed cyclically.

Each input channel is linked to a time slot, and is thus fixed precisely in the serialized output stream.

Figure 1.1 : SAMPLING & CODING. The Analog Signal to be digitalized is First Bandwidth limited (fig. 1.1a) Then Sampled at a Frequency f_S (fig. 1.1b). The Resulting Periodic Sequence of Samples is shown in Fig. 1.1c. Each Sample is then replaced with an 8–Bit Word representing the Amplitude (fig. 1.1d).

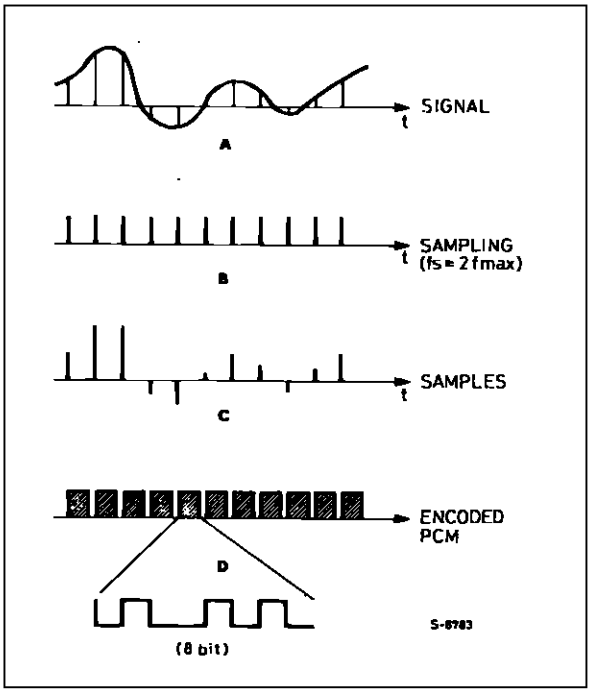
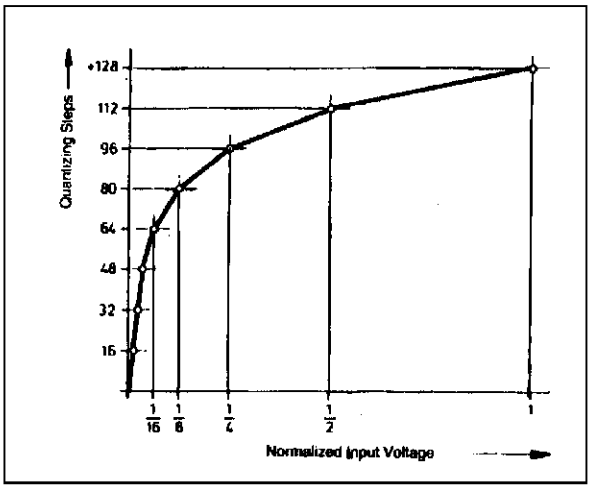


Figure 1.2 : The Quantization Curve for A-law Limited to Positive Samples. Each Group of 16 Steps is Contained in a Segment and the Normalized Values of the Input Signal Corresponding to the Extremes of Each Segment are One Half of Each Other.



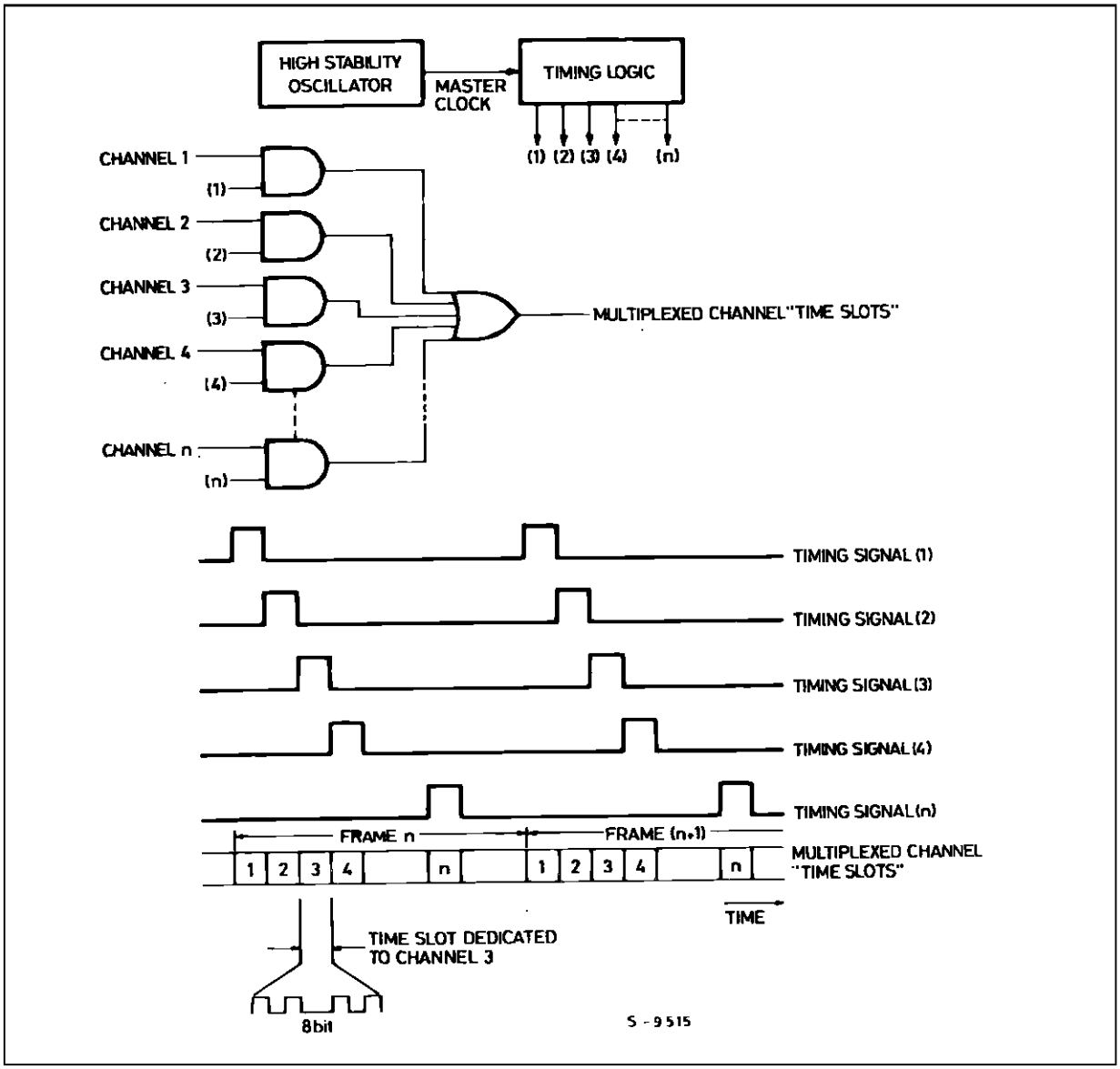
A very stable oscillator provides the master clock and all the timing functions used in the multiplexer.

The international standards for the TDM are two, namely :

a) the North American Standard (PCM 24 Transmission System) ;

b) the European Primary System (PCM 30 Transmission System) ;

Figure 1.3 : The Basic Principle of Time Division Multiplexing (TDM). Data from n Independent Channels are Compressed and Transferred to a Single Output. Each Channel Outputs Its Data in Separate Time Slots Defined by a Timing Circuit.



THE NORTH AMERICAN STANDARD (PCM 24)

Fig. 1-4 presents the PCM 24 Transmission System frame format.

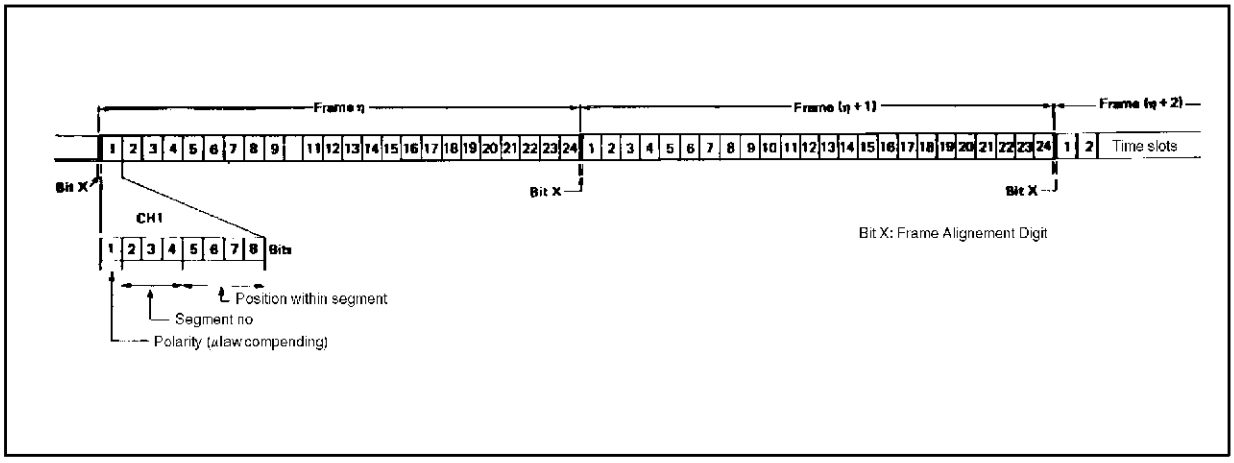
Each of the 24 channels has already been sampled at 8 KHz and coded, using Mu law with 8-bit words.

Messages reaching the channels are word interleaved, forming an uninterrupted sequence of 192 bits.

A single alignment framing digit (bit X) is inserted at the beginning of each sequence ; thus the total number of digits in a frame is 193. The velocity of the signal in bit/s is thus (8000 · 193) = 1544 Kbit/s.

In certain applications, usually PABX, the Extra bit (bit X) is omitted. In this last case the velocity of the signal becomes (8000 · 192) = 1536 Kbit/s.

Figure 1.4 : Frame Format of the Bell T1 (PCM24) System. Each Frame Contains 24 Channels PLus One Signalling Bit (bit X). This Format is Used in the USA, Canada and Japan.



THE EUROPEAN PRIMARY SYSTEM (PCM 30)

Fig. 1-5 shows the European Primary System frame format.

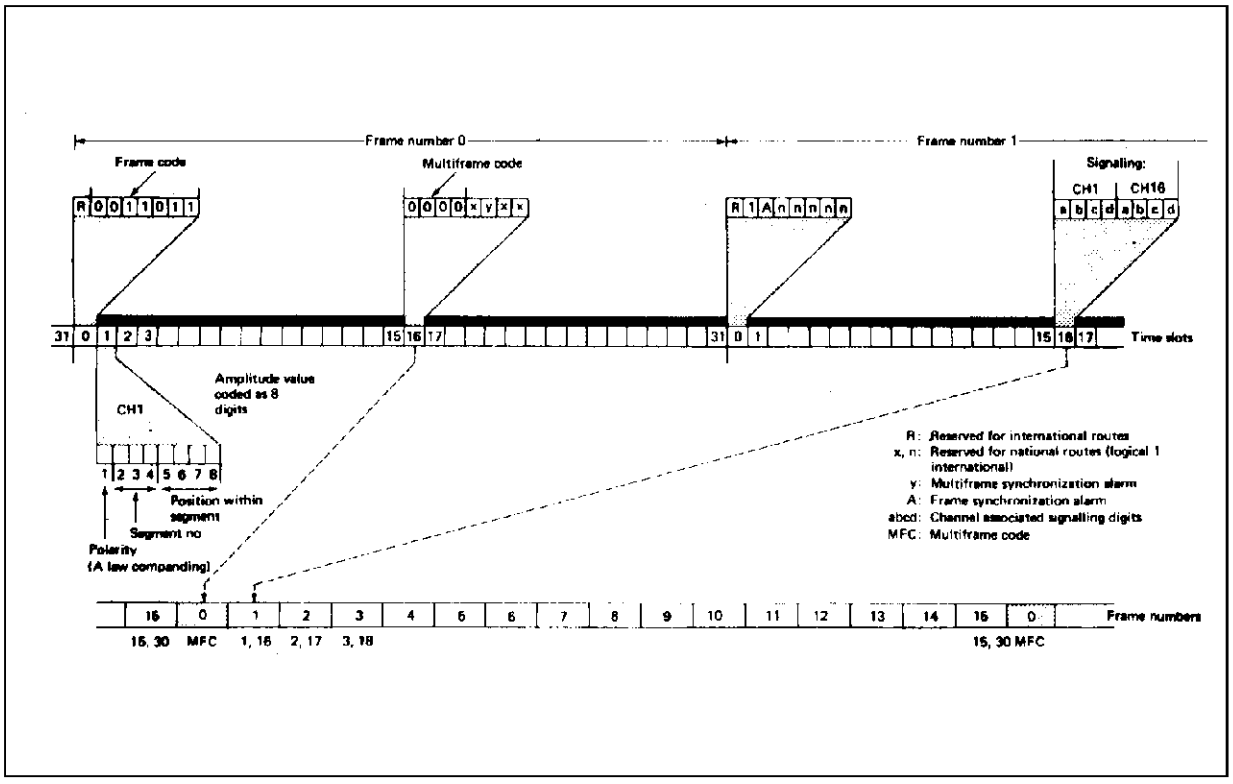
TDM combines 30 voice channels, sampled at 8 KHz, and coded using A law with 8-bit words.

Various channels messages are combined by word interleaving ; thirty 8-bit words are inserted in a frame with 32 time slots, numbered from 0 to 31.

Two of the slots (0 and 16) are used for frame alignment and signalling.

Each frame has (8 · 32) = 256 bits, and its velocity is (8000 · 256) = 2048 Kbit/s.

Figure 1.5 : Frame Format of the European System (PCM30). Each Frame contains 32 Channels of which two are dedicated to signalling. This Format is used in Europe, Latin America, Australia and Africa.



TIME AND SPACE DIVISION SWITCHING

Fig. 1-6 represents, using blocks, a digital switching system. Individual analog lines are applied to a multiplexer, which provides for their digitalization and merges them into a frame.

The various frames are transmitted to the switching matrix which carries out exactly the switching function, building various output frames as required.

These frames are transmitted to a demultiplexer which separates them into single channels, which, after conversion from digital to analog, are transmitted to the respective analog output lines.

Fig. 1-6 presents an example : subscriber S1-5 wishes to be connected to subscriber S8-11 ; S1-8 with S4-10.

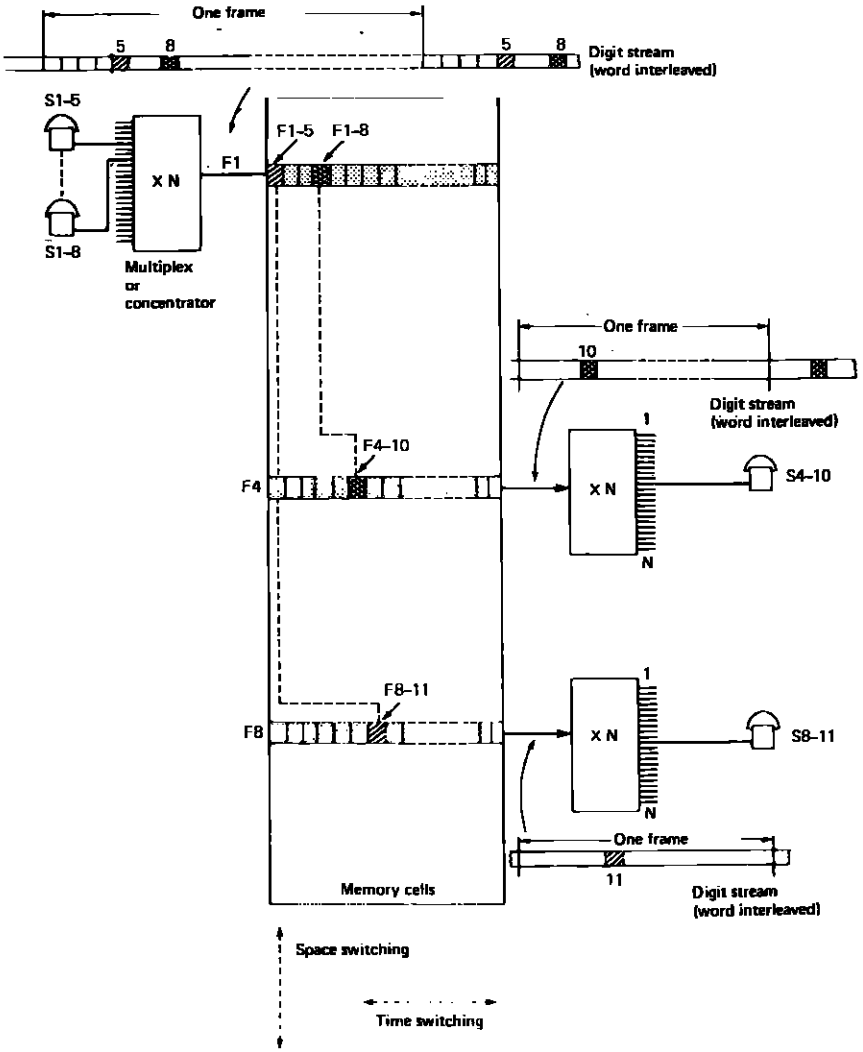
The connection operation between S1-5 and S8-11 involves two operations :

1) transfer of information from layer F1 to layer F8 (space division switching) ;
2) transfer from position 5 to 11 (time division switching).

Likewise, the connection between S1-8 and S4-10 involves space switching between F1 and F4, and time switching between positions 8 and 10.

SGS THOMSON digital switching matrixes operate, using this technique of time and space division switching, permitting switching without blocking, in other words, simultaneously of 256 channels.

Figure 1.6 : Space-and-Time-switching Digitally encoded Signals.



2. INTRODUCTION TO THE M3488 DSM

GENERAL DESCRIPTION

The M3488 device implements a non-blocking digital switching matrix, which operates with a maximum of 256 x 256 channels.

These channels are applied and extracted from the device, using 8 PCM frames at 2048 Kbit/s, each containing 32 channels.

The M3488 can connect each input channel with, or disconnect it from, any output channel in addition to carrying out other functions described in Section 4.

It can also be used at lower velocity, for example, to switch 192 x 192 channels, organized in eight frames of 24 channels each, at 1544 Kbit/s, using the North American Standard (PCM 24) or at 1536 Kbit/s.

Finally, there is no prohibition against using the device for non-standard applications, for example, in the field of Data Communications. A few examples are cited in Section 6.

KEY FEATURES

- A 256 input and 256 output channels digital switching matrix ;
- A building block designed for large capacity electronic exchanges, subsystems, voice-data PABXs ;
- European Primary System compatible (32 channels per frame) ;
- North American Standard (T1 System) compatible (24 channels par frame) (*) ;
- PCM input and output mutually compatible ;
- Actual input-output channel connections stored and modified using an on-chip 8-bit parallel microprocessor interface.
- 6 main functions or instructions available ;
- 5-volt power supply ;
- MOS and TTL input/output levels compatible ;
- High density advanced 1.2µm HCMOS3 process.

(*) For further information, see below, Section 6.

3. M3488 INTERNAL STRUCTURE

The component includes a Speech Memory, Control Memory, circuits for Serial to Parallel Conversion of incoming PCM links and for Parallel to Serial Conversion of the outgoing PCM links and a Bidirectional Interface for an 8-bit microprocessor. In addition, the M3488 performs other useful functions, such as Byte Insertion and Extraction, Addressing Memory Reading and 0 Channel Extraction. Referring to Fig. 3-1, the following functional blocks can be distinguished :

- Time Base
- Serial Parallel Converter for the PCM input links
- Speech Memory
- Control Memory
- Internal PCM Bus
- Parallel Serial Converter for the PCM output links
- Control and Interface Logic to and from the µP

TIME BASE

The time base generates the internal synchronous timing signals, using only two external signals, the clock (4.096 MHz) and the frame synchronism (8 KHz), supplied to the corresponding external pins of the device (CK and SYNC pins). The time base provides two ring counters, generating two sets of timing signals (e1 to e8 and u1 to u8), used for Serial to Parallel Conversion of input time slots and Parallel to Serial reconversion of output PCM time slots, respectively.

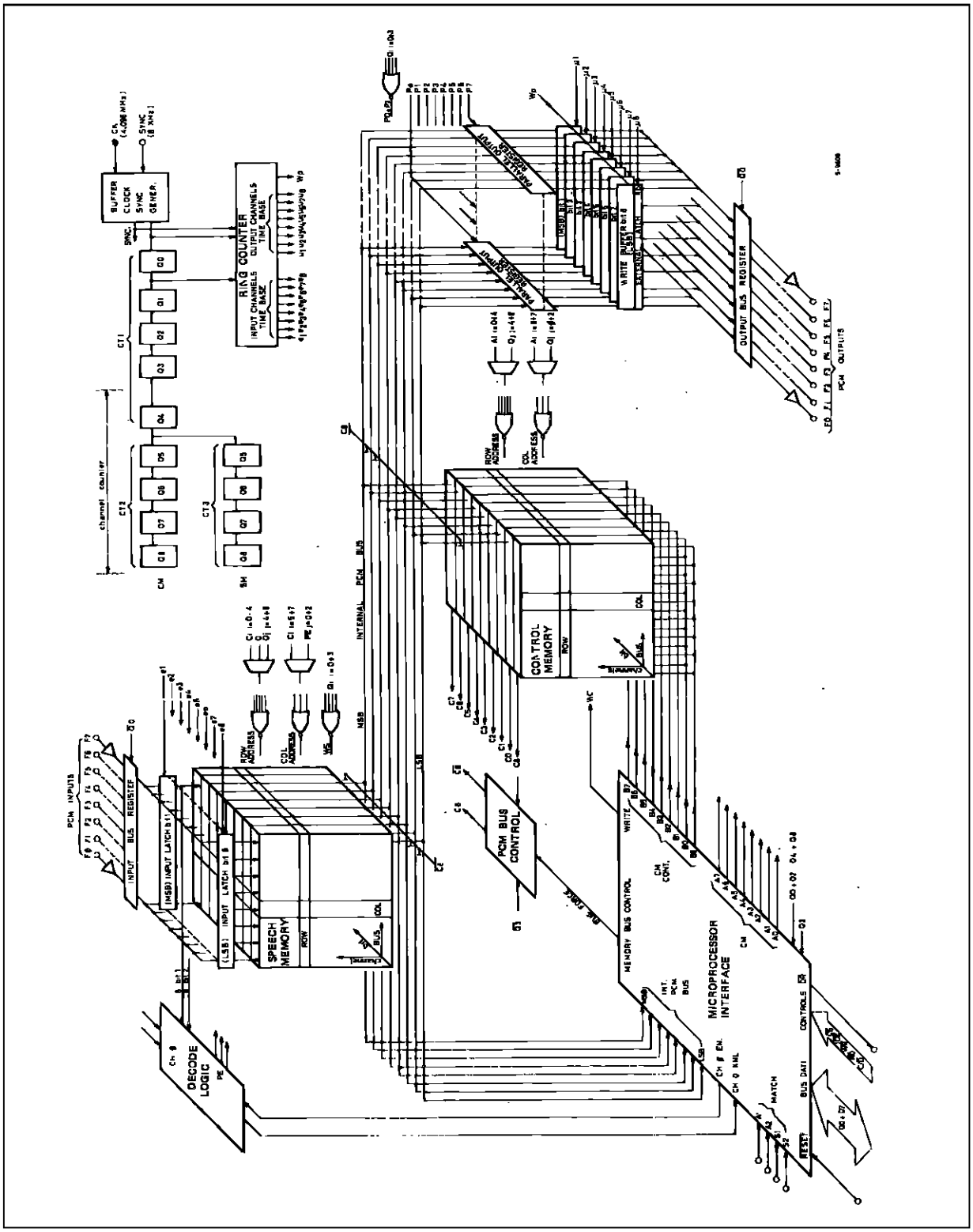
The time base consists mainly of a fast synchronous parallel resettable counter of which stages are obtained by repeated clock division and grouped into three subsets : the first, CT1, starting from the 250ns rate, generates the time phases controlling the 4µs input and output time slot servicing ; in particular, the signal Q3 (4µs) specifies two working phases : one dedicated to the microprocessor interface operations, the other related to PCM operations. The other two subsets, CT2 and CT3, operating synchronously with respect to CT1, generate the sequential channel addresses for control memory reading and for speech memory reading, respectively.

The counter CT2 addresses the control memory, using the output PCM channel address increased by one ; the counter CT3 addresses the speech memory, using the input PCM channel address decreased by one. This address difference is necessary to compensate for the internal component delay due to input and output PCM conversion.

INPUT SERIAL TO PARALLEL PCM CONVERTER

During each time slot (4µs), the 8 serial PCM (2048 Kbit/s) input bits are regenerated and sampled using a 500 ns clock signal, Q0, and then are stored in 8-bit latches clocked by the input ring counter's e1 to e8 signals. As soon as the 64 bits are updated, they are written, using a single write pulse, into the speech memory at the corresponding input channel address, selected by subset counter CT3, performing the parallel conversion in the same writing operation.

Figure 3.1 : The Fundamental Blocks are the Speech Memory (SM), which memorizes for Each Frame the Contents of All 256 Channels, and the Control Memory (CM) which contains Information on the Status of the 256 Output Channels (connected or not connected, loaded by the micro with a given byte).



SPEECH MEMORY

The memory is organized as 32 planes of 8 rows and 8 columns each ; every plane corresponds to an input PCM channel, every row to a bit of content and every column to an input PCM line. The working cycle is about 4µs, with this time divided into 2µs phases. The first one consists of eight 250 ns cycles : one particular cycle is devoted to memory updating according to input channel data ; in the other cycles, functions engaged by the µP interface logic can be performed at random in the memory (that is the case of PCM output channel reading). In the second, memory is cyclically read 8 times, using the control memory addresses, C0 to C7 (switching function).

CONTROL MEMORY

Control Memory is organized in 32 planes of 9 rows and 8 columns each ; every plane corresponds to any output PCM channel, every row to a content bit and every column to an output PCM line. The Control Memory working cycle is similar to the Speech Memory.

During the first 2µs phase, the Control Memory is idle and normally accessible to µP interface. On occasion, because of network connection updating or µP requests, some cycles are stolen here for this purpose. During the latter 2µs phase, the memory is read eight times, using the addresses coming from the time base (subsets CT1 and CT2). The output contents of 9 bits each are used as addresses for Speech Memory (C0 to C7) and as a control signal for switching the internal PCM bus to the proper Control or Speech Memory output data (C8).

INTERNAL PCM BUS

Speech and Control Memories are connected to the internal 8-bit parallel bus. The 9th Control Memory bit controls each memory's output during the switch function ; otherwise, it is forced by the µP interface.

The internal bus is connected on one side to the µP interface to perform functions like memory content transfer. On the other side, the bus connects the PCM Parallel to Serial conversion unit.

OUTPUT PARALLEL TO SERIAL CONVERTER

The bytes of the internal PCM bus, belonging to the 8 cycles previously mentioned in Control Memory, are saved in a group of 8 temporary registers, each selected by the timing signals P0 to P7 (see fig. 3-1). When all bytes are stored, a single pulse transfer takes place in order to supply new PCM data to the output registers.

The proper time phases u1 and u8 sequentially scan the 8 output registers and simultaneously feed the output pins performing the Parallel to Serial conversion. The output PCM flows are resynchronized, using a 500ns clock signal (Q0). PCM outputs are open drain type.

MICROPROCESSOR INTERFACE LOGIC

The interface logic controls, asynchronously with respect to the PCM timing, the 8 bit data bus and the control bus to and from the microprocessor. It also stores, in a five byte stack, the data field and the opcode instruction. It gives the other internal blocks the necessary signals to perform the function in the right time phase. Moreover, it stores the status information, which can be read by the µP for diagnostic purposes, in two internal registers, OR1 and OR2.

The external control bus allows the component to be used as a standard 8-bit peripheral device. It consists of RD and WR signals for reading and writing into the M3488 respectively, and the C/D signals, which selects between data and operating the code of command bytes to the written into the M3488. Signals CS1 and CS2 activate the component when other peripheral devices are connected to the same bus.

Signals A1, S1, A2 and S2 allow more M3488s to be connected in a simple way to obtain non-blocking matrix structures. An M3488 in a match condition where A1 = S1 and A2 = S2 is active, while the others are automatically disabled.

4. FUNCTIONAL DESCRIPTION

The device, controlled by the microprocessor, implements six different instructions. A specific function is executed after the microprocessor has transmitted, using the data bus, the data bytes and the command bytes.

Two or four data bytes carry the information necessary for the correct interpretation of the function. The command byte follows these with the operative coding information necessary for M3488 to execute the function.

Brief descriptions of individual functions are given here. For further information, the M3488 data sheet for the device should be consulted.

FUNCTION 1 : CHANNEL CONNECTION/DISCONNECTION

This function permits the formation of a new connection between a given input channel (C_{IN}) and a given output channel (C_{OUT}). See fig. 4-1.

The message coming from the microprocessor consist of four data bytes plus a command byte.

The first two data bytes carry, respectively, information about the PCM input line and the input channel ; the third and fourth bytes carry information about the PCM output line and the output channel.

The first two bytes are loaded in the control memory cell (CM), the address of which is specified in the last two bytes.

It cases of switching systems of more than 256 x 256 channels some examples are given in Section 6 use is made of additional M3488 chips, interconnected as required (multi-chip matrices).

In this case, the connection function is executed only by the M3488 in match condition (A1 = S1 and A2 = S2) ; all the other M3488s of the multi-chip matrix involved with channel C_{OUT} will execute a disconnection operation from that selected output channel (C_{OUT}).

FUNCTION 2 : CHANNEL DISCONNECTION

Disconnect the selected output (C_{OUT}). See fig. 4-2.

The message coming from the microprocessor is made up of two data bytes plus a command byte.

The first and the second bytes carry, respectively, information about the PCM output line and the output channel which must be disabled.

FUNCTION 3 : BYTE INSERTION/CHANNEL DISCONNECTION

The function permits a byte furnished by the microprocessor to be inserted in an output data channel (C_{OUT}). See fig. 4-3.

The message is made up of four data bytes plus a command byte.

The first and second bytes contain information for transferral to the PCM output channel. This 8-bit information is memorized inside a control memory cell (CM).

The third and fourth data bytes contain, respectively, information on the PCM output lines and on the output channel in which the byte is to be inserted. These last bytes are used as an address to specify the CM cell in which to load the information contained in the first two data bytes.

As was the case for the first instruction examined, in the case of multi-chip matrices, this instruction is executed only by the selected M3488 ; all the remaining M3488s of the matrix will execute a disconnection operation on the selected output channel.

FUNCTION 4 : BYTE EXTRACTION

This function permits transferral of the byte contained in an output data channel to the microprocessor, using the data bus.

The message is made up of two data bytes plus a command byte.

The first and second bytes contain, respectively, the number of PCM output line and of the output channel, the contents of which are to be read by the microprocessor.

The PCM octet is memorized by the device in register OR1 ; thereafter, the microprocessor, using the aforementioned register's read cycle, transfers the PCM sample to the CPU.

If it is useful to read the PCM byte from an input data channel C_{IN}, C_{IN} must be connected with a particular output channel C_{OUT}, and thus apply the extraction function to C_{OUT}. See fig. 4-4.

Figure 4.1 : Connection Any of the 256 Input Channels (C_{IN}) can be Permanently connected to any of the 256 Output Channels (C_{OUT}). It is Possible to have 256 Connections simultaneously.

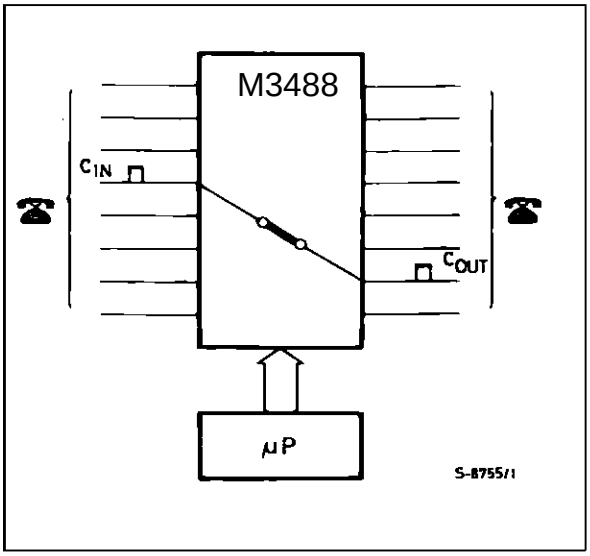


Figure 4.2 : Disconnection. Each Connection Previously made can be interrupted at any Time.

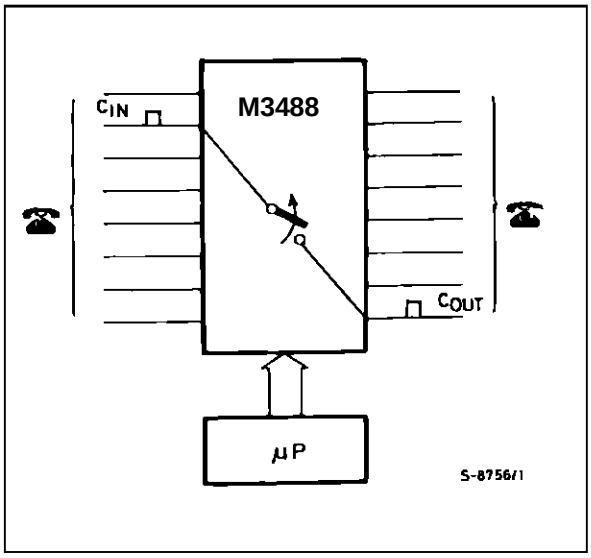


Figure 4.3 : Insertion of a Byte. The Control Microprocessor can send a given Byte to Any Output Channel.

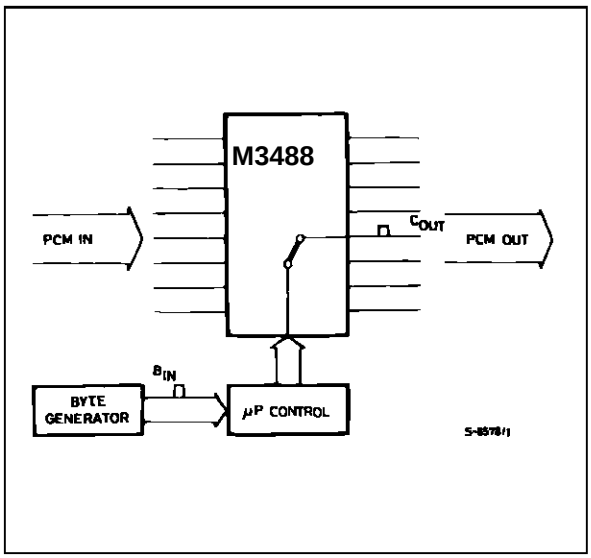
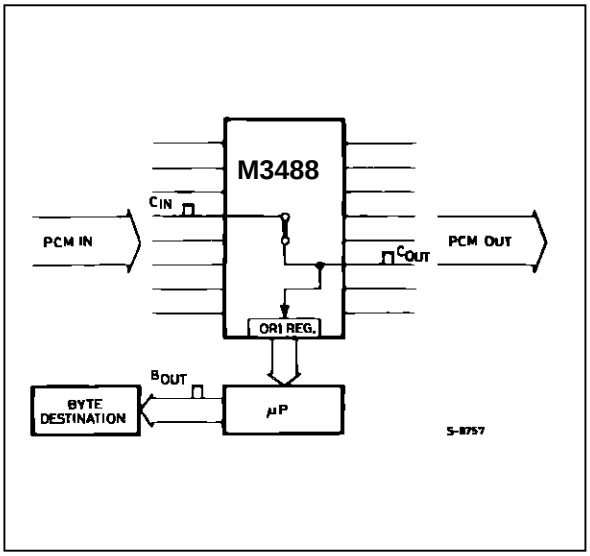


Figure 4.4 : Extraction of a Byte. The Micro Can Extract from Any Output Channel (C_{OUT}) the Contents (B_{OUT}) at the Time of the Request.



FUNCTION 5 : CONNECTION MAP READING

This function makes it possible to know, starting from a particular output channel C_{OUT}, the contents of the corresponding control memory cell CM, the address of which is exactly the same as C_{OUT}. See fig. 4-5.

As already explained in Section 3, each control memory cell CM is made up of nine bits (C8, C7.... C0).

If the ninth bit is equal to zero, the eight remaining bits (C7, C6.... C0) provide information concerning the input channel C_{IN} connected simultaneously with C_{OUT}. In particular, C7, C6 and C5 provide the PCM input line number, while C4, C3, C2, C1 and C0 provide the relevant C_{IN} channel number.

On the contrary, if bit C8 is equal to one, two possibilities can be examined :

a) byte C7, C6.... C0 is equal to 11111111 – in this case, output channel C_{OUT} is not connected to any input channel C_{IN}, and the microprocessor

never loaded any byte on the basis of instruction 3 ;

b) byte C7, C6.... C0 is not equal to 11111111 – also, in this case, the C_{OUT} channel is not connected to any input channel C_{IN}, however, the aforementioned byte is a copy of the one which the microprocessor has already loaded in C_{OUT}.

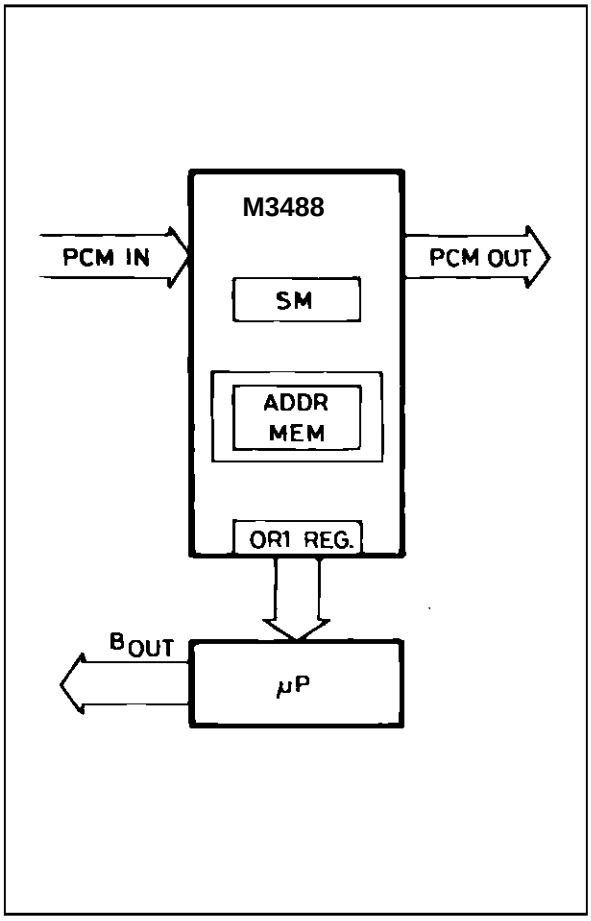
The message coming from the microprocessor is made up of two data bytes plus a command byte.

The first and second bytes correspond, respectively, to the number of PCM output line and to the C_{OUT} channel, and, as already mentioned, correspond to the CM cell address whose contents the microprocessor must read.

Bits C7, C6.... C0 are memorized in the OR1 register, while bit C8 is memorized in the OR2 register.

With two read cycles, the microprocessor can thus transfer the contents of the two registers OR1 and OR2 into the CPU.

Figure 4.5 : Reading the Control Memory. Through This Operation the Microprocessor Can Read the Status of Every Output Channel.



FUNCTION 6 : CHANNEL 0 CONNECTION MASK STORE/DATA TRANSFER

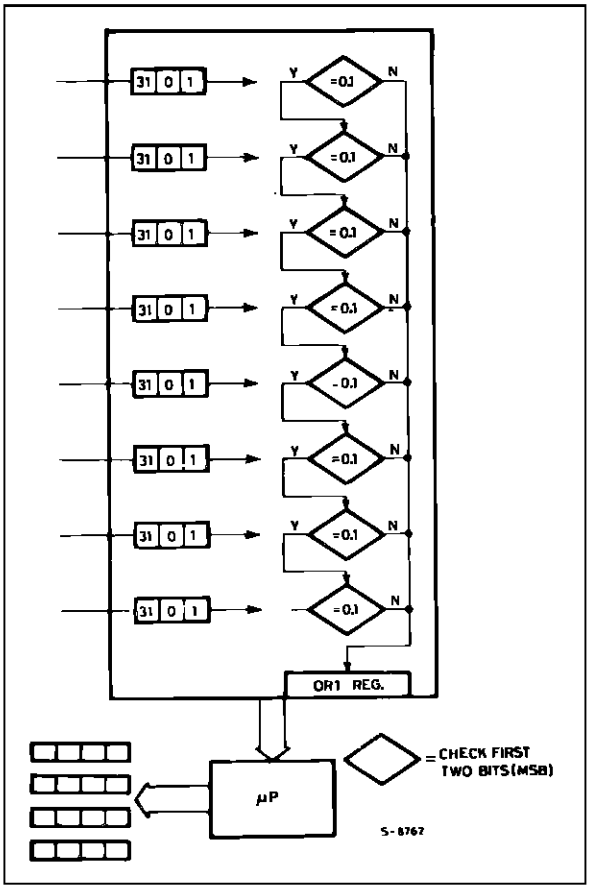
This last function is used to extract information rapidly from channel 0. See fig. 4-6. The indispensable requirement for the extraction to take place is that the two most significant bits of the byte contained in channel 0 not be equal to 01.

The PCM input lines from which the 0 channels are extracted are selected by using the microprocessor to load two data bytes, comprising the mask byte and a command byte.

The contents of channel 0 are available from the OR1 register, from which the microprocessor can transfer them externally by successive reads from the same register.

Experimental testing has shown that, with a CPU clock of 4.000 MHz in a time frame (125µs), it is possible to extract the 0 channels from all eight PCM lines.

Figure 4.6 : Rapid Extraction of Channel 0. Allows the Extraction of the Contents of the Active Channel Zeros and Channels with the Most Significant Bits Not Equal to 01.



5. VARIOUS NOTES AND CONSIDERATIONS ABOUT THE M3488

In this section, certain aspects of the timing and operation of the device will be described in some detail.

In order to better understand the subject matter, it is recommended to have already read the component's data sheet.

SYNC TIMING

One of the aspects which should be handled with particular attention in the use of the component is the timing relation between the synchronization signal ($\overline{SYNC}$) and the clock signal (CK).

The $\overline{SYNC}$ signal, specifically its rising edge, specifies the beginning of the frame and, thus, bit 0 of channel 0.

The zone sketched in fig. 5-1 shows the areas of possible transition of the rising and falling edges of the SYNC signal with respect to the CK signal.

The absolute value of the width of this zone (t_V) is :

$t_V\ (\overline{SY}) = t_{CK} - t_R - t_{HL}\ (\overline{SY}) - t_{SH}\ (\overline{SY})$

in which :

$t_V\ (\overline{SY})$ is the maximum time width of the area of the rising edge of SYNC ;

t_{CK} is the clock (CK) period ;

t_R is the maximum clock (CK) rise time (= 25 ns) ;

$t_{HL}\ (\overline{SY})$ is the $\overline{SYNC}$ minimum low level hold time (= 30 ns) ;

$t_{SH}\ (\overline{SY})$ is the $\overline{SYNC}$ minimum high level set-up time (= 80 ns).

The falling edge of $\overline{SYNC}$ can take place anywhere if the length of level 1 is greater or equal to t_{CK} and the length of level 0 is greater than or equal to :

$t_{SL}\ (SY) + t_R + t_{HL}\ (SY) = 115$ ns,

$t_{SL}\ (\overline{SY})$ being the $\overline{SYNC}$ min low level set-up time (60 ns).

PCM INPUT SIGNAL TIMING

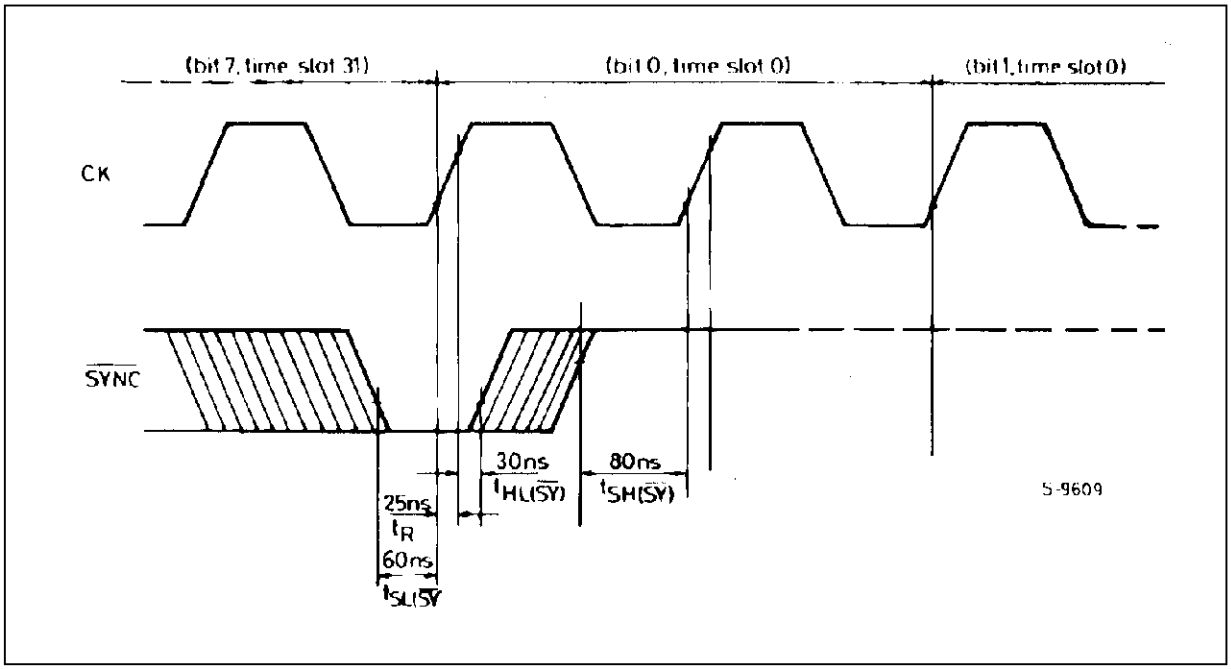
Another very important point is the timing relationship between the PCM input signals and the SYNC signal.

In many cases, it is of major importance to know how much the eight PCM input signals can be mutually dephased with respect to the CK signal.

Fig. 5-2 presents an example of dephasing of the general PCM input signal with respect to CK. To better illustrate this aspect in the figure, the PCM input signal is represented both with the minimum, and with the maximum, permissible delay.

In the same figure, an extremely interesting aspect is evident, namely, that the various PCM input flows

Figure 5.1 : SYNC Signal Timing. The Shaded Zones are the Regions of Possible Transitions. The Rising Edge of SYNC Determines Bit 0 of Channel 0.



are able to mutually tolerate dephasing at a level of nearly one bit-time.

Indeed, the time variation between the PCM input signals with minimum and maximum permissible delays, t_V (PCM), is as follows :

$t_V (PCM) = (2 \cdot t_{CK}) - (t_H (PCM) + t_R (CK) + t_S (PCM))$

Therefore, referring to fig. 5-2 ;

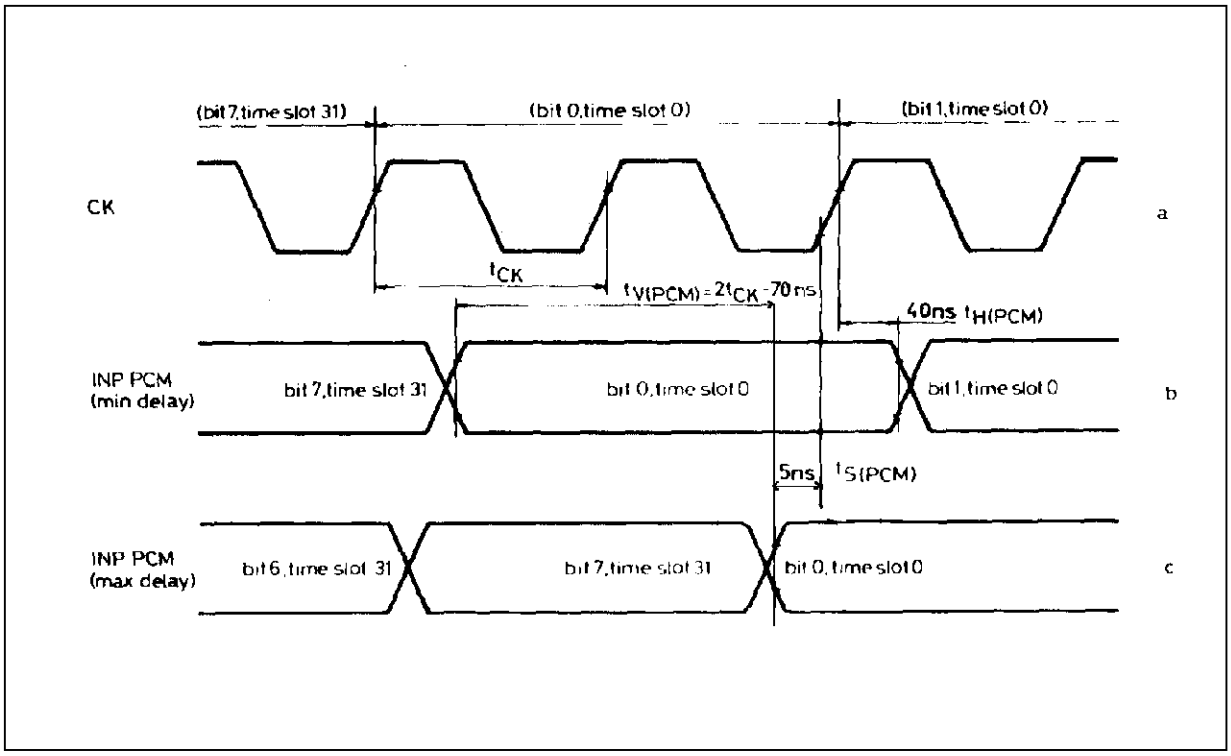
$t_V (PCM) = (2 \cdot t_{CK})$ -70 ns.

In the case of the European PCM (2048 Kbit/s), t_V (PCM) = 418 ns, or 86 % of bit-time.

In the case of the North American PCM (1544 Kbit/s, t_V (PCM) = 577 ns, or 89 % of bit-time.

This fact suggests one of the component's possible alternative applications, namely that of the PCM flow rephaser for delays included in values which have already been mentioned.

Figure 5.2 : Timing of the PCM Input Signal (INP PCM). This Diagram Illustrates the Cases of (INP PCM) with the Minimum (b) and Maximum (c) Tolerated delay Referred to the Clock Period (a) Corresponding to Bit 0 of Channel 0. Note That the Regions of Possible Variation Correspond to Almost One PCM Bit Period.



PCM OUTPUT SIGNAL TIMING

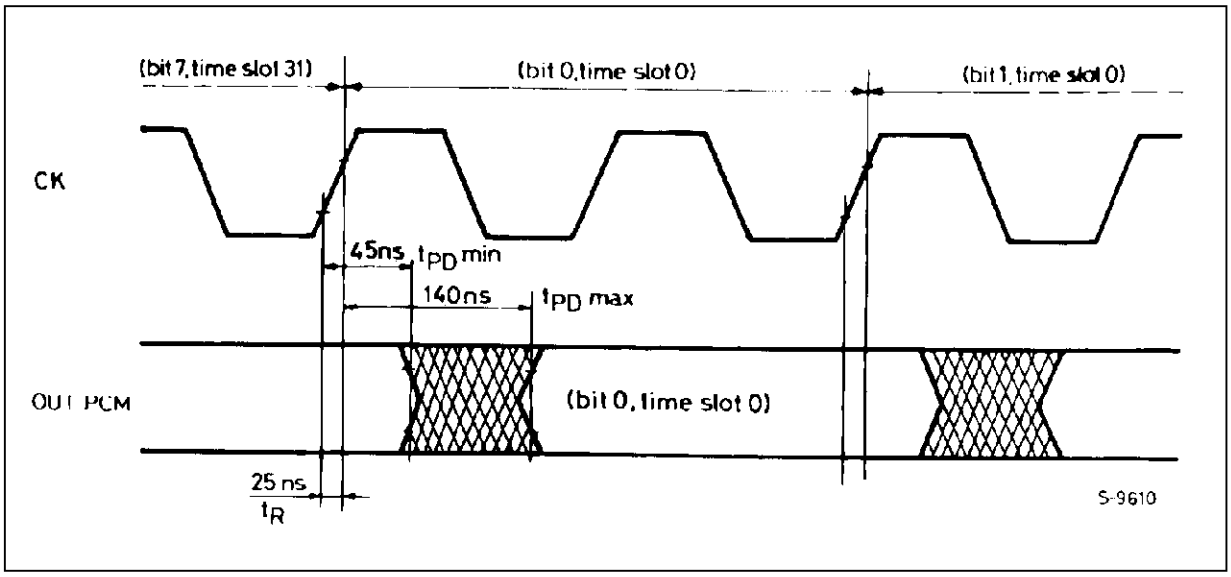
Fig. 5-3 shows the areas of variation of the edges of the PCM output signal with respect to the CK signal, the PCM input signal with maximum and minimum delay.

The width of such areas amounts to 155ns.

Also, the figure clearly indicates the possibility of using the PCM output flows as PCM input flows, in other words, to create a loop between the PCM outputs and inputs.

This could be used for test operations or for introducing frame delays into the PCM flow.

Figure 5.3 : Timing of the PCM Output Signal (OUT PCM). The Shaded Regions Indicate Where the Transitions May Take Place.



READ AND WRITE TIMING

The M3488 device requires that the PCM signals be correlated with the CK signal.

In theory, the microprocessor interface signals could be completely asynchronous with the CK signal.

In reality, that is completely true only in cases where M3488 is not inserted in a multi-chip matrix. In this last case, it is indeed to be recommended to link the $\overline{RD}$ and $\overline{WR}$ signals to the CK signal.

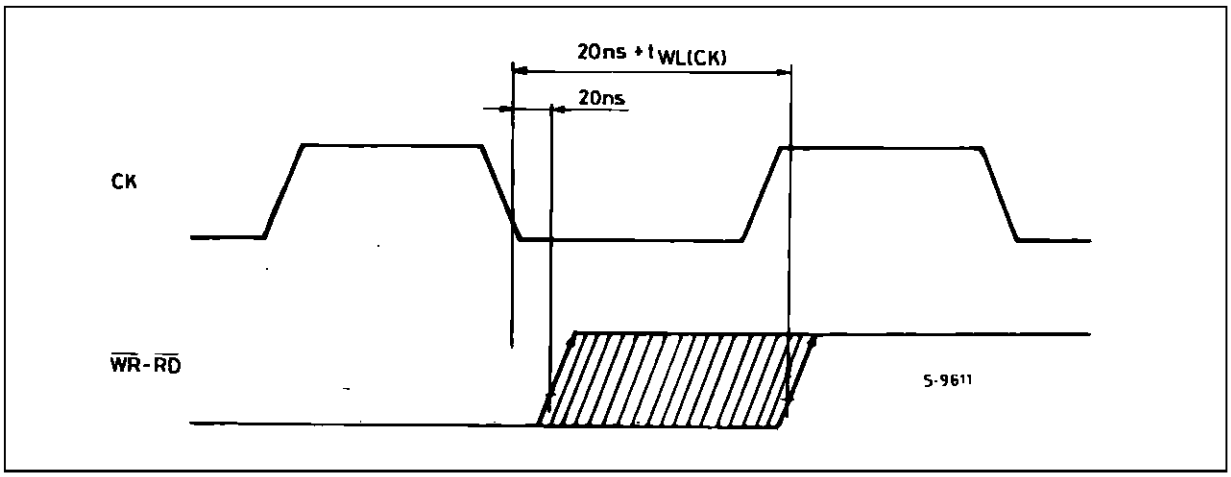
In particular, their rising edges must be delayed with respect to the falling edge of CK in a single phase, t_V (RW), in the range between 20ns and (20ns + t_{WL} (CK) = 120ns.

Fig. 5-4 presents an example of areas of transition among the rising edges of the aforementioned signals with respect to CK.

Given certain special conditions which are very difficult to deal with, problems could occur if the recommended synchronization for a multi-chip switching matrix is not respected. The connection of the relevant M3488 will be carried out before the disconnection of the output channels of all the remaining M3488s of the matrix.

This could cause an error in the correlation of the first bit in the first byte of the signal transferred.

Figure 5.4 : The Shaded Area Shows the Recommended Variation in the Rising Edge of the READ and WRITE Signals in the Case of Multi-chip Matrices.



Anyhow, this only concerns the first byte transferred ; there will be no problem with those following. Another interesting parameter concerning the $\overline{RD}$ and $\overline{WR}$ signals is the minimum timing interval to maintain between two consecutive cycles, in other words, between the two rising edges.

The timing, t_{REP}, is a CK period function, namely :

$$t_{REP} = 40\ ns + 2\ t_{CK} + t_{WL}\ (CK) + t_R\ (CK).$$

When $t_{CK} = 244ns$, $t_{REP} = 653ns$.

The reading operations of the OR1 and OR2 registers during instruction 6 are the only exceptions.

In this case, a request is indeed made for the minimum time between $\overline{RD}$ rising edges to be 3 CK periods for sequences from OR1 to OR2, and 13, for sequences from OR2 to OR1.

INSTRUCTION EXECUTION TIMING

Within a time slot (3.92µs for PCM input flows of 2048 Kbit/s), there are 16 CK periods. Each period corresponds to a machine cycle.

Of the 16 cycles contained in a time slot, 8 are free and are used to carry out instructions received from the microprocessor. Fig. 5-5 shows the internal distribution in a time slot with these cycles.

Physical time for internal execution of an instruction amounts to 5 cycles, excluding loading time for data bytes and commands coming from the microprocessor.

This time can be increased by 8 cycles if the instruction execution is not complete before the beginning of the block of 8 cycles reserved for internal operations.

Moreover, if instruction 6 is activated, all other instructions will be processed after instruction 6 has been completed or, at the latest, at the beginning of the new frame.

By activating instruction 1 (Connection/Disconnection) between a given input channel C_{IN} and an output channel C_{OUT}, the byte transferred to C_{OUT} corresponds to the byte taken from C_{IN} in the same or the preceding frame, based on the relative position of C_{OUT} with respect to C_{IN}.

In particular, if the number of C_{OUT} channels (NC_{OUT}) is greater than or equal to two units as compared with the number of C_{IN} channels (NC_{IN}), the connection occurs in the same frame.

6. APPLICATIONS

EXCHANGE NETWORK

The M3488 device was designed to be used as a basic element in large-scale switching systems, with up to 65536 connections.

An example of a structure which could be used for this purpose is shown in fig. 6-1, which shows that a system of 64 K users (2048 PCM links, each having 32 channels) is made up of eight central modules, each with a capacity equal to 8 K connections (256 PCM links, each having 32 channels) and of (256 + 256) M3488 peripherals.

Fig. 6-2 shows the internal organization of a central module with 8 K connections.

It should be noted that it is made up of eight switching units, each with a capacity equal to 1 K connections (32 PCM links, each having 32 channels) and of (32 + 32) M3488 peripherals.

Figure 5.5 : The Division within Each Time Slot Between the Time Reserved for Internal Processing and That Reserved for the Execution of Commands Supplied by the Microprocessor.

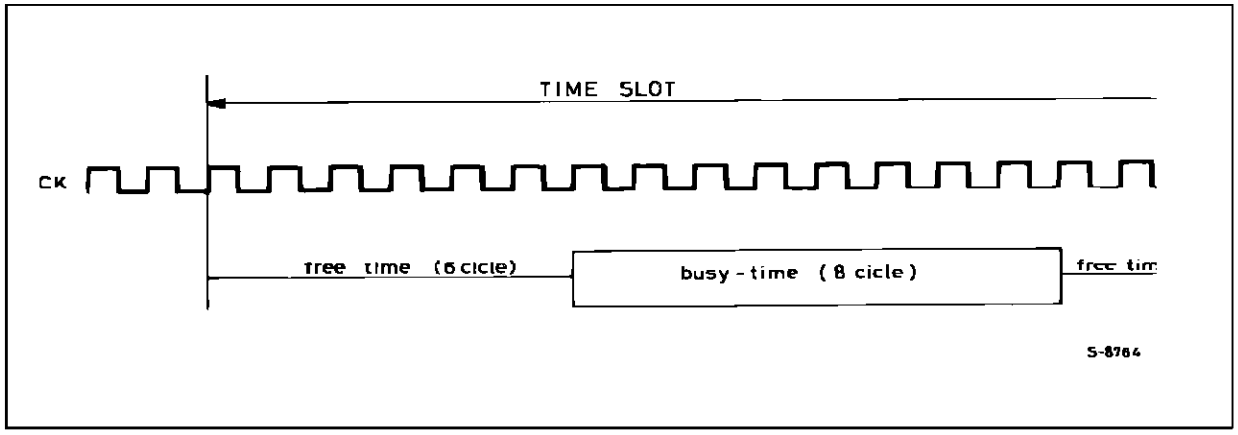


Figure 6.1 : Simplified Block Diagram of a Switching Matrix with 65536 Channels Concentrated in 2048 PCM Links at 2048 Kbit/s Each.

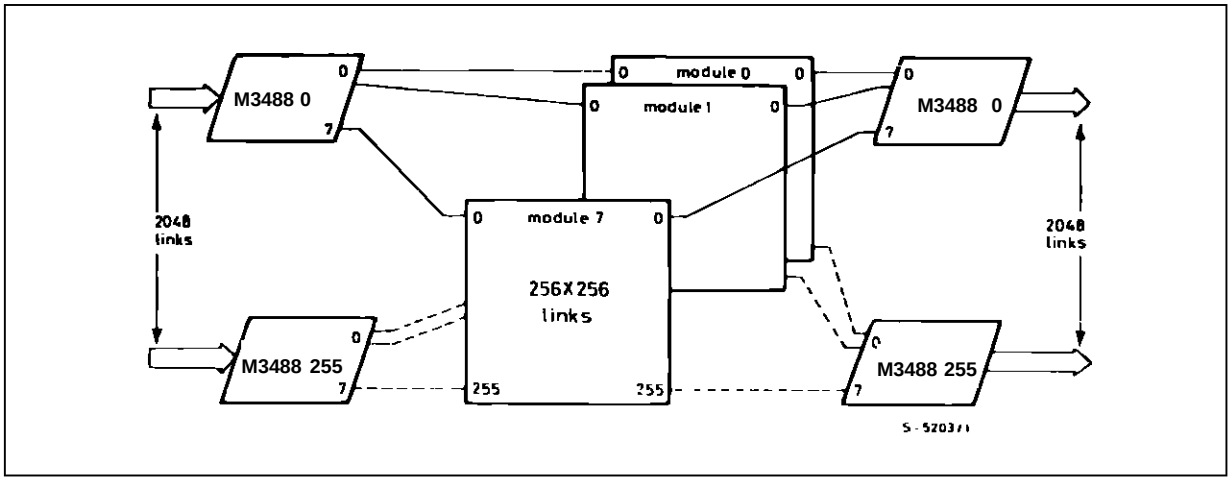
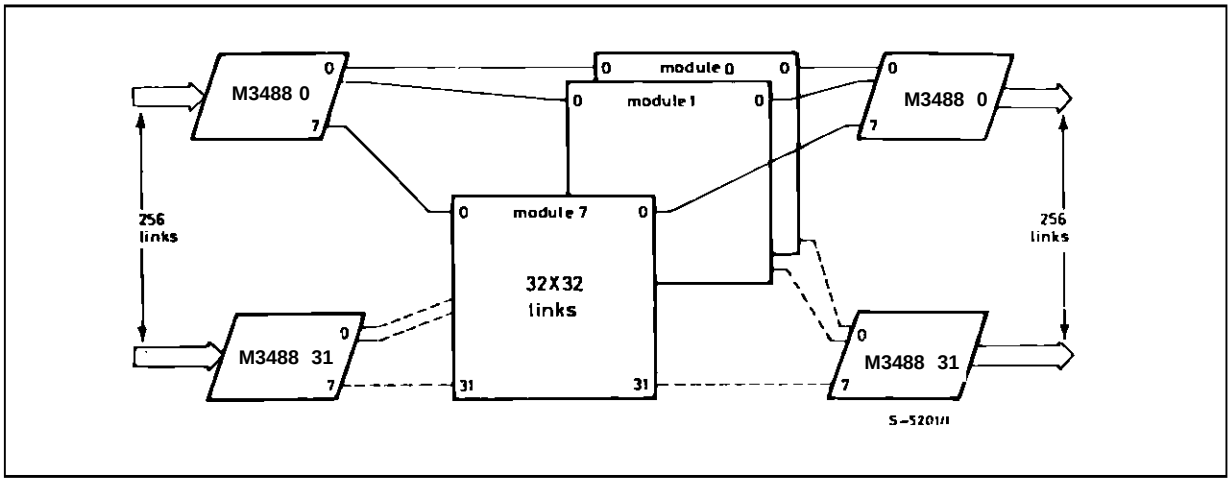


Figure 6.2 : Simplified Block Diagram of a Switching Module Four 8192 Channels Concentrated Into 256 PCM Links at 2048 Kbits/s.



The internal structure of a switching unit with 1K connections is shown in fig. 6.3.

It is made up of 16 M3488s organized in a square matrix (multi–chip matrix).

It is important to stop, finally, with this last structure, insofar as it could, without any variation, be used as a PABX switching matrix, up to 1000 lines.

The 1000 lines, or, more precisely, 1024, are concentrated in 32 PCM flows at 2048 Kbit/s.

All 16 M3488s have microprocessor interface signals in common (D7 to D0, RD, WR, C/D, RESET), as well as CK, SYNC and selection pins A1, A2 and CS2.

Also, all 4 M3488s belonging to the same column have the same output channels in common and all 4 M3488s belonging to the same row have the same input channels. When the microprocessor needs to execute an operation on a certain output channel C_{OUT}, the relevant M3488 column is chosen from among the chip select signals CS10, CS11, CS12 and CS13.

Thus, the microprocessor transmits the relevant bytes which, obviously, are received by all the M3488s of the matrix.

However, only one of these M3488s should execute the instruction.

The single M3488 which should execute the function request is the one in which pins S1 and S2 have been connected to V_{CC} and V_{SS} in such a way as to correspond to the signals present, respectively, on the common wires A1 and A2.

Figure 6.3 : Switching Matrix for 1024 Channels Concentrated Into 32 Links at 2048 Kbits/s.

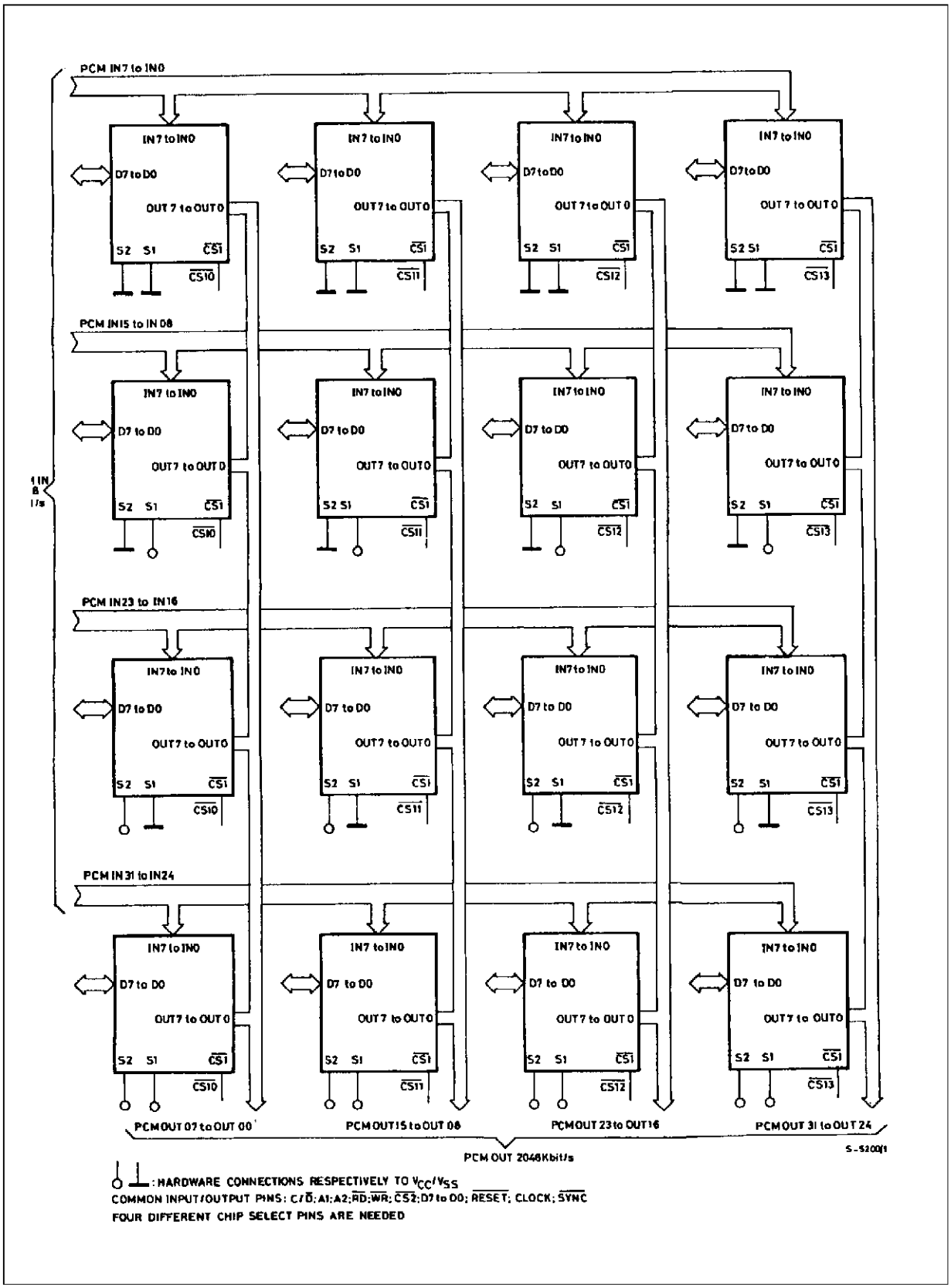


Figure 6.4 : Switching Matrix for 512 Channels Concentrated Into 16 PCM Links at 2048 Kbits/s.

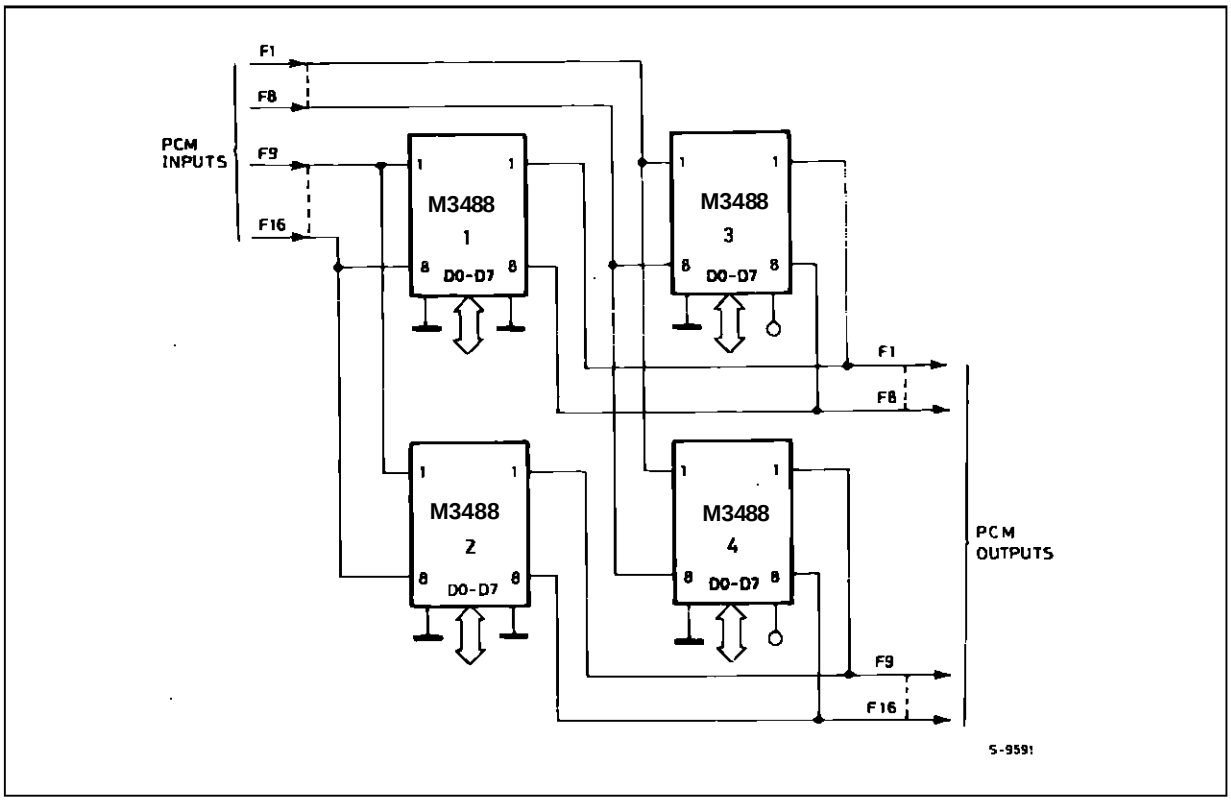
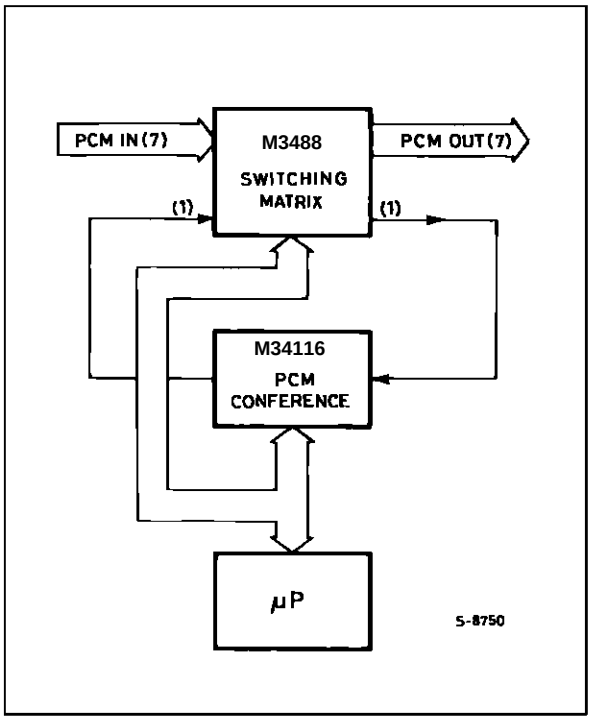


Figure 6.5 : Typical M3488-M34116-µP Configuration. One Output Stream of the M3488 are Connected to the M34116 and Dedicated to the Conference Function.



The other M3488s in the column selected recognize that, even though having to do with an operation of a channel under their control, this operation must be carried out by another M3488 in their column and they act on this basis.

In the case of instructions 1 and 3, they carry out a disconnection from the relevant output channel C_{OUT}, instruction 5 is unaffected and instructions 2, 4 and 6 are not executed.

*Bus reading only takes place on M3488 in match condition (A1 = S1, A2 = S2).

This fact greatly simplifies the controlling software of the matrix insofar as, when a new connectionneeds to be executed or a byte loaded on a certain C_{OUT}, it is possible to ignore the same C_{OUT} disconnection from earlier connections because the disconnection is carried out automatically by the multichip matrix.

PABX

What was explained in the previous paragraph applies to switching systems up to 1024 lines.

The switching matrix for systems up to 512 users is represented in fig. 6-4.

Also, in this case, it is important to demonstrate the great simplification in the control software determined by the use of S1, S2, A1 and A2 for the choice

of M3488 involved in operations.

A single M3488 will suffice for switching system up to 256 channels.

In the sphere of the PABX, regardless of its size, a function currently always in demand is the conference function, that is, the possibility to interconnect several users.

SGS-THOMSON has developped a device for this purpose, called CONFERENCE CALL (M34116), which is used in conjunction with the M3488 to carry out this function.

In addition M34116 is able to generate up to 7 tones +1 Melody simultaneously fully programmable in amplitude, duration and frequencies saving all the circuitry normally dedicated to tone generation inside a PABX.

Fig. 6-5 demonstrates this application.

The M34116 is also controlled by an 8-bit microprocessor, and, therefore, has been given a parallel interface for the microprocessor, using characteristics exactly the same as those available in the M3488.

In order to carry out a conference operation, it is essential to reserve a PCM output and input in the matrix, for which, when using a single M3488, switching capacity decreases to (224 x 224) users. With a single M34116, it is possible to carry out from 1 to 29 conferences simultaneously, with the only limitation being that the total number of users involved in the conferences must be less than 32 ; fig. 6-6 illustrates this aspect.

With reference to fig. 6-7, in which the case of three users in conference is examined, we can see which phases are required to bring about a conference :

1) the channels to use for the conference (A, B and C, in the example) are allocated in any channel position of the reserved PCM bus. The operation is carried out by the M3488.
2) the supplementary channels are added together, in other words, the contents of channel B arereplaced by the sum of channels (A and C) etc. This is carried out by the M34116. These sum signals are loaded in the reserved PCM output bus.
3) the sum signal are withdrawn from the reserved PCM bus and switched into the relevant output channels. This operation is carried out by the M3488.

It is also possible to use the M34116 in a multi-chip switching matrix - see fig. 6-8 - or use more than one M34116 in the same matrix - see fig. 6-9.

Figure 6.6 : With a Single M34116 It is Possible to Realize from 1 to 29 Independent Conferences with a Total of up to 32 Channels Conferenced.

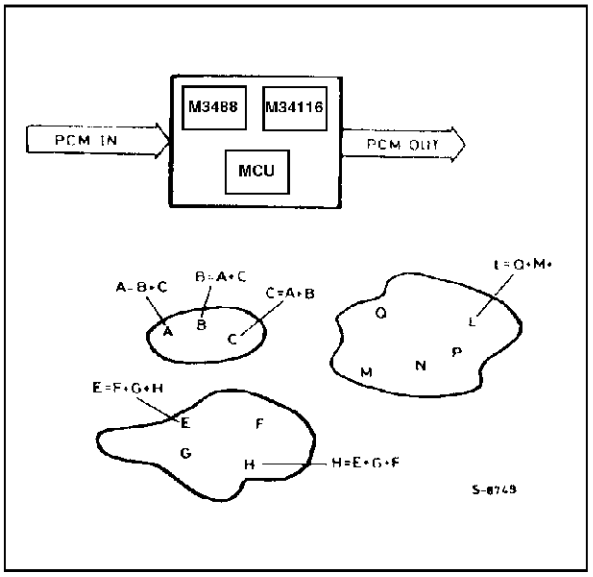


Figure 6.7 : Example of a conference with three channels ; A, B and C.

1) The M3488 allocated A, B and C to the PCM stream applied to the M34116.
2) The M34116 processes the channels A, B and C, returning to the outputs B+C, A+C and A+B respectively.
3) The M3488 allocates the signals B+C, A+C and A+B, to the outputs corresponding to the time slots of the channels A, B & C.

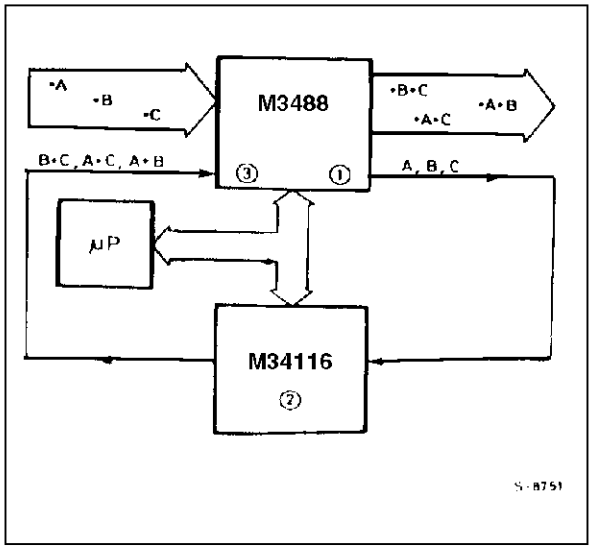


Figure 6.8 : The M34116 Can Also Been Used in Multichip Matrices.

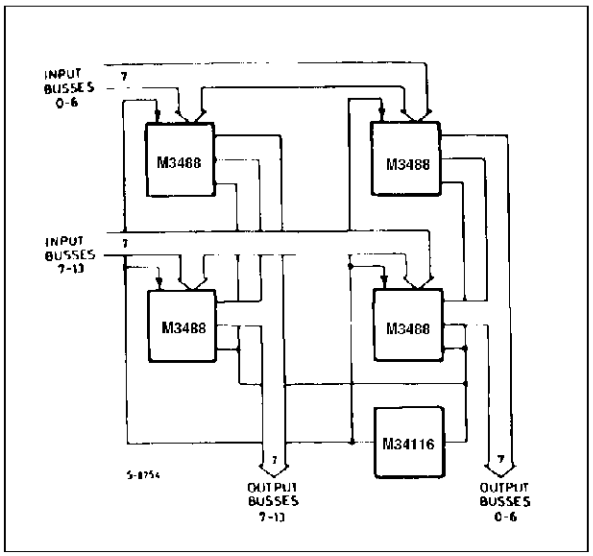
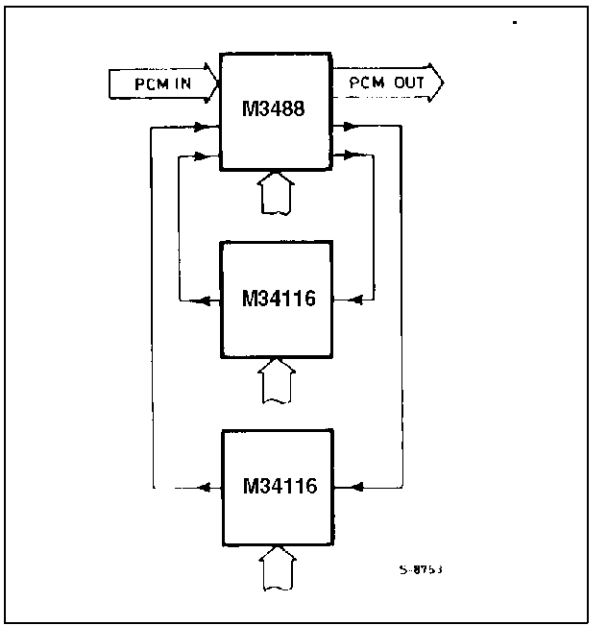


Figure 6.9 : More Than One M34116 May be Added to Each Matrix to Increase the Number fo Conferences (10 per device).



For more detailed information see the M34116 datasheet.

Finally, it is interesting to note how the M34116, on its own, can be used with other types of switching matrixes ; however, two considerations lead to recommending its use with the M3488 ;

a) M34116 PCM signal timing and microprocessor interface are exactly the same as those of the M3488 ;

b) the command format that the microprocessor sends to the M34116 to program the different operations is the same as the one used to program the M3488.

To sum up, by using the M34116 with the M3488, complete compatibility is obtained, both with hardware and software, between switching matrices and the M34116.

M3488 WITH LESS PCM LINKS THAN 32 CHANNELS

It is also possible to use M3488 when the PCM frames are made up of a number of channels other than 32.

Suppose that the PCM frames are made up of N-Channels, which will be numbered from 0 to (N-1).

Each PCM frame will thus be made up of a number of bits multiplied by 8 ; this exactly equal to (N · 8).

Also, in this case, it is necessary to respect the timing relationship between the different signals shown on the data sheet ; in particular, a relationship is always carefully made between the rising edge of SYNC and the first clock (CK) bit contained in the slot time for bit 0 of channel 0.

In order to use M3488 with these frames, it is sufficient, using the data bytes sent by the microprocessor, to modify the numbering of a few channels.

In particular :

a) in all instructions in which reference is made to the input channel (N-1), the number 31 should be substituted for the number (N-1) ;

b) in all instructions in which reference is made to the output channel 0, the number N should be substituted for the number 0.

These variations can be made insofar as the M3488 is internally programmed to execute the different operations using 32 channels.

In particular, during the time slot which corresponds to the last channel of the frame, channel (N-1), the M3488 loads the bits corresponding to the next channel to be output in the next slot time into its registers.

We consider this last channel to be channel 0, but for the M3488 it is Channel N ; indeed, the M3488 draws the bits that it will successively output from the corresponding cells of Channel-N.

Likewise, during the general time slot X, M3488 loads the PCM input frame bits corresponding to channel X ; simultaneously, it memorizes the bits loaded in the previous time slot into the Speech Memory (SM) memory location corresponding to channel (X-1).

Therefore, during the time slot corresponding to channel 0, M3488 memorizes the bits received in the previous time slot, which we consider to be channel (N-1), in the SM memory locations corresponding to channel 31.

For whoever wishes to connect the input channel (N-1) to any output channel, the same channel's PCM samples will be drawn from locations reserved for channel 31.

M3488 WITH THE NORTH AMERICAN PCM STANDARD

The operation of the M3488 with PCM frames using the North American standard can be considered a special case of the operating mode described in the previous paragraph.

The only variable in this case is the presence in each frame of an auxiliary bit (bit X), for which the total number of bits in a frame is :

(24 channels . 8 bits) + 1 bit = 193 bits/frame

As in the preceding case, in alteration in the numbering of the canals is introduced, in particular, the number 23 is replaced by the number 31 in every case in which reference is made to the last channel of the PCM input frame, and in every case where reference is made to output channel 0, the number 0 is replaced by the number 24.

Also, the signals for synchronization ($\overline{SYNC}$) and for clock (CK) are modified as shown in fig. 6-10.

In particular, the rising edge of the $\overline{SYNC}$ signal must appear in bit X's bit time (the 193rd of the PCM input frame). The single variation in the timing of this signal as far as the MCK and CK signals is concerned in that the minimum time for t_{WH} $\overline{SYNC}$ high level width must be from 1 t_{CK} to 3 t_{CK} and thus with (3 . 324) ns = 972ns.

The clock (CK) signal to be applied to the M3488 (pin 6) must be frozen for two clock periods during bit X's bit time. A scheme which is recommended for obtain CK beginning from the MCK and $\overline{SYNC}$ signals is shown in fig. 6-11.

The signal bits located in the PCM input frames are ignored, while, in the corresponding positions of the PCM output frames, they assume the same logical values of the 0 bits of channel 0.

If you use the M3488 with an M34116 the scheme recommended of fig. 6.11 is not necessary. In fact the "frozen clock" is provide by M34116 itself (pin EC).

Therefore is enough to connect pin EC of M34116 to pin CK of M3488. Of course the $\overline{SYNC}$ signal must be the same as shown in Fig. 6.10 and must be connect both to M3488 and M34116.

DATA FLOW SWITCHING

A very simple, but very important, application of the M3488 is that of using it to switch PCM or other high speed data links.

To enable this function, it suffices to switch all relevant input channels to their preselected output channels.

The data rate of these data flows can have any value less that the maximum permissible velocity (2048 Kbit/s).

Obviously, the CK frequency must be the double of the data rate chosen, while the SYNC frequency must be included between 1/16 and 1/256 of the same data rate.

Figure 6.10 : Timing of the CLOCK, $\overline{SYNC}$ and PCM IN Signals for 1544 Kbit/s PCM Streams. At the 193 rd Bit (bit X) the CLOCK Signal applied to the M3488 is frozen for two Periods.

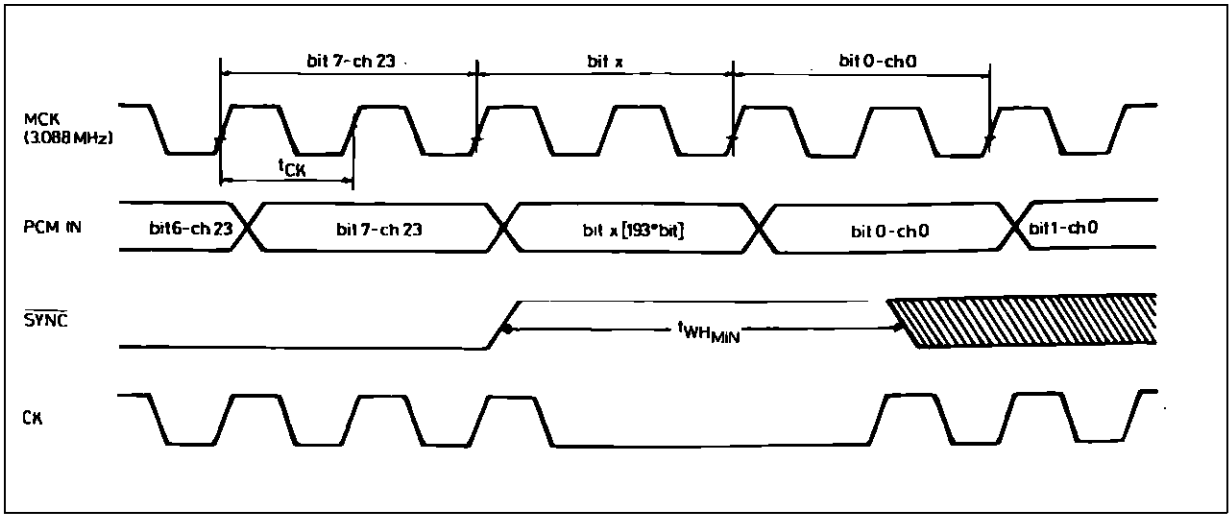
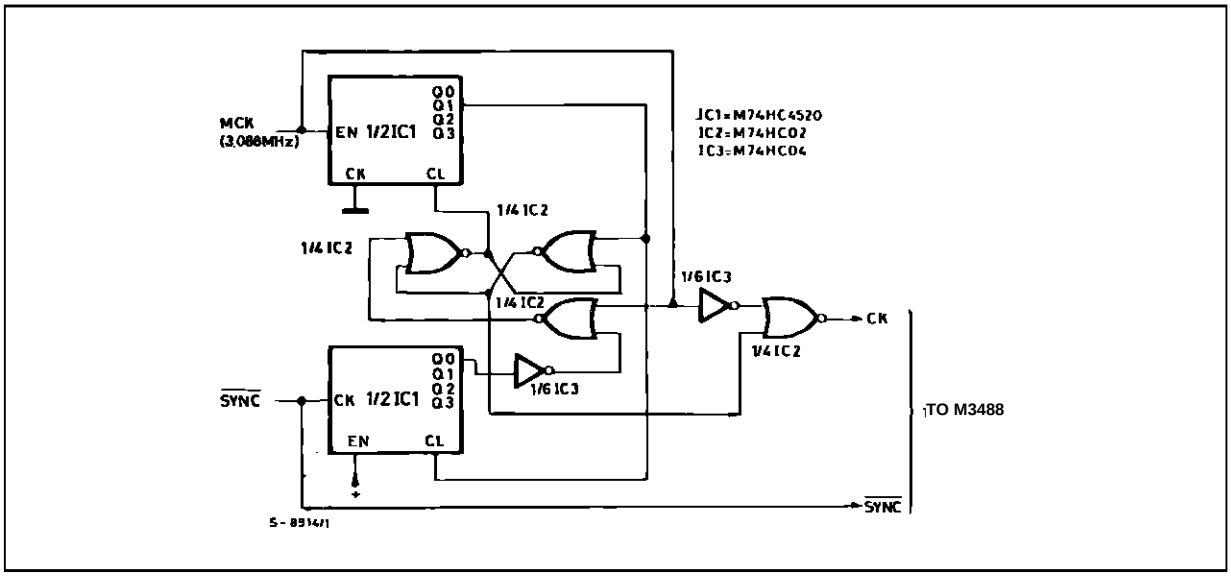


Figure 6.11 : Auxiliary Circuit to use the M3488 with 1544 Kbits/s PCM Streams. This Circuit is not necessary if the M3488 is used with an M34116.



It is particularly interesting, in this application, to demonstrate a characteristic of the M3488 which has already been mentioned and, therefore, of the fact that the device accepts that a certain delay can exist between one data flow and another.

The absolute value of the maximum acceptable delay is not constant, but depends on the velocity of the data flow ; in any case, it is always greater than 80 % of bit time.

This obviously means that when the data flows are not generated internally, but come from peripheral devices located at different distances - See fig. 6-12- within certain limits, it is not necessary to equalize the delays caused by variable arrival times.

RS232 C/V-24 DATA INTERFACE SWITCHING

One of the alternative fields for possible use of the M3488 is that of DATA COMMUNICATIONS.

Fig. 6-13 presents the block diagram of one of the possible applications : a device which allows for switching between the V-24 interface of four DTEs and the V-24 of four DCEs.

As is well known, the RS232 C/V-24 is one of the most common connection interfaces between Data Terminal Equipment (DTE), i.e., computers and terminals, and Data Communication Equipment (DCE), i.e., modems, etc.

Figure 6.12 : Structure of a PABX with Peripheral Concentration Blocks. Note That the CE-PP Connections are PCM Links.

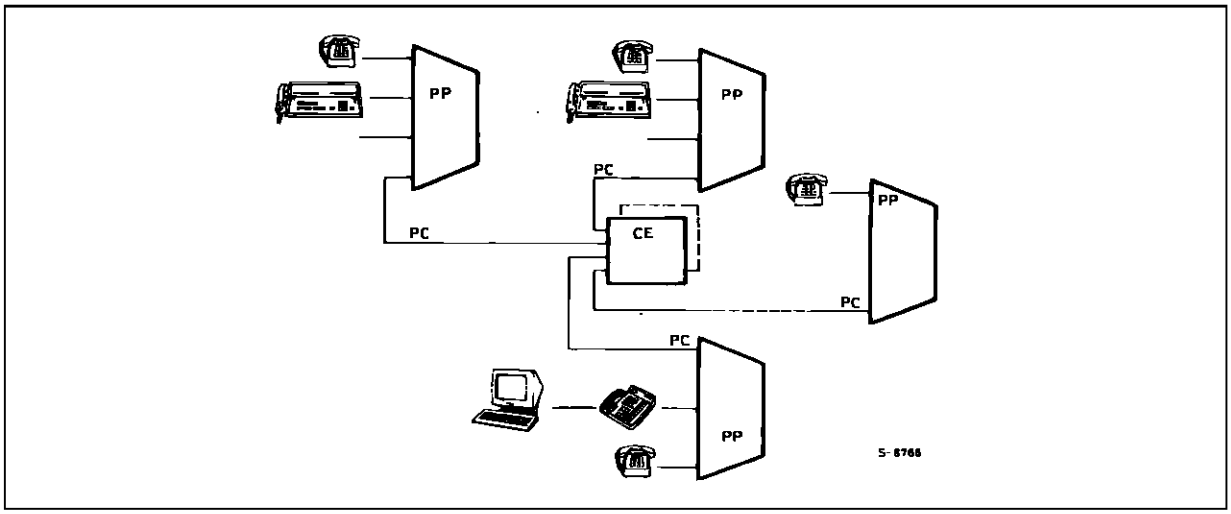
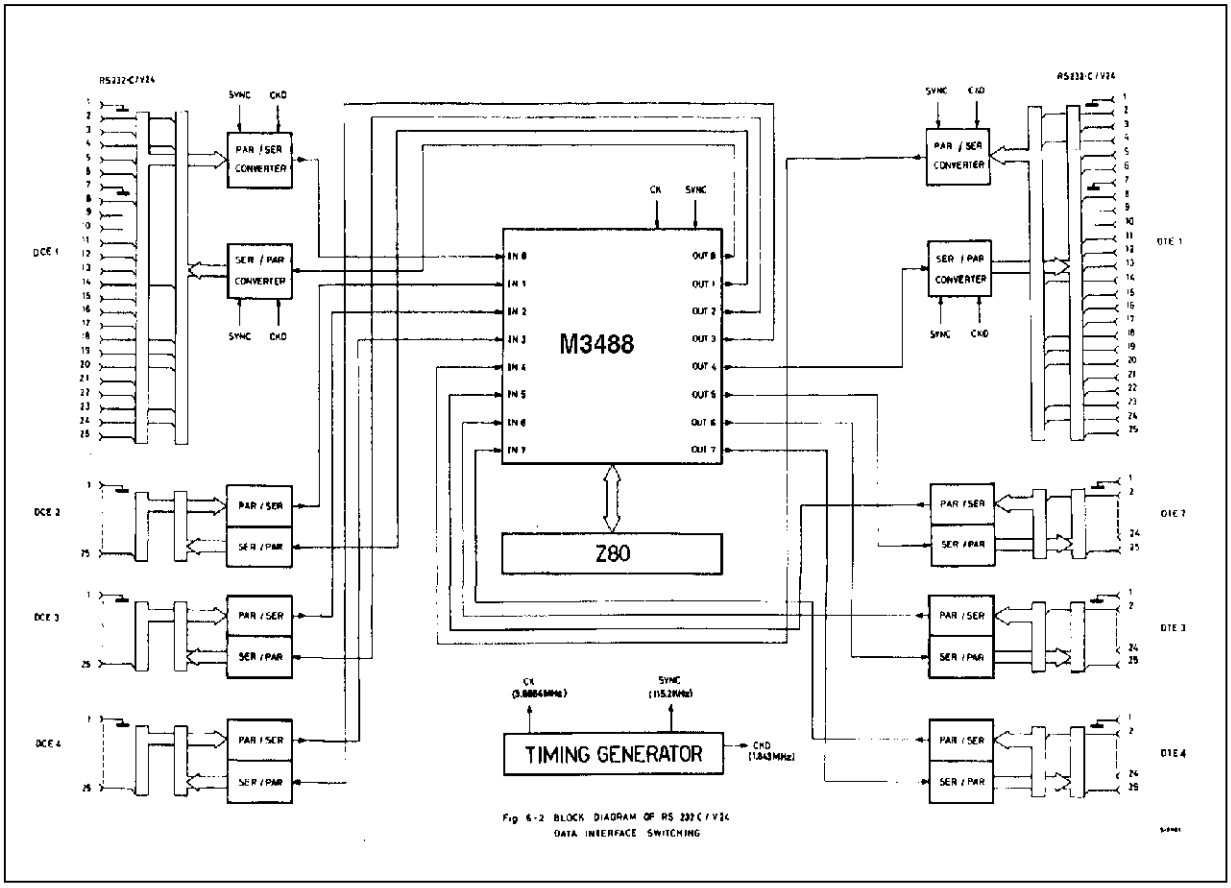


Figure 6.13 : Switching Matrix for Parallel Data Interfaces (eg : RS232C/V24). Signals from the Parallel Interfaces are Serialized, Switched and Parallelized.



The table in fig. 6-14 presents the names of 25 distinct pins which determine the interface and the direction of the same signals (13 DCE → DTE and 8 DTE → DCE).

The basic idea of the device is to sample, using a frequency of 115.2 KHz, the 21 usable interface signals, serialized at a velocity of 1843.2 Kbit/s, and send or receive them through the switching matrix exactly as if they were PCM streams.

In the case of interfaces coming from DCE, of the 21 usable signals, 13 are signals inputting the device, and 8 outputting it, thus it is necessary to run a parallel/serial conversion on the first, and obviously, serial/parallel on the second.

For reasons of simplicity in the serialization phase for the 13 bits, three bits are added so that every sampling period (8.7 µs) will amount to exactly two octets ; in the parallel/serial conversion phase, the three additional bits are disregarded.

Concerning the DTE, the discussion is similar, with the obvious exception of the fact that the signals undergoing serial/parallel conversion are 13 and those which undergoing parallel/serial conversion are 8.

To these last 8 bits should be added, for the same reasons mentioned before, 8 bits so that, during each sampling period, exactly 16 bits are serialized.

An input and an output made available by the M3488 are reserved for each interface.

The M3488 views the data streams which are entering exactly if they were PCM frames at 1843 Kbit/s.

In this case, the difference is that the number of channels used is only two, thus each two octets require that the M3488 internal channel counter be reset to zero.

This is obtained simply by raising the frequency of the SYNC signal from the usual 8 KHz to 115.2 Khz, in other words, to use as SYNC the same signal used to sample the interfaces (see fig. 6-13).

Wanting, for example, to switch the V-24 from DCE1 to that of DTE4 is sufficient through the microprocessor sending to the M3488 instructions for connecting channels 0 and 1 of input 0 with channels 0 and 1 of output 7, channels 0 and 1 of input 7 with 0 and 1 of output 0.

Figure 6.14 : RS-232-C/V. 24 Data Interface Connector Pin Assignements.

Pin	Circuit EIA	Circuit CCITT	SIGNAL NAME	Direction DTE — DCE
1	AA	101	Protective Ground	→
2	BA	103	Transmitted Data	→
3	BB	104	Received Data	←
4	CA	105	Request to Send	→
5	CB	106	Clear to Send	←
6	CC	107	Data Set Ready	←
7	AB	102	Signal Ground (Common Return)	↔
8	CF	109	Received Line Signal Detector	←
9			Unassigned	
10			Unassigned	
11		126	Select Tx Frequency	←
12	SCF	122	Secondary Received Line Signal Detector	←
13	SCB	121	Secondary Clear to Send	←
14	SBA	118	Secondary Transmitted Data	→
15	DB	114	Transmit Signal Element Timing (DCE Source)	←
16	SBB	119	Secondary Received Data	←
17	DD	115	Receiver Signal Element Timing (DCE Source)	←
18		141	Local Loopback	→
19	SCA	120	Secondary Request to Send	→
20	CD	108/2	Data Terminal Ready	→
21	CG	110	Signal Quality Detector	←
22	CE	125	Ring Indicator	←
23	CH	111	Data Signal Rate Selector (DTE Source)	→
24	DA	113	Transmit Signal Element Timing (DTE Source)	→
25		142	Test Indicator	←

Obviously, it is possible to carry out simultaneously all four connections in any combination.

Using M3488 instead of standard analog cross-point besides switching, you can also implement addition functions as monitoring or programming by µP the status of the interfaces using the instruction 3 and 4 of the M3488 itself.

Using more M3488s extends at will the number of interfaces thus switchable due to their subdivision between DTE and DCE V-24s.

Finally, there are no limits to the use of this system for switching other interface types.

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