N-Channel Enhancement Mode MOSFET General Purpose Amplifier Switch

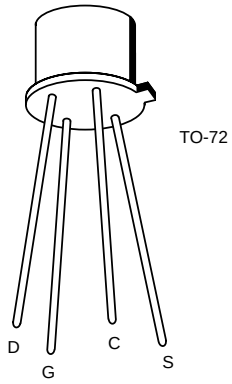
calogic CORPORATION

IT1750

FEATURES

- **Low ON Resistance**
- **Low C_{dg}**
- **High Gain**
- **Low Threshold Voltage**

PIN CONFIGURATION



1003

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Drain-Source and Gate-Source Voltage 25V
Peak Gate-Source Voltage (Note 1) . . . . . ±125V
Drain Current 100mA
Storage Temperature Range . . . . . -65°C to +200°C
Operating Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Power Dissipation 375mW
Derate above 25°C . . . . . 3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
IT1750	Hermetic TO-72	-55°C to +150°C
XIT1750	Sorted Chips in Carriers	-55°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Body connected to Source and V_{BS} = 0 unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$V_{GS(th)}$	Gate to Source Threshold Voltage	0.50	3.0	V	V_{DS} = V_{GS}, I_D = 10µA
I_{DSS}	Drain Leakage Current		10	nA	V_{DS} = 10V, V_{GS} = 0
I_{GSS}	Gate Leakage Current	(See note 2)			
BV_{DSS}	Drain Breakdown Voltage	25		V	I_D = 10µA, V_{GS} = 0
$r_{DS(on)}$	Drain to Source on Resistance		50	ohms	V_{GS} = 20V
$I_{D(on)}$	Drain Current	10		mA	V_{DS} = V_{GS} =10V
Y_{fs}	Forward Transadmittance	3,000		µS	V_{DS} = 10V, I_D = 10mA, f = 1kHz
C_{iss}	Total Gate Input Capacitance		6.0	pF	I_D = 10mA, V_{DS} = 10V, f = 1MHz (Note 3)
C_{dg}	Gate to Drain Capacitance		1.6	pF	V_{DG} = 10V, f = 1MHz (Note 3)

NOTES: **1.** Devices must not be tested at ±125V more than once nor longer than 300ms.
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.
3. For design reference only, not 100% tested.