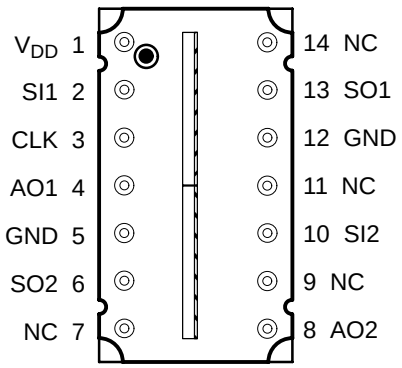
- **128 × 1 Sensor-Element Organization**
- **200 Dots-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Uniformity**
- **Wide Dynamic Range . . . 2000:1 (66 dB)**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 5 MHz**
- **Single 5-V Supply**
- **Replacement for TSL202**

(TOP VIEW)



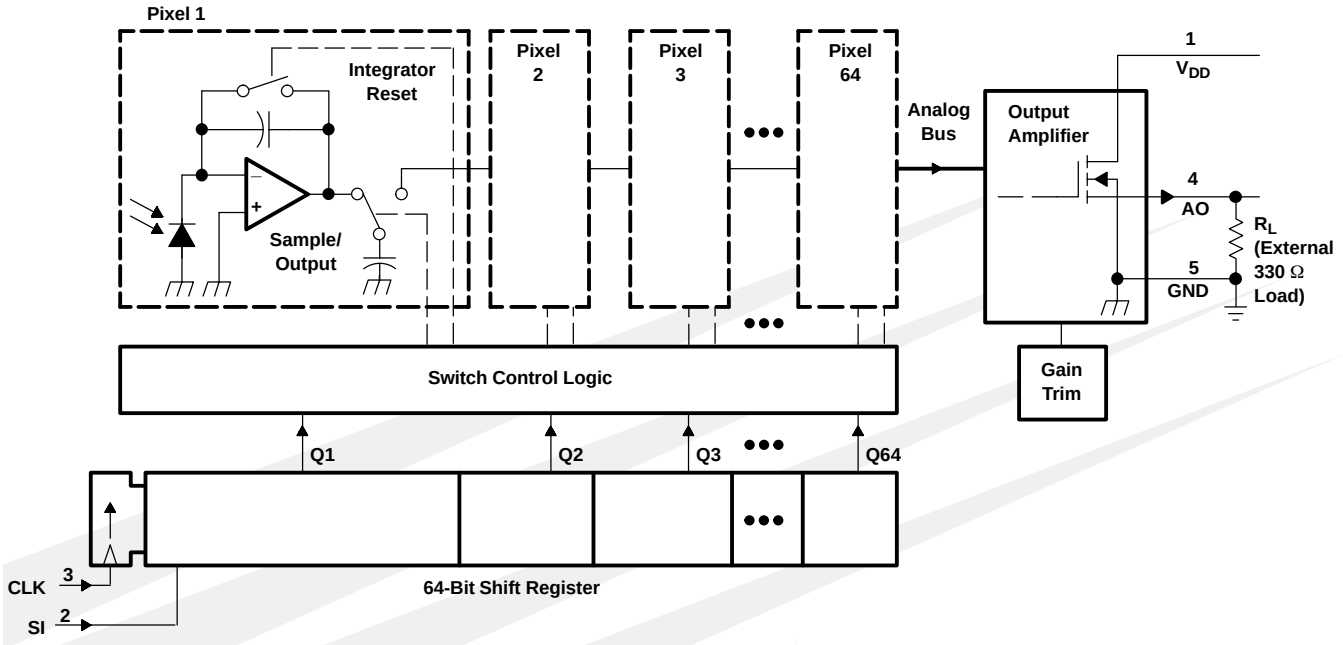
NC – No internal connection

Description

The TSL202R linear sensor array consists of two sections of 64 photodiodes and associated charge amplifier circuitry arranged to form a contiguous 128 × 1 array. The pixels measure 120 µm (H) by 70 µm (W) with 125-µm center-to-center spacing and 55-µm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

The TSL202R is intended for use in a wide variety of applications including mark detection and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning as well as optical linear and rotary encoding.

Functional Block Diagram (each section — pin numbers apply to section 1)



Texas Advanced Optoelectronic Solutions Inc.
800 Jupiter Road, Suite 205 • Plano, TX 75074 • (972) 673-0759
www.taosinc.com

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO1	4	Analog output of section 1
AO2	8	Analog output of section 2
CLK	3	Clock. Clk controls charge transfer, pixel output, and reset.
GND	5,12	Ground (substrate). All voltages are referenced to GND.
NC	7, 9, 11, 14	No internal connection
SI1	2	Serial input (section 1). SI1 defines the start of the data-out sequence.
SI2	10	Serial input (section 2). SI2 defines the start of the data-out sequence.
SO1	13	Serial output (section 1). SO1 provides a signal to drive the SI2 input.
SO2	6	Serial output (section 2). SO2 provides a signal to drive the SI input of another device for cascading or as an end-of-data indication.
V_{DD}	1	Supply voltage. Supply voltage for both analog and digital circuitry.

Detailed Description

The sensor consists of 128 photodiodes arranged in a linear array. Light energy impinging on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel. During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time. The integration time is the interval between two consecutive output periods.

The output and reset of the integrators is controlled by a 128-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI for one positive going clock edge (see Figures1 and 2)†. As the SI pulse is clocked through the 128-bit shift register, the charge on the sampling capacitor of each pixel is sequentially connected to a charge-coupled output amplifier that generates a voltage output, AO. When the bit position goes low, the pixel integrator is reset. On the 129th clock rising edge, the SI pulse is clocked out of the shift register and the output assumes a high-impedance state. Note that this 129th clock pulse is required to terminate the output of the 128th pixel and return the internal logic to a known state. A subsequent SI pulse can be presented as early as the 130th clock pulse, thereby initiating another pixel output cycle.

The voltage developed at analog output (AO) is given by:

$$V_{out} = V_{drk} + (R_e)\ (E_e)\ (t_{int})$$

where:

- V_{out} is the analog output voltage for white condition
- V_{drk} is the analog output voltage for dark condition
- R_e is the device responsivity for a given wavelength of light given in V/(μJ/cm^2)
- E_e is the incident irradiance in μW/cm^2
- t_{int} is integration time in seconds

AO is driven by a source follower that requires an external pulldown resistor (330-Ω typical). The output is nominally 0 V for no light input, 2 V for normal white-level, and 3.4 V for saturation light level. When the device is not in the output phase, AO is in a high impedance state.

A 0.1 μF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

† For proper operation, after meeting the minimum hold time condition, SI must go low before the next rising edge of the clock.

Absolute Maximum Ratings†

Supply voltage range, V_{DD} . . . . . –0.3 V to 6 V
Input voltage range, V_I . . . . . –0.3 V to V_{DD} + 0.3V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) . . . . . –20 mA to 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) . . . . . –25 mA to 25 mA
Voltage range applied to any output in the high impedance or
power-off state, V_O . . . . . –0.3 V to V_{DD} + 0.3V
Continuous output current, I_O (V_O = 0 to V_{DD}) . . . . . –25 mA to 25 mA
Continuous current through V_{DD} or GND . . . . . –40 mA to 40 mA
Analog output current range, I_O . . . . . –25 mA to 25 mA
Operating free-air temperature range, T_A . . . . . –25°C to 85°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		5000	kHz
Sensor integration time, serial, t_{int}	0.026		100	ms
Sensor integration time, parallel, t_{int}	0.013		100	ms
Operating free-air temperature, T_A	0		70	°C
Load resistance, R_L	300		4700	Ω
Load capacitance, C_L			420	pF

Electrical Characteristics at f_{clock} = 1 MHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 640 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 16.5 μW/cm² (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{out}	Analog output voltage (white, average over 128 pixels)	See Note 1	1.6	2	2.4	V
V_{drk}	Analog output voltage (dark, average over 128 pixels)		0	50	150	mV
PRNU	Pixel response nonuniformity	See Notes 2 & 3		±4%	±10%	
	Nonlinearity of analog output voltage	See Note 3		±0.4%		FS
	Output noise voltage	See Note 4		1		mVrms
R_e	Responsivity		18	23	30	V/(μJ/cm²)
SE	Saturation exposure	See Note 5		142		nJ/cm²
V_{sat}	Analog output saturation voltage		2.5	3.4		V
DSNU	Dark signal nonuniformity	All pixels See Note 6		25	120	mV
IL	Image lag	See Note 7		0.5%		
I_{DD}	Supply current, output idle			5	8	mA
I_{IH}	High-level input current	$V_I = V_{DD}$			10	μA
I_{IL}	Low-level input current	V_I = 0			10	μA
V_{OH}	High-level output voltage, SO1 and SO2	I_O = 50 μA	4.5	4.95		V
		I_O = 4 mA		4.6		
V_{OL}	Low-level output voltage, SO1 and SO2	I_O = 50 μA		0.01	0.1	V
		I_O = 4 mA		0.4		
$C_{i(SI)}$	Input capacitance, SI			5		pF
$C_{i(CLK)}$	Input capacitance, CLK			10		pF

NOTES:
1. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640 nm.
2. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated at the white irradiance level. PRNU includes DSNU.
3. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
4. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
5. Minimum saturation exposure is calculated using the minimum V_{sat}, the maximum V_{drk}, and the maximum R_e.
6. DSNU is the difference between the maximum and minimum output voltage in the absence of illumination.
7. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{out\ (IL)} - V_{drk}}{V_{out\ (white)} - V_{drk}} \times 100$$

Timing Requirements (see Figure 1 and Figure 2)

		MIN	NOM	MAX	UNIT
$t_{su(SI)}$	Setup time, serial input (see Note 8)	20			ns
$t_{h(SI)}$	Hold time, serial input (see Note 8 and Note 9)	0			ns
t_w	Pulse duration, clock high or low	50			ns
t_r, t_f	Input transition (rise and fall) time	0		500	ns

NOTES:
8. Input pulses have the following characteristics: t_r = 6 ns, t_f = 6 ns.
9. SI must go low before the rising edge of the next clock pulse.

Dynamic Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 10 pF		185		ns
$t_{pd(SO)}$	Propagation delay time, SO1, SO2			50		ns

TYPICAL CHARACTERISTICS

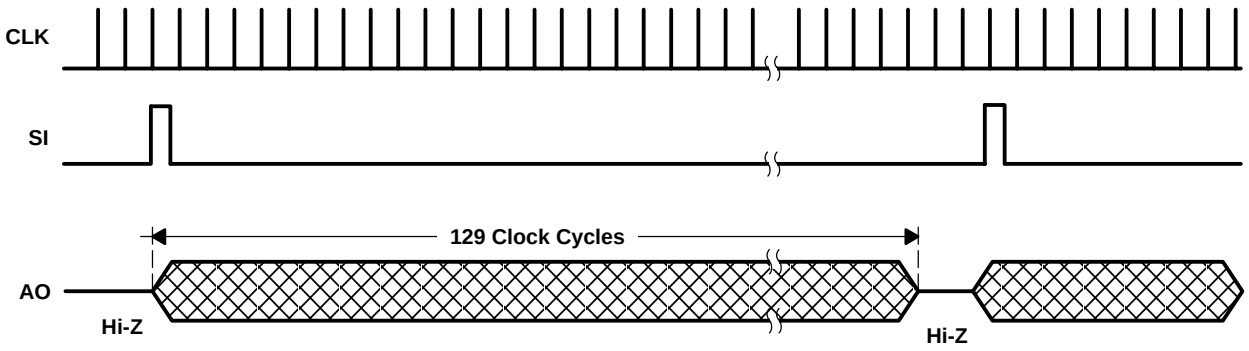


Figure 1. Timing Waveforms

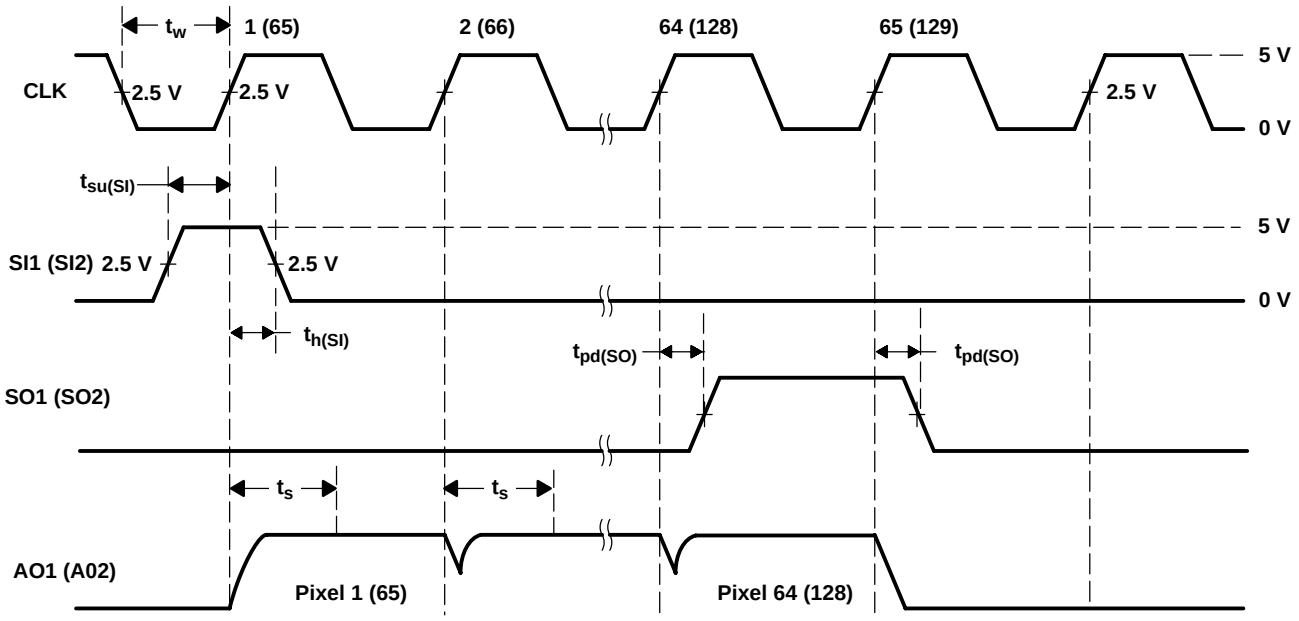


Figure 2. Operational Waveforms (each section)

TYPICAL CHARACTERISTICS

PHOTODIODE SPECTRAL RESPONSIVITY

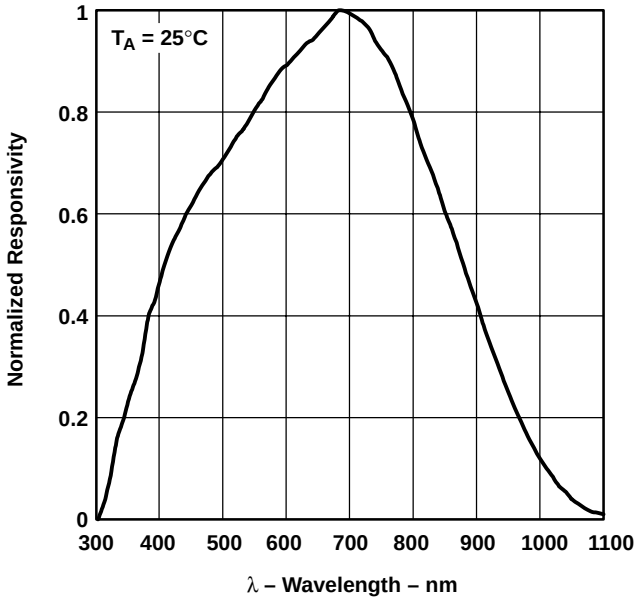


Figure 3

ANALOG OUTPUT SETTLING TIME vs LOAD CAPACITANCE AND RESISTANCE

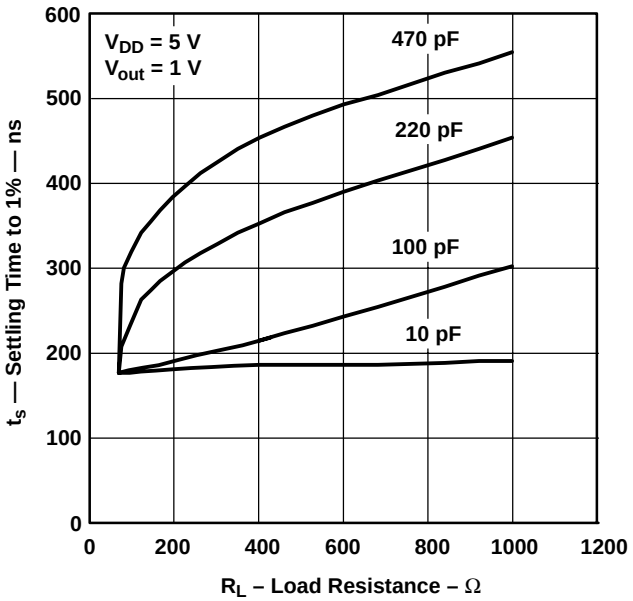


Figure 4

APPLICATION INFORMATION

Power Supply Considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01-μF to 0.1-μF capacitor with short leads mounted close to the device package (see Figure 5 and Figure 6).

Connection Diagrams

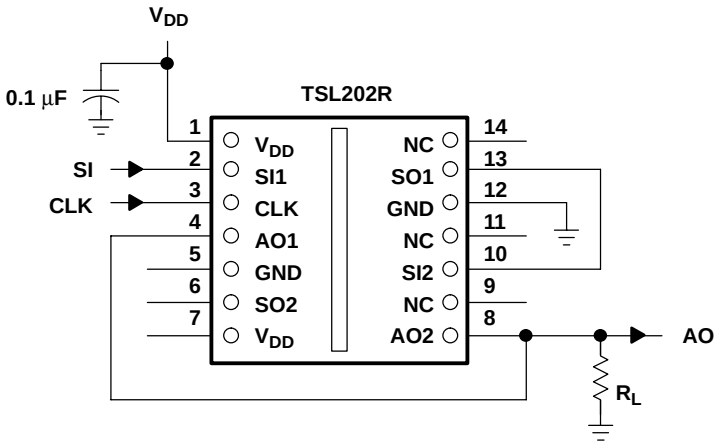


Figure 5. Serial Connection

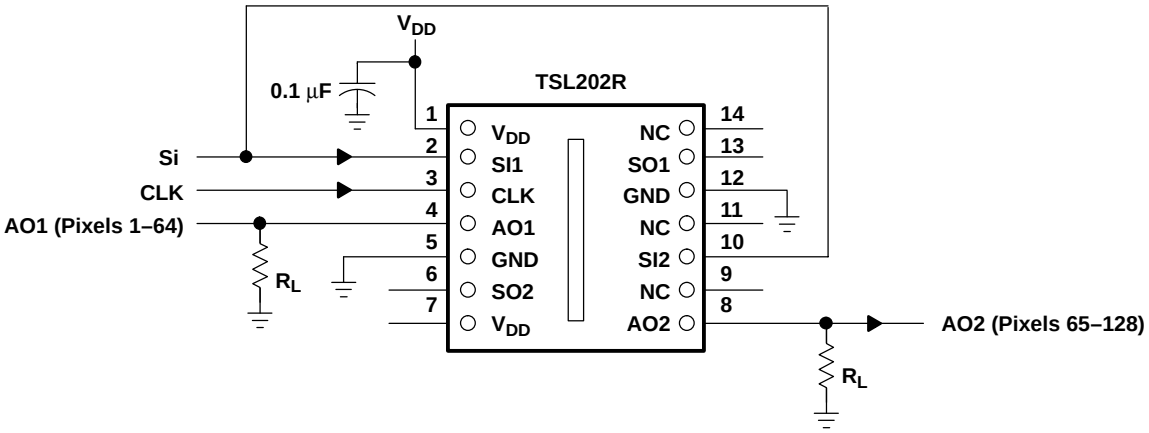
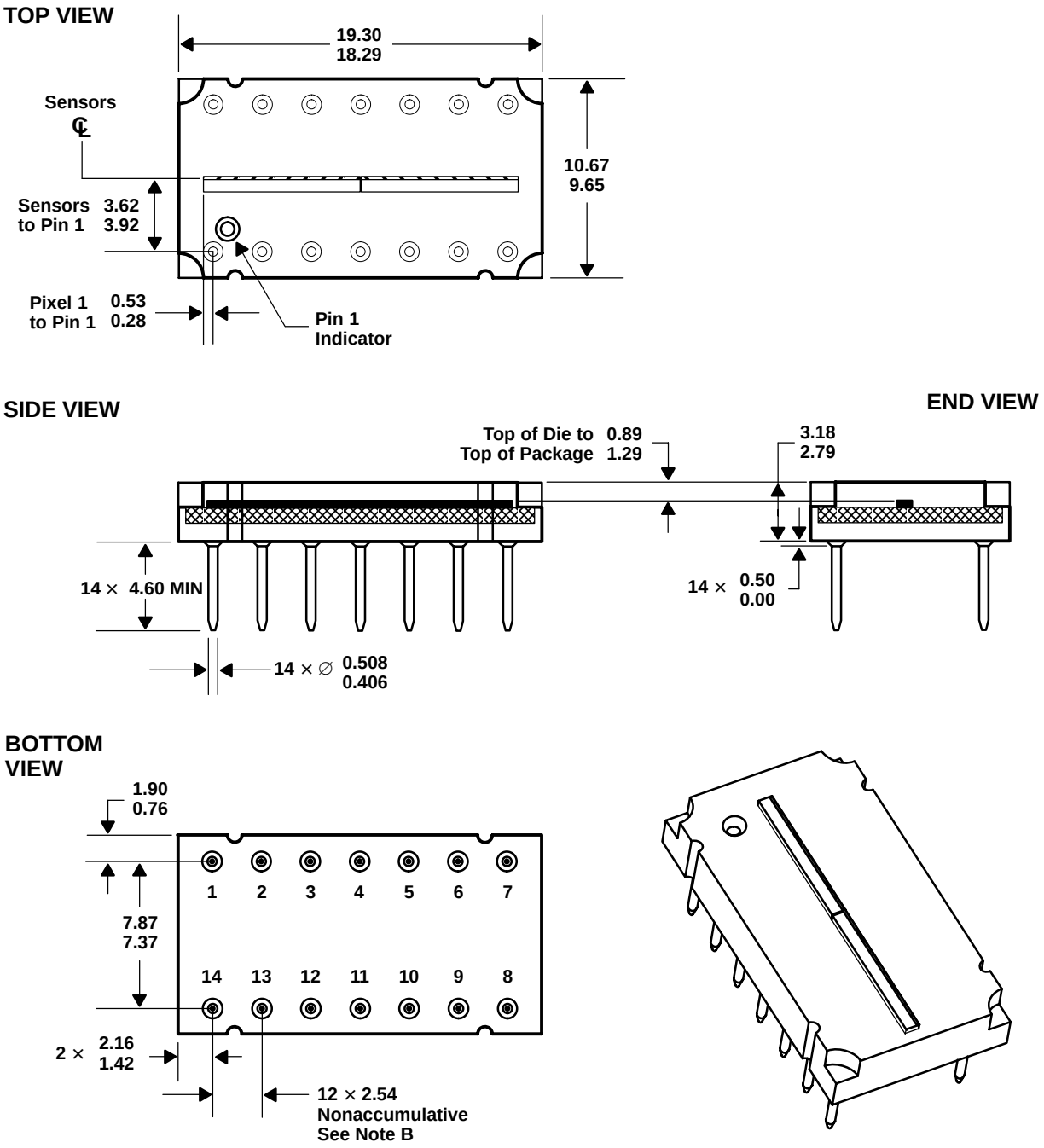


Figure 6. Parallel Connection

MECHANICAL INFORMATION

This assembly consists of 2 sensor chips mounted on a printed-circuit board in a clear molded plastic package.



NOTES: A. All linear dimensions are in millimeters.
B. The true-position spacing is 2.54 mm between lead centerlines. Each pin centerline is located within 0.25 mm of its true longitudinal positions.
C. Index of refraction of clear plastic is 1.52.
D. This drawing is subject to change without notice.

Figure 7. Packaging Configuration

PRODUCTION DATA — information in this document is current at publication date. Products conform to specifications in accordance with the terms of Texas Advanced Optoelectronic Solutions, Inc. standard warranty. Production processing does not necessarily include testing of all parameters.

NOTICE

Texas Advanced Optoelectronic Solutions, Inc. (TAOS) reserves the right to make changes to the products contained in this document to improve performance or for any other purpose, or to discontinue them without notice. Customers are advised to contact TAOS to obtain the latest product information before placing orders or designing TAOS products into systems.

TAOS assumes no responsibility for the use of any products or circuits described in this document or customer product design, conveys no license, either expressed or implied, under any patent or other right, and makes no representation that the circuits are free of patent infringement. TAOS further makes no claim as to the suitability of its products for any particular purpose, nor does TAOS assume any liability arising out of the use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages.

TEXAS ADVANCED OPTOELECTRONIC SOLUTIONS, INC. PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN CRITICAL APPLICATIONS IN WHICH THE FAILURE OR MALFUNCTION OF THE TAOS PRODUCT MAY RESULT IN PERSONAL INJURY OR DEATH. USE OF TAOS PRODUCTS IN LIFE SUPPORT SYSTEMS IS EXPRESSLY UNAUTHORIZED AND ANY SUCH USE BY A CUSTOMER IS COMPLETELY AT THE CUSTOMER'S RISK.