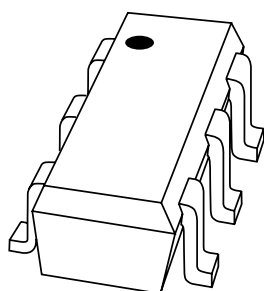


# DATA SHEET



**PESD3V3L5UY; PESD5V0L5UY**  
Low capacitance 5-fold ESD  
protection diode arrays in SOT363  
package

Product specification

2004 Mar 23

# Low capacitance 5-fold ESD protection diode arrays in SOT363 package

# PESD3V3L5UY; PESD5V0L5UY

**FEATURES**

- Uni-directional ESD protection of up to five lines
- Bi-directional ESD protection of up to four lines
- Low diode capacitance
- Maximum peak pulse power:  $P_{pp} = 25\text{ W}$  at  $t_p = 8/20\ \mu\text{s}$
- Low clamping voltage:  $V_{CL(R)} = 12\text{ V}$  at  $I_{pp} = 2.5\text{ A}$
- Ultra low leakage current:  $I_{RM} = 8\text{ nA}$  at  $V_{RWM} = 5\text{ V}$
- ESD protection > 20 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge);  $I_{pp} = 2.5\text{ A}$  at  $T_p = 8/20\ \mu\text{s}$ .

**APPLICATIONS**

- Cellular handsets and accessories
- Portable electronics
- Computers and peripherals
- Communications systems
- Audio and video equipment.

**DESCRIPTION**

Low capacitance 5-fold ESD protection array in the very small SOT363 plastic package designed to protect up to five transmission or data lines from the damage caused by Electrostatic Discharge (ESD).

**MARKING**

TYPE NUMBER	MARKING CODE <sup>(1)</sup>
PESD3V3L5UY	*K3
PESD5V0L5UY	*K4

**Note**

1. \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.  
\* = W: Made in China.

**ORDERING INFORMATION**

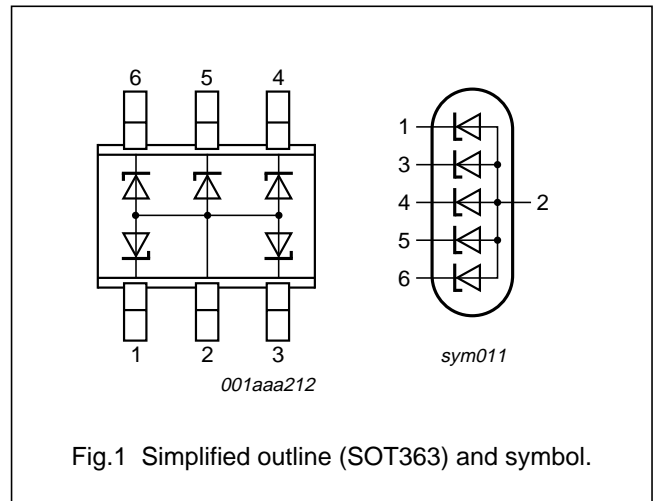
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PESD3V3L5UY	–	plastic surface mounted package; 6 leads	SOT363
PESD5V0L5UY	–	plastic surface mounted package; 6 leads	SOT363

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	VALUE	UNIT
$V_{RWM}$	reverse standoff voltage		
	PESD3V3L5UY	3.3	V
	PESD5V0L5UY	5	V
$C_d$	diode capacitance		
	PESD3V3L5UY	22	pF
	PESD5V0L5UY	16	pF
	number of protected lines	5	

**PINNING**

PIN	DESCRIPTION
1	cathode 1
2	common anode
3	cathode 2
4	cathode 3
5	cathode 4
6	cathode 5



## Low capacitance 5-fold ESD protection diode arrays in SOT363 package

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per diode</b>					
P <sub>pp</sub>	peak pulse power	8/20 μs pulse; notes 1 and 2	–	25	W
I <sub>pp</sub>	peak pulse current	8/20 μs pulse; notes 1 and 2	–	2.5	A
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
T <sub>stg</sub>	storage temperature		–65	+150	°C

### Notes

1. Non-repetitive current pulse 8/20 μs exponentially decaying waveform; see Fig.2.
2. Measured from any of pins 1, 3, 4, 5 or 6 to pin 2.

### ESD maximum ratings

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
<b>Per diode</b>				
ESD	electrostatic discharge capability	IEC 61000-4-2 (contact discharge); notes 1 and 2	20	kV
		HBM MIL-Std 883	10	kV

### Notes

1. Device stressed with ten non-repetitive Electrostatic Discharge (ESD) pulses; see Fig.3.
2. Measured from any of pins 1, 3, 4, 5 or 6 to pin 2.

### ESD standards compliance

ESD STANDARD	CONDITIONS
IEC 61000-4-2, level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
HBM MIL-Std 883, class 3	> 4 kV

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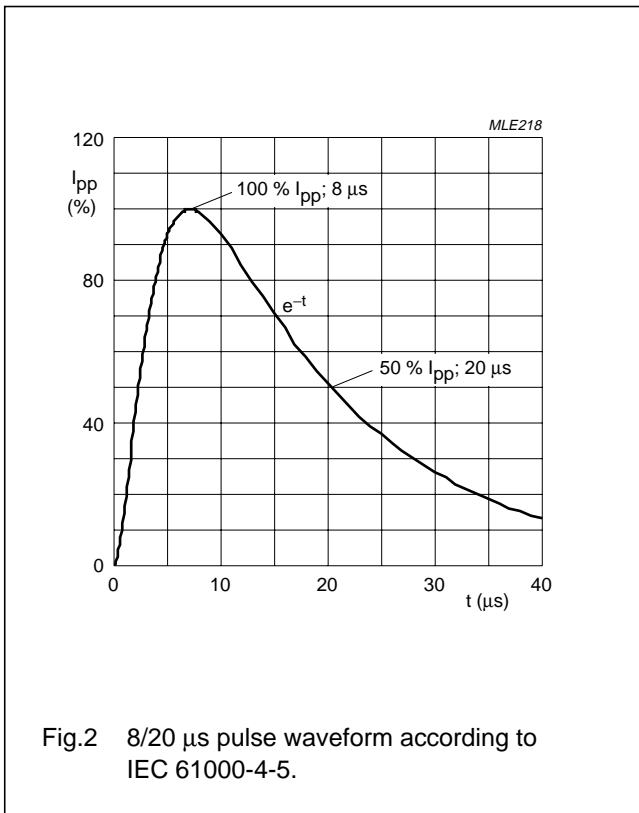


Fig.2 8/20  $\mu$ s pulse waveform according to IEC 61000-4-5.

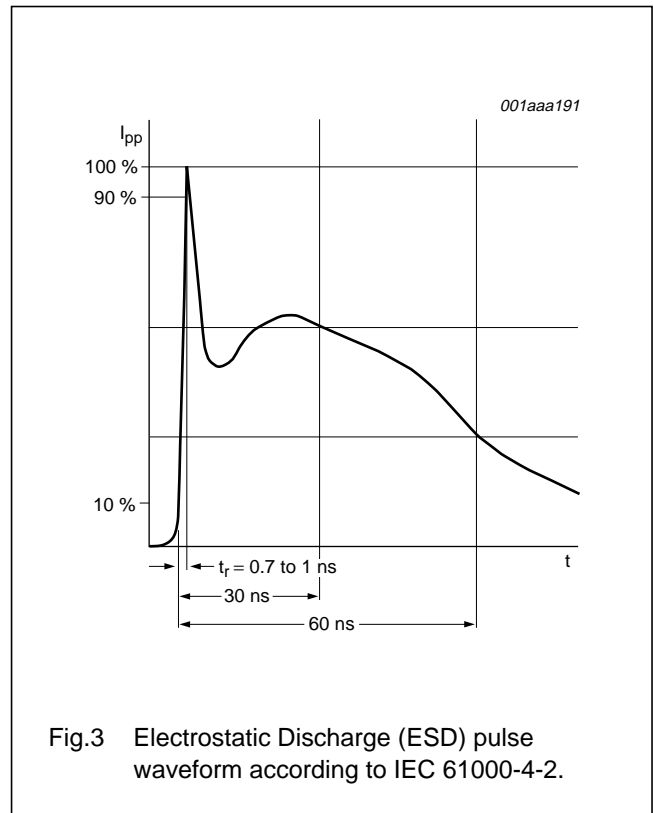


Fig.3 Electrostatic Discharge (ESD) pulse waveform according to IEC 61000-4-2.

Low capacitance 5-fold ESD protection  
diode arrays in SOT363 package

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PESD5V0L5UY

**CHARACTERISTICS**

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per diode</b>						
$V_{RWM}$	reverse stand-off voltage					
	PESD3V3L5UY		–	–	3.3	V
	PESD5V0L5UY		–	–	5	V
$I_{RM}$	reverse leakage current					
	PESD3V3L5UY	$V_{RWM} = 3.3\text{ V}$	–	75	300	nA
	PESD5V0L5UY	$V_{RWM} = 5\text{ V}$	–	5	25	nA
$V_{BR}$	breakdown voltage	$I_Z = 1\text{ mA}$				
	PESD3V3L5UY		5.3	5.6	5.9	V
	PESD5V0L5UY		6.4	6.8	7.2	V
$C_d$	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V};$ see Fig.5				
	PESD3V3L5UY		–	22	28	pF
	PESD5V0L5UY		–	16	19	pF
$V_{CL(R)}$	clamping voltage	notes 1 and 2				
	PESD3V3L5UY	$I_{pp} = 1\text{ A}$	–	–	10	V
		$I_{pp} = 2.5\text{ A}$	–	–	12	V
	PESD5V0L5UY	$I_{pp} = 1\text{ A}$	–	–	10	V
		$I_{pp} = 2.5\text{ A}$	–	–	12	V
$r_{diff}$	differential resistance	$I_R = 1\text{ mA}$				
	PESD3V3L5UY		–	–	200	$\Omega$
	PESD5V0L5UY		–	–	100	$\Omega$

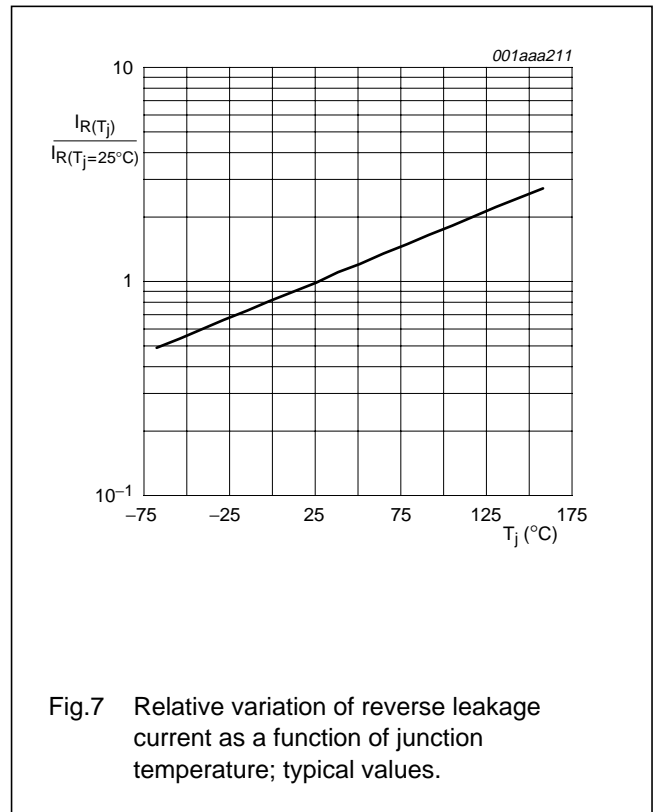
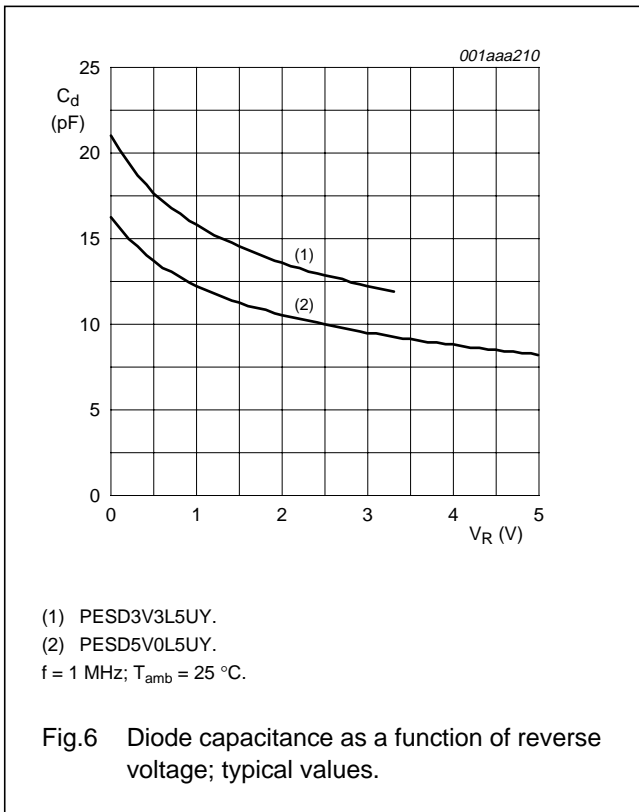
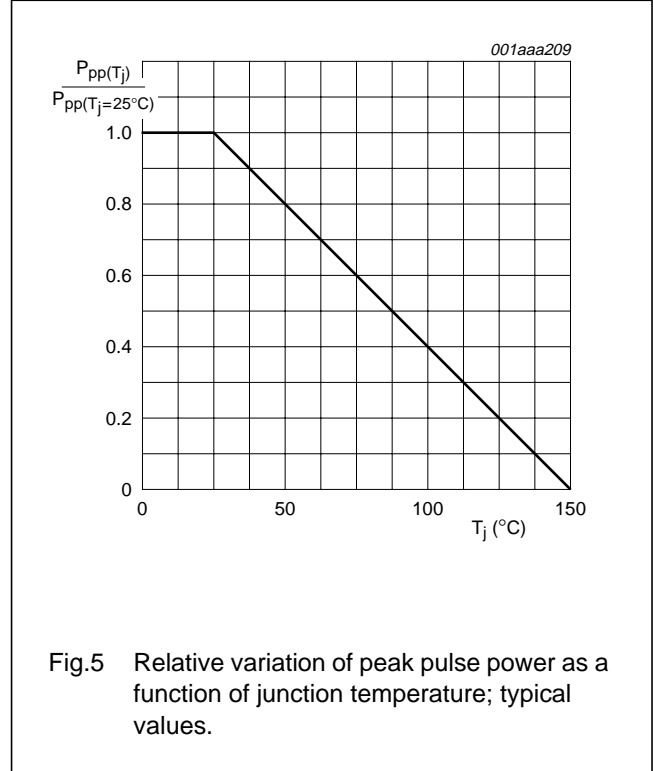
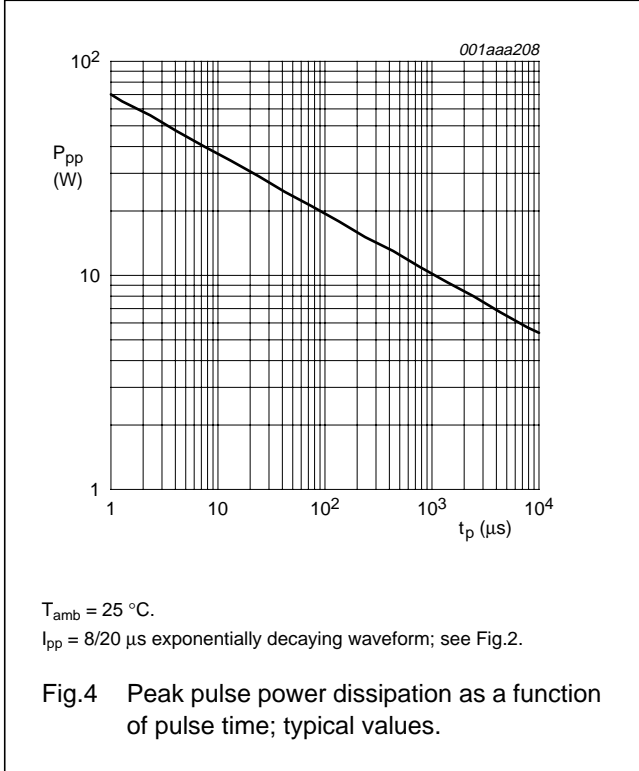
**Notes**

1. Non-repetitive current pulse 8/20  $\mu\text{s}$  exponentially decaying waveform; see Fig.2.
2. Measured from any of pins 1, 3, 4, 5 or 6 to pin 2.

Low capacitance 5-fold ESD protection diode arrays in SOT363 package

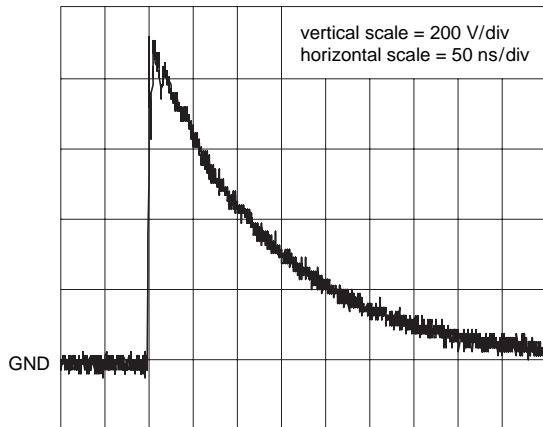
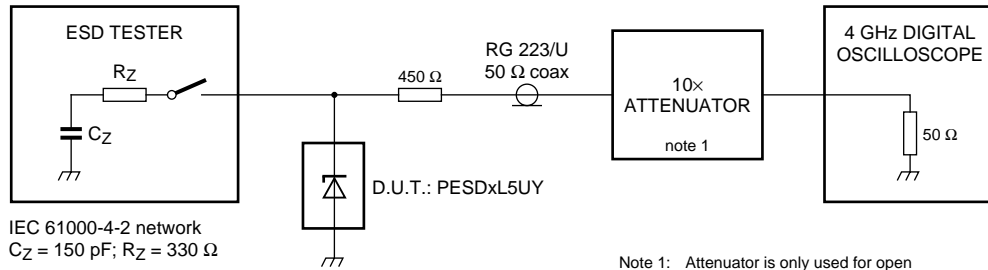
PESD3V3L5UY;  
PESD5V0L5UY

GRAPHICAL DATA

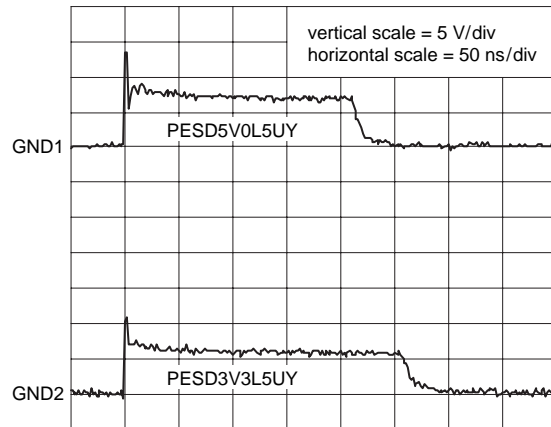


Low capacitance 5-fold ESD protection diode arrays in SOT363 package

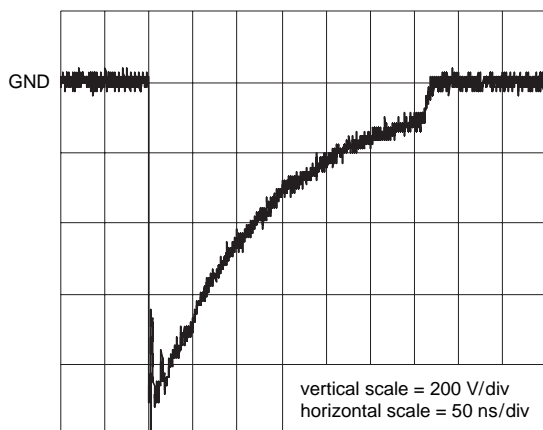
PESD3V3L5UY;  
PESD5V0L5UY



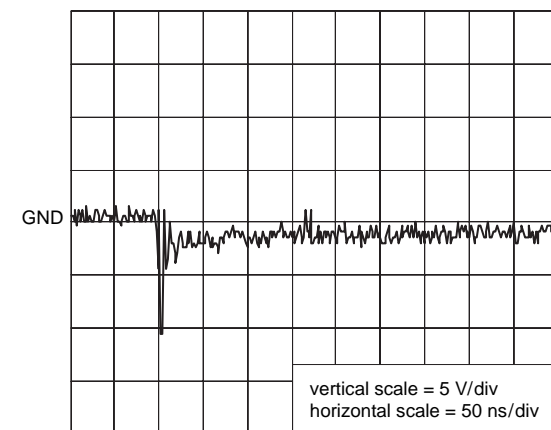
unclamped +1 kV ESD voltage waveform (IEC61000-4-2 network)



clamped +1 kV ESD voltage waveform (IEC61000-4-2 network)



unclamped -1 kV ESD voltage waveform (IEC61000-4-2 network)



clamped -1 kV ESD voltage waveform (IEC61000-4-2 network)

001aaa218

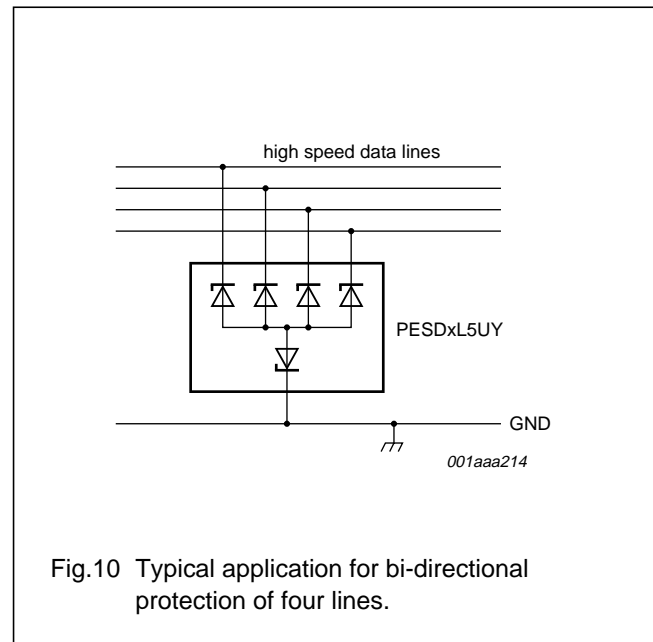
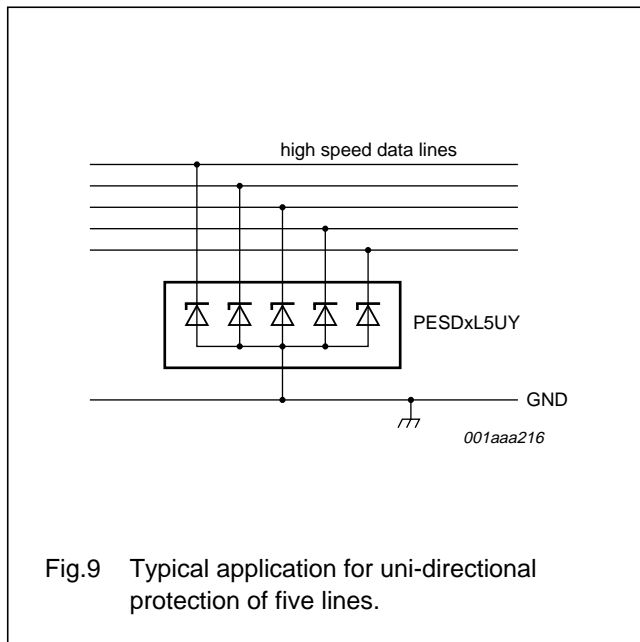
Fig.8 ESD clamping test set-up and waveforms.

## Low capacitance 5-fold ESD protection diode arrays in SOT363 package

PESD3V3L5UY;  
PESD5V0L5UY

### APPLICATION INFORMATION

The PESDxL5UY is designed for the uni-directional protection of up to five lines or bi-directional protection of four lines from the damage caused by Electrostatic Discharge (ESD) and surge pulses. The PESDxL5UY may be used on lines where the signal polarities are above or below ground. PESDxL5UY can withstand and provides protection from a surge of 25 watts peak pulse power per line for a 8/20  $\mu$ s waveform.



### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. The protection device should be placed as closely as possible to the input terminal or connector.
2. The path length between the protection device and the protected line should be as short as possible.
3. Parallel signal paths should be kept to a minimum.
4. Running protection conductors in parallel with unprotected conductor should be avoided.
5. All printed-circuit board conductive loops (including power and group loops) should be kept to a minimum.
6. The length of the transient return path to ground should be kept to a minimum.
7. The use of shared transient return paths to a common ground point should be avoided.
8. Ground planes should be used whenever possible.
9. For multilayer printed-circuit boards, ground vias should be used.



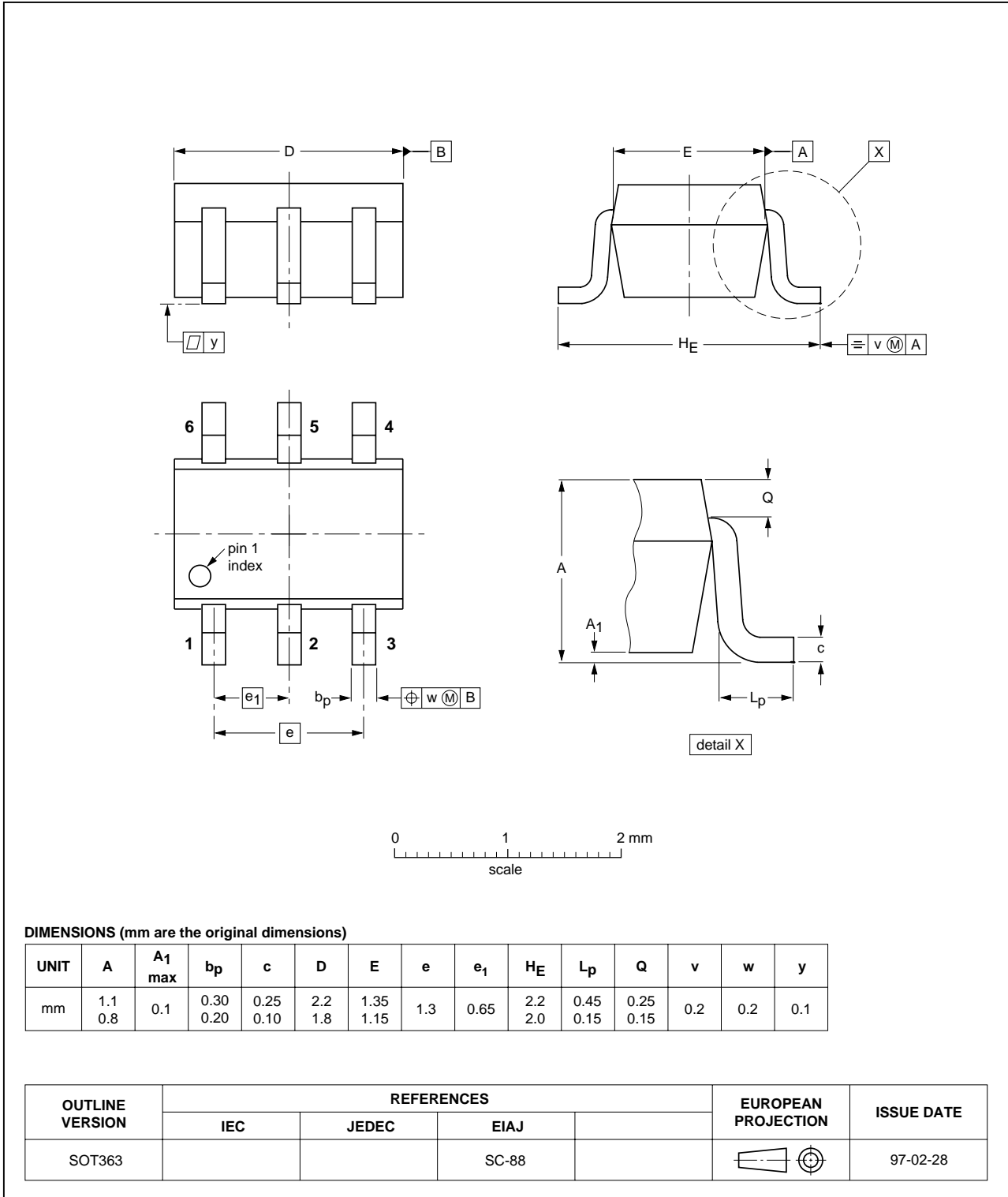
Low capacitance 5-fold ESD protection  
diode arrays in SOT363 package

PESD3V3L5UY;  
PESD5V0L5UY

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



## Low capacitance 5-fold ESD protection diode arrays in SOT363 package

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PESD5V0L5UY

### DATA SHEET STATUS

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Printed in The Netherlands

R76/01/pp11

Date of release: 2004 Mar 23

Document order number: 9397 750 12255

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