# 64×240 dots DG06243 (Built-in controller) 1/64 Duty

SANYO SEMICONDUCTOR CORP

This dot matrix module has a controller that allows 40 characters by 8 lines on 64 dots by 240 dots of graphics to be displayed. It provides the control circuits such as data RAM, character ROM. It can be interfaced with a CPU through an 8-bit bidirectional data bus and connected directly to 80-series CPU.

## Mechanical characteristics

| Parameter | Dimensions | unit |
|---|---|---|
| Out line | 180.0 (W)×65.0 (H)×13.0(T) | mm |
| Min. viewing area | 132.5 (W)×39.5 (H) | mm |
| Dot display area | 127.15(W)×33.87(H) | mm |
| Dot size | 0.48(W)× 0.48(H) | mm |
| Dot pitch | 0.53(W)× 0.53(H) | mm |
| Weight | 105(approximately) | g |

## Absolute maximum ratings

| Parameter | Symbol | min. | max. | unit |
|---|---|---|---|---|
| Logic supply voltage | $V_{DD}-V_{SS}$ | −0.3 | 7.0 | V |
| LCD supply voltage | $V_{DD}-V_O$ | −0.3 | 20.0 | V |
| Input voltage | $V_I$ | −0.3 | $V_{DD}+0.3$ | V |
| Operating temperature | $T_{opg}$ | 0 | +50 | °C |
| Storage temperature | $T_{stg}$ | −20 | +70 | °C |

## Electrical characteristics (Ta=25°C, $V_{DD}=5.0\pm0.25V$)

| Parameter | Symbol | Condition | min. | typ. | max. | unit |
|---|---|---|---|---|---|---|
| Input high-level voltage | $V_{IH}$ | Input pin | $V_{DD}-2.2$ | − | $V_{DD}$ | V |
| Input low-level voltage | $V_{IL}$ | | 0 | − | 0.8 | V |
| LCD drive voltage | $V_O$ | − | − | 14.0 | − | V |
| Oscillation frequency | $f_{OSC}$ | − | − | 4.0 | − | MHz |
| Supply current | $I_{DD}$ | $V_{DD}-V_{SS}=5.0V$ | − | 15.0 | 25.0 | mA |
| LCD supply current | $I_{EE}$ | $V_{DD}=V_O=14.0V$ | − | 1.0 | 4.0 | mA |

## Pin functions

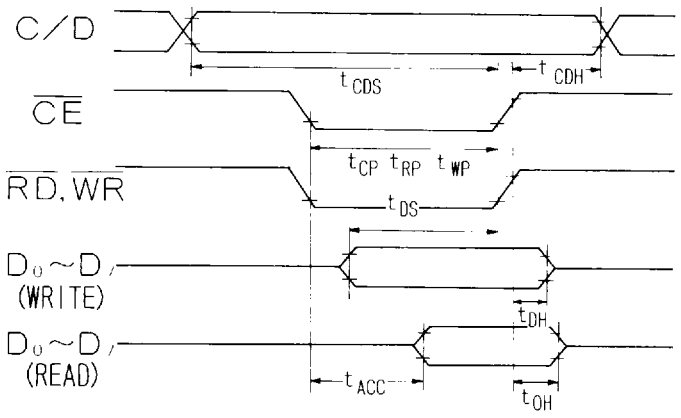
| No | Symbol | Functions | No | Symbol | Functions |
|---|---|---|---|---|---|
| 1 | FGND/ELGND | Frame Gnd/EL Gnd, pin | 11 | DB 0 | |
| 2 | $V_{SS}$ | Gnd pin, 0V | 12 | DB 1 | |
| 3 | $V_{DD}$ | Positive power pin, +5V | 13 | DB 2 | |
| 4 | $V_{EE}$ | Negative power pin, −15V max. | 14 | DB 3 | Data bus line |
| 5 | $\overline{WR}$ | Write input pin, L:data write | 15 | DB 4 | D 0 : LSB |
| 6 | $\overline{RD}$ | Read input pin, L:data read | 16 | DB 5 | D 7 : MSB |
| 7 | $\overline{CE}$ | Chip enadle input pin, L:enable | 17 | DB 6 | |
| 8 | C/D | Command/data select pin, H:command, L:data | 18 | DB 7 | |
| 9 | NC | | 19 | FS | Word area select pin, FS1=L(8×8) |
| 10 | $\overline{RESET}$ | Reset input pin, L:reset | 20 | NC | |

| | | |
|---|---|---|
| 21 | EL+ | (High voltage side, EL input pin) |
| 22 | EL(GND) | (Gnd side, EL input pin) |



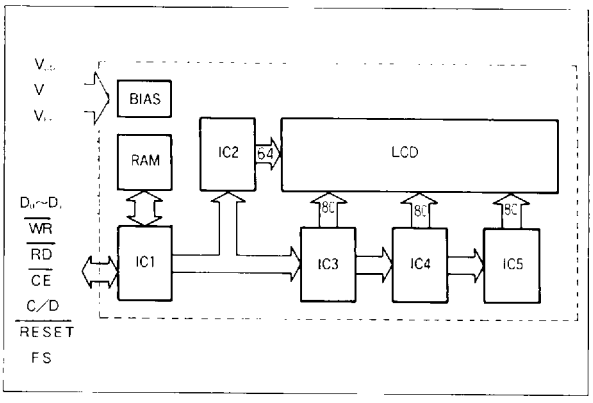
## Timing chart




$V_{DD}$=5V±10%、$V_{SS}$=0V、Ta=−10~+70℃

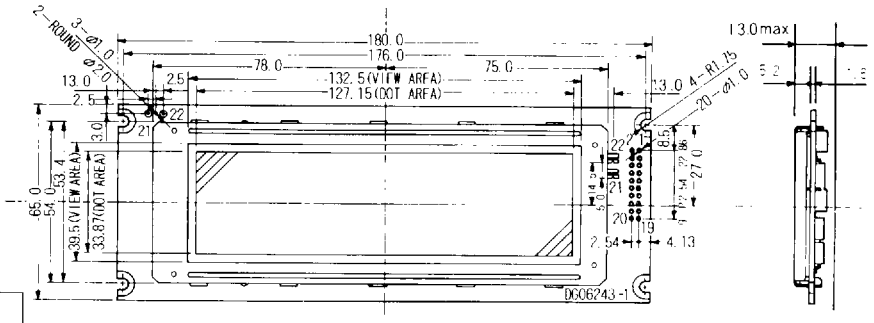
| Parameter | Symbol | min. | max. | unit |
|---|---|---|---|---|
| C/D setup time | tCDS | 100 | — | ns |
| C/D hold time | tCDH | 10 | — | ns |
| CE, RD, WR, pulse width | tCP<br>tRP<br>tWP | 80 | — | ns |
| Data setup time | tDS | 80 | — | ns |
| Data hold time | tDH | 40 | — | ns |
| Access time | tACC | — | 150 | ns |
| Output hold time | tOH | 10 | 50 | ns |

## Block diagram




## Module dimensions

(unit : mm)




### ■Pattern dimensions