

C²MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC40H074P/F

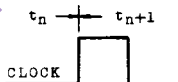
TC40H074 DUAL D-TYPE FLIP-FLOP WITH PRESET AND CLEAR

The TC40H074 is a D-type flip-flop containing two circuits which permits clear and preset operations.

*1 ... Set CLEAR and PRESET to "H" level.

D-MODE (*1)

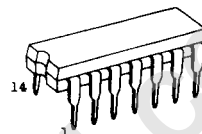
t_n	t_{n+1}	
D	Q	$\bar{Q}$
L	L	H
H	H	L



R-S MODE (*2)

INPUTS		OUTPUTS	
CLEAR	PRESENT	$\bar{Q}$	Q
H	L	L	H
L	H	H	L
L	L	H	H
H	H	D - MODE	

*2 ... Set D and CLOCK to "H" or "L" level.

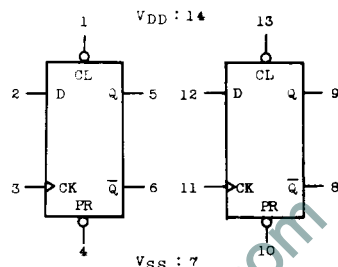


DIP14 (3D14A-P)



MFP14 (F14GB-P)

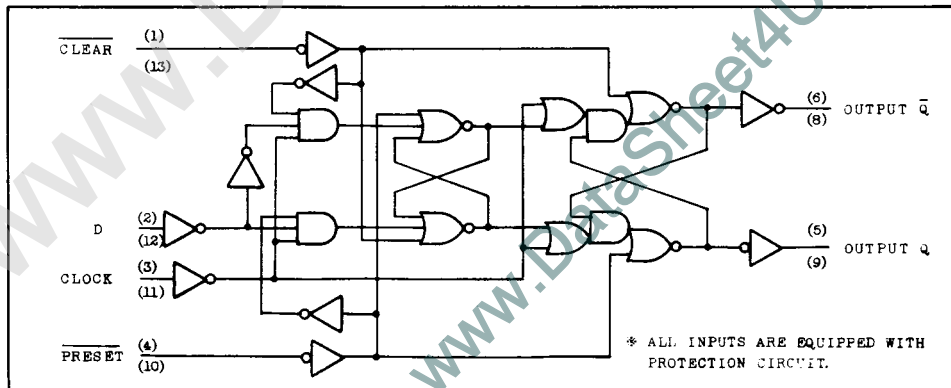
BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+10$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$
Lead Temp./Time	T_{sol}	$260^{\circ}\text{C} \cdot 10 \text{ sec}$	

LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	-	2.0	-	8.0	V
Input Voltage	V _{IN}	-	0.0	-	V _{DD}	V
Operating Temperature	T _{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} = V _{SS} , V _{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} = V _{SS} , V _{DD}	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current	I _{OH}	V _{OH} = 4.6V V _{IN} = V _{SS} , V _{DD}	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I _{OL}	V _{OL} = 0.4V V _{IN} = V _{SS} , V _{DD}	5	1.4	-	1.1	-	-	0.8	-	
Input Voltage	"H" Level V _{IH}	I _{OUT} < 1μA V _{OH} = 4.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level V _{IL}	V _{OL} = 0.5V	5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level I _{IH}	V _{IH} = 8.0V	8	-	0.3	-	10 ⁻⁵	0.3	-	1.0	μA
	"L" Level I _{IL}	V _{IL} = 0.0V	8	-	-0.3	-	-10 ⁻⁵	-0.3	-	-1.0	
Quiescent Supply Current	I _{DD}	*V _{IN} = V _{SS} , V _{DD}	5	-	5.0	-	10 ⁻²	5.0	-	25.0	μA

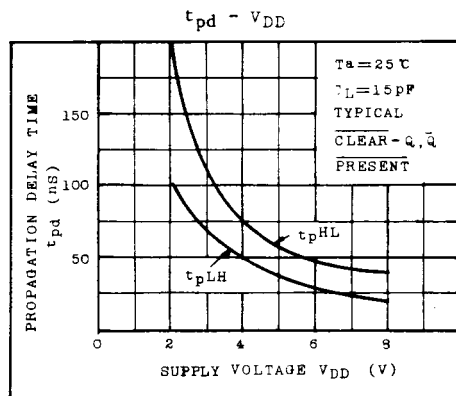
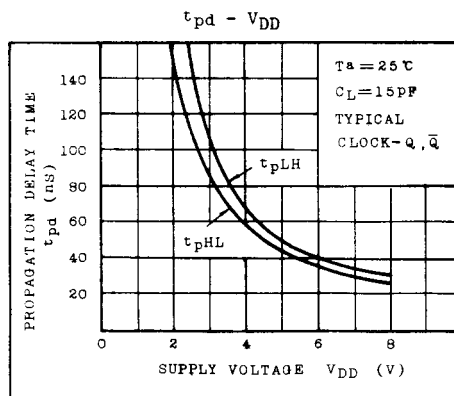
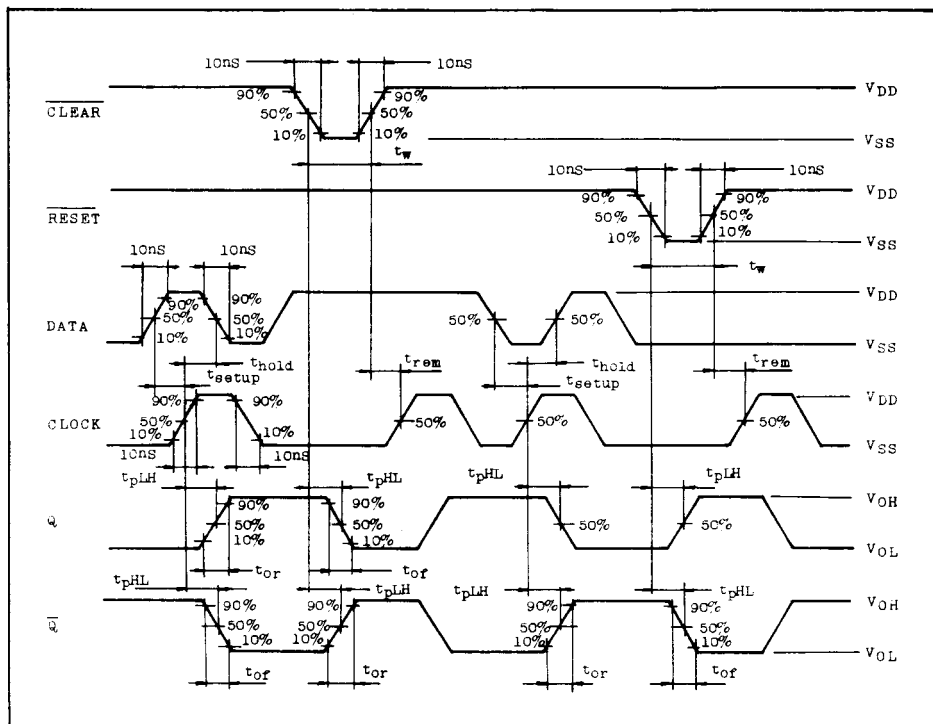
*All valid input combinations

SWITCHING CHARACTERISTICS (T_a = 25°C, V_{SS} = 0.0V, C_L = 15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t _{or}		5	-	27	40	ns
Output Fall Time		t _{of}		5	-	27	40	
Propagation Delay Time	(Low-High)	t _{pLH}	CLOCK-Q, $\bar{Q}$	5	-	49	72	ns
	(High-Low)	t _{pHL}		5	-	43	65	
	(Low-High)	t _{pLH}	CLEAR PRESET -Q, $\bar{Q}$	5	-	33	50	
	(High-Low)	t _{pHL}		5	-	59	88	
Min. Pulse Width		t _W	CLEAR, PRESET	5	-	20	32	ns
Max. Clock Rise Time		t _{rφ}	CLOCK	5	1.0	-	-	μs
Max. Clock Fall Time		t _{fφ}						
Min. Data Setup Time		t _{set-up}	D-CLOCK	5	-	16	25	ns
Min. Data Hold Time		t _{hold}	CLOCK-D	5	-	-	0	ns
Max. Clock Frequency		f _{MAXφ}		5	10	20	-	MHz
Input Capacitance		C _{IN}			-	5		pF
Clear and Preset Removal Time		t _{rem}		5	-	19	35	ns

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SWITCHING TIME TEST WAVEFORM



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