# LH5021B/LH5022 LCD Dot Matrix Driver LSI

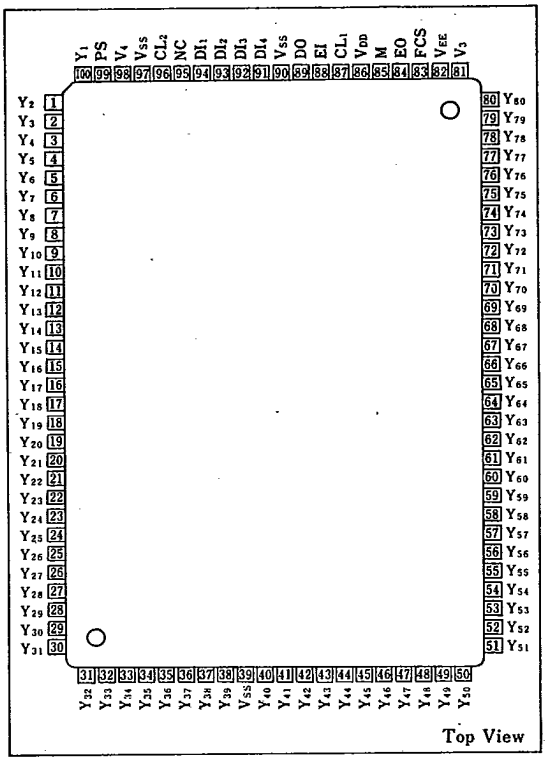
## Description

LH5021B/LH5022 is an LCD driver LSI which can receive either serial input data or parallel input data. In case of the serial input mode, it can be connected in series. It converts character pattern data input to parallel data output with 80-bit latch circuit and provides character pattern waveforms output in accordance with mode select signal.

## Features

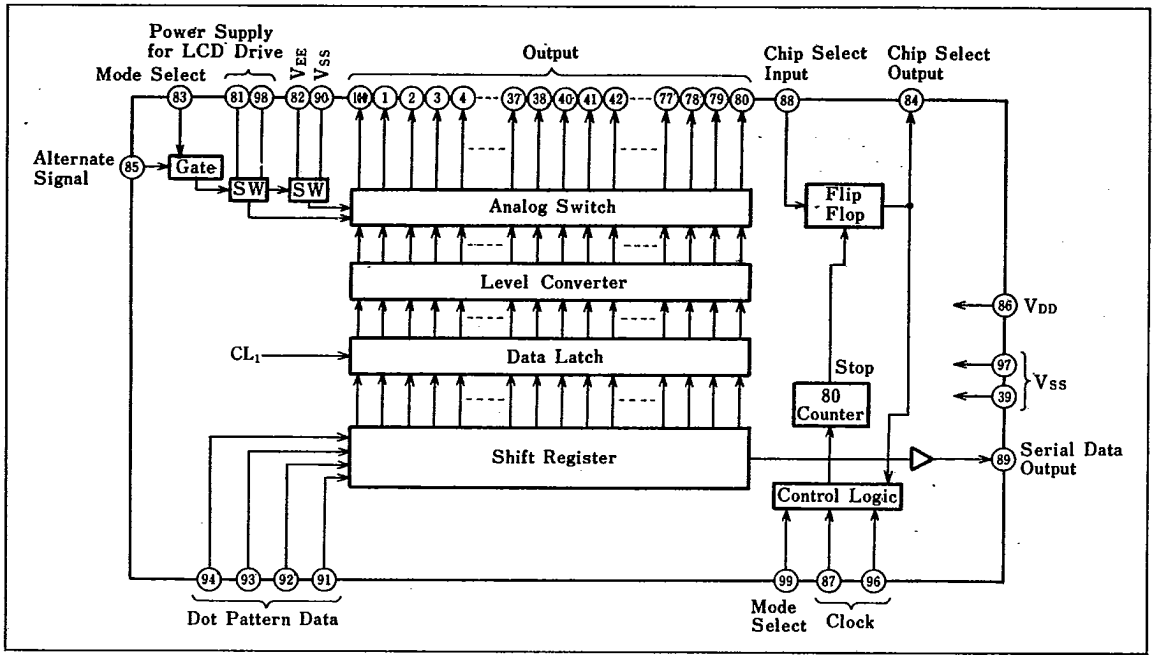
1. CMOS process
2. 80-LCD driver circuit
3. 4 functions selectable as follows
   (a) Segment signal drivers on the serial input mode
   (b) Segment signal drivers with the chip-selectable function on the serial input mode
   (c) Segment signal drivers with the chip-selectable function on the parallel input mode
   (d) Common signal drives on the serial input mode
4. Auto count function ; in a chip selected state, counts 80 input data automatically and stops the internal clock $CL_2$
5. Power supply voltage : −5V (TYP.)
6. Display voltage
   LH5021B : −17V (TYP.),
   LH5022 : −24V (TYP.)
7. 100-pin quad-flat package

## Pin Connections



Top View

## Block Diagram



## ■ Pin Description

| Pin name | Name | I/O | Functions |
|---|---|---|---|
| $V_{DD}$ | Power supply | I | For logic circuit (−5V) |
| $V_{EE}$ | | | For liquid crystal drive circuit (LH5021A: −17V, LH5022: −24V) |
| $V_{SS}$ | | | GND |
| $V_3$, $V_4$ | Segment output voltage supply | I | Durling non-select, however $V_{SS}>V_3>V_4>V_{EE}$ |
| $Y_1$-$Y_{80}$ | Segment output | O | |
| $CL_1$ | Clock | I | For data latch *It must be applied when 4 times the shift clock |
| $CL_2$ | | | For data shift |
| FCS, PS | Mode select | I | See table below |
| M | Liquid crystal drive waveform AC conversion signal input | I | See table below |
| $DI_1$-$DI_4$ | Display data input | I | When used with a common driver and in the serial input mode, supply the data to the $DI_1$ pin. In this case, it is necessary to fix $DI_2$−$DI_4$ to the $V_{SS}$ level or the $V_{DD}$ level. |
| DO | Serial data output | O | When used in the chip select mode, it becomes high level. |
| EI | For chip select | I | Used only in the chip select mode. |
| EO | | O | (1) The ($CL_1$ · $CL_2$) timing causes EO to become low level.<br>(2) After (1), the device is set to the select mode by inputting a high signal to EI, and the input data is read in according to the timing of the fall of $CL_2$.<br>(3) When 80 items of input data (equivalent to 80 $CL_2$ clock cycles in the serial mode or 20 $CL_2$ clock cycles in the 4-bit parallel mode) have been read in, EO automatically becomes high level and data read in is terminated. EO is reset 1.5 cycles later. |

| FCS | PS | Mode | Chip select | DO out. |
|---|---|---|---|---|
| Low | Low | 1-bit serial input segment driver | No | Yes |
| Low | High | 4-bit parallel input segment driver | Yes | High |
| High | Low | 1-bit serial input segment driver | Yes | High |
| High | High | Commnn driver (serial input) | No | Yes |

Note 1: In the serial input mode, data is supplied from the $DI_1$ pin.

Note 2: The relationship between data input during 4-bit parallel input and the Y output is as follows.

- $DI_1$ : $Y_1$, $Y_5$, $Y_9$, ··· $Y_{73}$, $Y_{77}$
- $DI_2$ : $Y_2$, $Y_6$, $Y_{10}$, ··· $Y_{74}$, $Y_{78}$
- $DI_3$ : $Y_3$, $Y_7$, $Y_{11}$, ··· $Y_{75}$, $Y_{79}$
- $DI_4$ : $Y_4$, $Y_8$, $Y_{12}$, ··· $Y_{76}$, $Y_{80}$

Note 3: When used as a comon driver, the clock used for transfer is input to the $CL_2$ pin. $CL_1$ is internally fixed.

Note 4: To minimize current consumption, it is necessary to fix unused input pins to the same level as the $V_{SS}$ pin or the $V_{DD}$ pin.

Common signal drive mode

| Latch data | M | Y out. |
|---|---|---|
| Low (non-display) | Low | $V_3$ |
| | High | $V_4$ |
| High (display) | Low | GND |
| | High | $V_{EE}$ |

Segment signal drive mode

| Latch data | M | Y out. |
|---|---|---|
| Low (non-display) | Low | $V_3$ |
| | High | $V_4$ |
| High (display) | Low | $V_{EE}$ |
| | High | GND |

| Pin name | Name | I/O | Functions |
|---|---|---|---|
| | | | (4) When two or more devices are used in the chip select mode, EO of the first stage and EI of the second stage are connected and used.<br>1. EO of all devices connected is reset by (1) and goes to the non-select condition and waits for EI input.<br>2. When a high signal is applied to EI of the initial device in the cascade connection, this device performs the operations in (2) and (3).<br>3. Connecting EO of the initial devices to EI of the next devices causes the devices perform the operations in (2) and (3) after the initial device. This operation is repeated in the same manner for all subsequent devices.<br>In the non-select condition, the shift clock $CL_2$ stops internally, so power consumption becomes extremely small. |

## ■ Absolute Maximum Ratings

| Parameter | Symbol | LH5021B Ratings | LH5022 Ratings | Unit | Note |
|---|---|---|---|---|---|
| Applied voltage (logic) | $V_{DD}$ | −7 to +0.3 | −7 to +0.3 | V | 1 |
| Applied voltage (Liquid crystal drive circuit) | $V_{EE}$ | −20 to +0.3 | −30 to +0.3 | V | 1 |
| Input voltage (logic) | $V_{IN}$ | $V_{DD}$−0.3 to +0.3 | $V_{DD}$−0.3 to +0.3 | V | 1 |
| Operating temperature | $T_{opr}$ | −20 to +70 | −20 to +70 | ℃ | |
| Storage temperature | $T_{stg}$ | −55 to +150 | −55 to +150 | ℃ | |

Note 1: The maximum applicable voltage on any pin with respect to $V_{SS}$.

## ■ DC characteristics

**LH5021B** ($V_{SS}$=0V, $V_{DD}$=−5V±10%, $V_{EE}$=−17±1V, Ta=−20 to +70℃)

| Paramenter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL}$ | | | | $0.8V_{DD}$ | V |
| Input "High" voltage | $V_{IH}$ | | $0.2V_{DD}$ | | | V |
| Output "Low" voltage | $V_{OL}$ | $I_{OL}$=0.4mA | | | V+0.4 | V |
| Output "High" voltage | $V_{OH}$ | $I_{OH}$=0.4mA | −0.4 | | | V |
| Voltage drop between Vi-Yi | $V_{D1}$ | Apply 0.2mA to one of $Y_1$-$Y_{80}$ | | | 1.1 | V |
| Voltage drop between Vi-Yi | $V_{D2}$ | Apply 0.2mA to each of $Y_1$-$Y_{80}$ | | | 1.5 | V |
| Input leakage current | $\lvert I_{LI} \rvert$ | | | | 1.0 | μA |
| Output leakage current | $\lvert I_{LO} \rvert$ | | | | 10.0 | μA |
| Current consumption for logic unit | $I_{LOG}$ | Logic clock : 3.3 MHz | | 2.2 | 6.0 | mA |

**LH5022** ($V_{SS}$=0V, $V_{DD}$=−4.5 to −5.5V, $V_{EE}$=−21 to −27V, $V_3$=−2.5 to −5.5V, $V_4$=−16.5 to −23.5V, Ta=−20 to +70°C)

| Paramenter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL}$ | | | | $0.8V_{DD}$ | V |
| Input "High" voltage | $V_{IH}$ | | $0.2V_{DD}$ | | | V |
| Output "Low" voltage | $V_{OL}$ | $I_{OL}$=0.4mA | | | $V_{DD}$+0.4 | V |
| Output "High" voltage | $V_{OH}$ | $I_{OH}$=0.4mA | −0.4 | | | V |
| Voltage drop between $V_1$-$Y_1$ | $V_{D1}$ | Apply 0.5mA to one of $Y_1$-$Y_{80}$<br>$V_3$=2/12$V_{EE}$, $V_4$=10/12$V_{EE}$ | | | 1.0 | V |
| Voltage drop between $V_1$-$Y_1$ | $V_{D2}$ | Apply 0.08mA to each of $Y_1$-$Y_{80}$<br>$V_3$=2/12$V_{EE}$, $V_4$=10/12$V_{EE}$ | | | 1.5 | V |
| Input leakage current | $\lvert I_{LI} \rvert$ | | | | 1.0 | μA |
| Output leakage current | $\lvert I_{LO} \rvert$ | | | | 10.0 | μA |
| Current consumption for logic unit | $I_{LOG}$ | Logic clock : 3.3 MHz<br>1-bit serial transfer : 3.3MHz | | | 5.0 | mA |
| | | 4-bit parallel transfer : 2.0MHz | | | 10.0 | mA |

**LH5022** ($V_{SS}$=0V, $V_{DD}$=−4.5 to −5.5V, $V_{EE}$=−15 to −24V, $V_3$=−5 to +1.5V, $V_4$=−11.5 to −21V, Ta=−20 to +70°C)

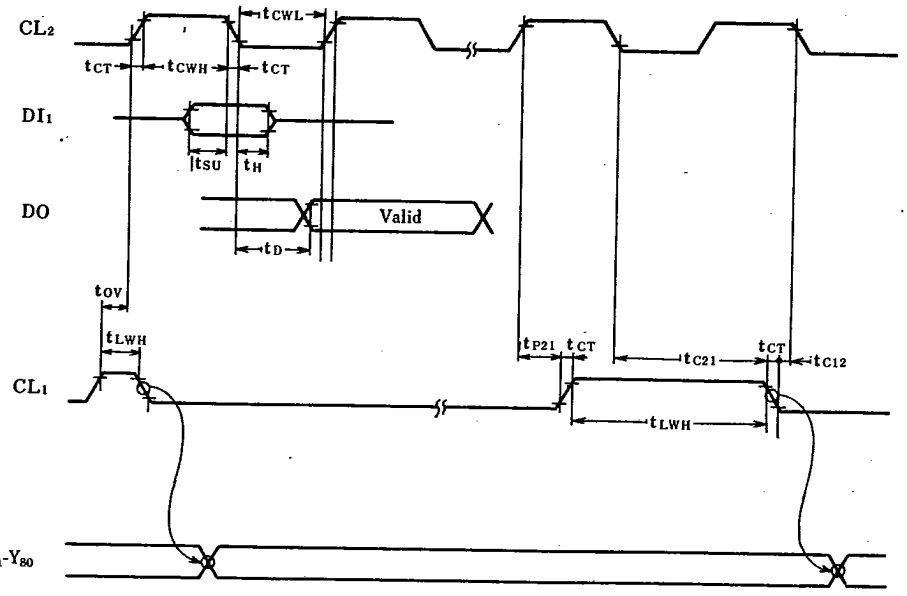
| Paramenter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL}$ | | | | $0.8V_{DD}$ | V |
| Input "High" voltage | $V_{IH}$ | | $0.2V_{DD}$ | | | V |
| Output "Low" voltage | $V_{OL}$ | $I_{OL}$=0.4mA | | | $V_{DD}$+0.4 | V |
| Output "High" voltage | $V_{OH}$ | $I_{OH}$=0.4mA | −0.4 | | | V |
| Voltage drop between $V_1$-$Y_1$ | $V_{D1}$ | Apply 0.35mA to one of $Y_1$-$Y_{80}$<br>$V_3$=2/12$V_{EE}$, $V_4$=10/12$V_{EE}$ | | | 1.0 | V |
| Voltage drop between $V_1$-$Y_1$ | $V_{D2}$ | Apply 0.06mA to each of $Y_1$-$Y_{80}$<br>$V_3$=2/12$V_{EE}$, $V_4$=10/12$V_{EE}$ | | | 1.5 | V |
| Input leakage current | $\lvert I_{LI} \rvert$ | | | | 1.0 | μA |
| Output leakage current | $\lvert I_{LO} \rvert$ | | | | 10.0 | μA |
| Current consumption for logic unit | $I_{LOG}$ | Logic clock : 3.3 MHz<br>1-bit serial transfer : 3.3MHz | | | 5.0 | mA |
| | | 4-bit parallel transfer : 2.0MHz | | | 10.0 | mA |

## ■ AC Characteristics

### (1) 1-bit Serial Input Segment Driver (PS=FCS="Low") ($V_{DD}$=−5V±10%, $V_{SS}$=0V, Ta=−20 to +70℃)

| Parameter | Symbol | Conditions *1 | MIN. | MAX. | Unit | Applicable pins |
|---|---|---|---|---|---|---|
| Clook frequency | $t_C$ | | 300 | | ns | $CL_2$ |
| Clock "High" width | $t_{CWH}$ | | 130 | | ns | $CL_2$ |
| Clock "Low" width | $t_{CWL}$ | | 130 | | ns | $CL_1$, $CL_2$ |
| Data setup time | $t_{SU}$ | | 70 | | ns | $DI_1$ |
| Data hold time | $t_H$ | | 50 | | ns | $DI_1$ |
| Output delay | $t_D$ | $C_L$=15pF | | 230 | ns | DO |
| Latch clock "High" width | $t_{LWH}$ | | 130 | *3 | ns | $CL_1$ |
| Clock margin time (from $CL_1$ ↓ to $CL_2$ ↓) | $t_{C12}$ | | 20 | | ns | $CL_1$, $CL_2$ |
| Clock margin time *2 (from $CL_2$ ↓ to $CL_1$ ↓) | $t_{C21}$ | | 200 | | ns | $CL_1$, $CL_2$ |
| Clock margin time (from $CL_2$ ↑ to $CL_1$ ↑) | $t_{P21}$ | | 20 | | ns | $CL_1$, $CL_2$ |
| Clock ↑, ↓ time | $t_{CT}$ | | | 50 | ns | $CL_1$, $CL_2$ |
| Overlap time of $CL_2$ "Low" and $CL_1$ "High" | $t_{OV}$ | | 130 | | ns | $CL_1$, $CL_2$ |

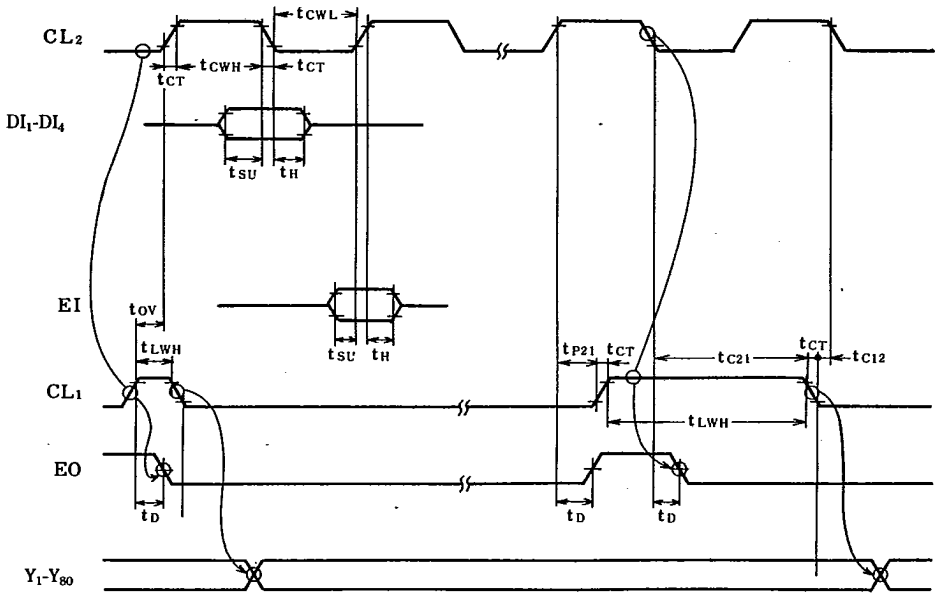
Test conditions
Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.2V_{DD}$, $0.8V_{DD}$
*1 LH5021B : $V_{EE}$=−17V±1V, LH5022 : $V_{EE}$=−24V±3V
*2 Internal shift register valid time
*3 $1.5t_C-t_{C12}-t_{P21}-3t_{CT}$



(2) **4-bit Input Segment Driver** (PS="High", FCS="Low") ($V_{DD}$=−5V±10%, $V_{SS}$=0V, Ta=−20 to +70℃)

| Parameter | Symbol | Conditions*1 | MIN. | MAX. | Unit | Applicable pins |
|---|---|---|---|---|---|---|
| Clock frequency | $t_C$ | | 500 | | ns | $CL_2$ |
| Clock "High" width | $t_{CWH}$ | | 230 | | ns | $CL_2$ |
| Clock "Low" width | $t_{CWL}$ | | 230 | | ns | $CL_1$, $CL_2$ |
| Data setup time | $t_{SU}$ | | 70 | | ns | $DI_1$, $DI_2$, $DI_3$, $DI_4$, EI |
| Data hold time | $t_H$ | | 50 | | ns | $DI_1$, $DI_2$, $DI_3$, $DI_4$, EI |
| Output delay | $t_D$ | $C_L$=15pF | | 230 | ns | EO |
| Latch clock "High" width | $t_{LWH}$ | | 130 | *3 | ns | $CL_1$ |
| Clock margin time (from $CL_1$ ↓ to $CL_2$ ↓) | $t_{C12}$ | | 20 | | ns | $CL_1$, $CL_2$ |
| Clock margin time *2 (from $CL_2$ ↓ to $CL_1$ ↓) | $t_{C21}$ | | 200 | | ns | $CL_1$, $CL_2$ |
| Clock margin time (from $CL_2$ ↑ to $CL_1$ ↑) | $t_{P21}$ | | 20 | | ns | $CL_1$, $CL_2$ |
| Clock ↑, ↓ time | $t_{CT}$ | | | 50 | ns | $CL_1$, $CL_2$ |
| Overlap time of $CL_2$ "Low" and $CL_1$ "High" | $t_{OV}$ | | 130 | | ns | $CL_1$, $CL_2$ |

Test conditions
Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.2V_{DD}$, $0.8V_{DD}$
*1 LH5021B : $V_{EE}$=−17V±1V, LH5022 : $V_{EE}$=−24V±3V
*2 Internal shift register valid time
*3 $1.5t_C-t_{C12}-t_{P21}-3t_{CT}$

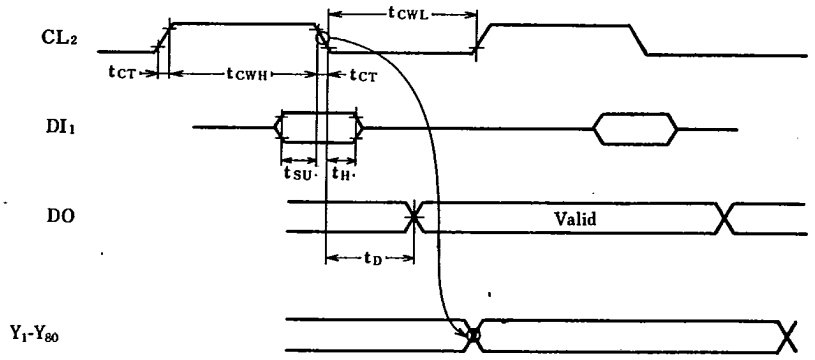


### (3) Common Driver (PS="Low", FCS="High")

($V_{DD}$=−5V±10%, $V_{SS}$=0V, Ta=−20 to +70℃)

| Parameter | Symbol | Conditions*1 | MIN. | MAX. | Unit | Applicable pins |
|---|---|---|---|---|---|---|
| Clock frequency | $t_C$ | | 1000 | | ns | $CL_2$ |
| Clock "High" width | $t_{CWH}$ | | 130 | | ns | $CL_2$ |
| Clock "Low" width | $t_{CWL}$ | | 830 | | ns | $CL_2$ |
| Data setup time | $t_{SU}$ | | 70 | | ns | $DI_1$ |
| Data hold time | $t_H$ | | 50 | | ns | $DI_1$ |
| Output delay | $t_D$ | $C_L$=15pF | | 500 | ns | DO |
| Clock ↑, ↓ time | $t_{CT}$ | | | 50 | ns | $CL_2$ |

Test conditions
Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.8V_{DD}$, $0.2V_{DD}$
*1 LH5021B : $V_{EE}$=−17V±1V, LH5022 : $V_{EE}$=−24V±3V

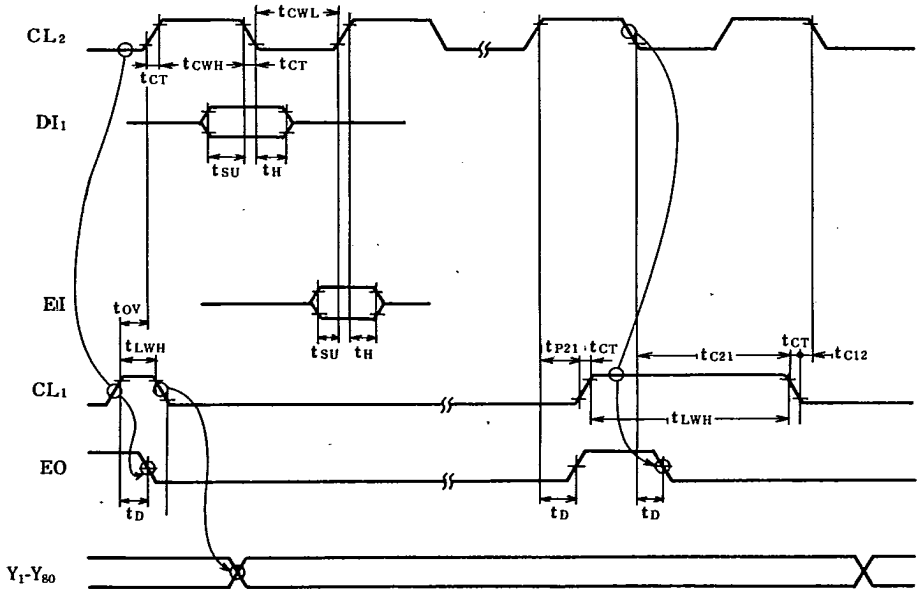


### (4) 1-bit Serial Input Segment Driver (PS="Low", FCS="High")

($V_{DD}$=−5V±10%, $V_{SS}$=0V, Ta=−20 to +70℃)

| Parameter | Symbol | Conditions *1 | MIN. | MAX. | Unit | Applicable pins |
|---|---|---|---|---|---|---|
| Clock frequency | $t_C$ | | 380 | | ns | $CL_2$ |
| Clock "High" width | $t_{CWH}$ | | 170 | | ns | $CL_2$ |
| Clock "Low" width | $t_{CWL}$ | | 170 | | ns | $CL_1$, $CL_2$ |
| Data setup time | $t_{SU}$ | | 70 | | ns | $DI_1$, EI |
| Data hold time | $t_H$ | | 50 | | ns | $DI_1$, EI |
| Output delay | $t_D$ | $C_L$=15pF | | 230 | ns | EO |
| Latch clock "High" width | $t_{LWH}$ | LH5021B | 140 | *3 | ns | $CL_1$ |
| | | LH5022 | 130 | | | |
| Clock margin time (from $CL_1$↓ to $CL_2$↓) | $t_{C12}$ | | 20 | | ns | $CL_1$, $CL_2$ |
| Clock margin time *2 (from $CL_2$↓ to $CL_1$↓) | $t_{C21}$ | | 200 | | ns | $CL_1$, $CL_2$ |
| Clock margin time (from $CL_2$↑ to $CL_1$↑) | $t_{P21}$ | | 20 | | ns | $CL_1$, $CL_2$ |
| Clock ↑, ↓ time | $t_{CT}$ | | | 50 | ns | $CL_1$, $CL_2$ |
| Overlap time of $CL_2$ "Low" and $CL_1$ "High" | $t_{OV}$ | | 130 | | ns | $CL_1$, $CL_2$ |

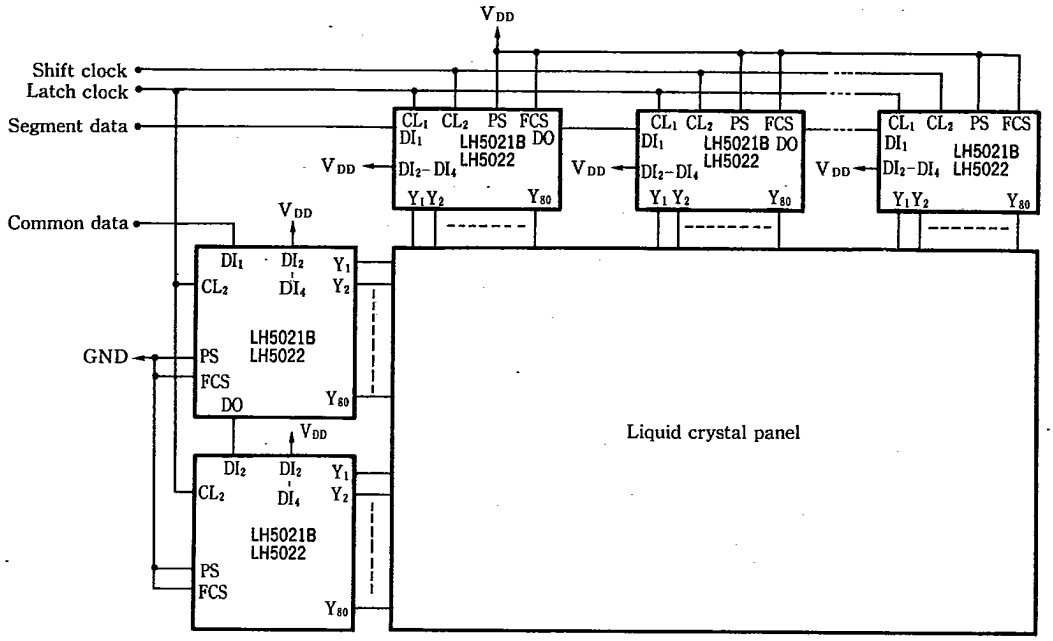
Test conditions
Input frequency : $0.8V_{DD}$, $0.2V_{DD}$; Input reference level : $0.8V_{DD}$, $0.2V_{DD}$; Output reference level : $0.2V_{DD}$, $0.8V_{DD}$
*1 LH5021B : $V_{EE}$=−17V±1V, LH5022 : $V_{EE}$=−24V
*2 Internal shift register valid time
*3 $1.5t_C-t_{C12}-t_{P21}-3t_{CT}$



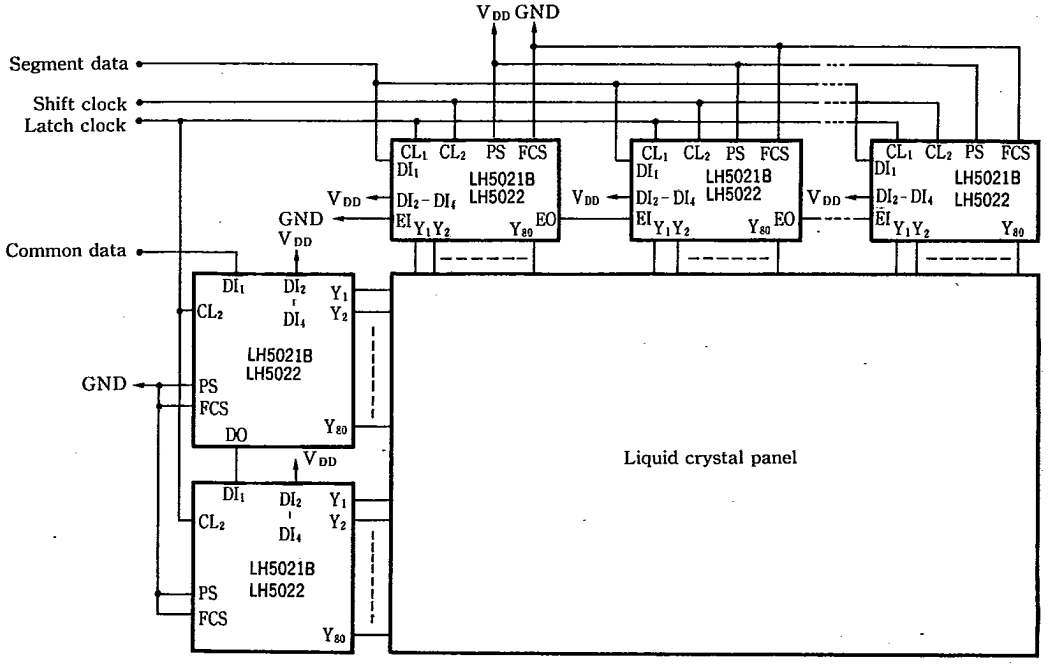
## ■ System Configuration Example

T-51-17

### (1) 1-bit serial input segument driver and common driver




### (2) 1-bit chip select segument driver and common driver



### (3) 4-bit parallel input segument driver and common driver