# LH1692

## 300-output TFT-LCD Gate Driver IC

## DESCRIPTION

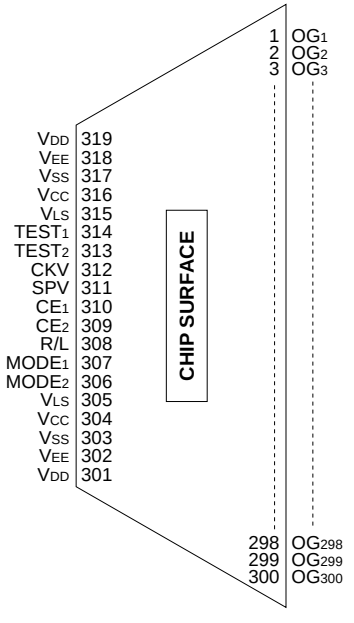
The LH1692 is a 300-output TFT-LCD gate driver IC.

## FEATURES

- Number of LCD drive outputs : 300
- LCD drive output sequence :
  Output shift direction can be selected
  $OG_1 \rightarrow OG_{300}$ or $OG_{300} \rightarrow OG_1$
- Cascade connection :
  Max. 4 cascades (internal counting system)
- Usable with both positive/negative power supplies
- Output mode selection
  – Normal mode (1-pulse scanning)
  – Continuous 2-pulse mode (2-pulse scanning)
  – Jumping 2-pulse mode (2-pulse scanning)
- LCD drive voltage : +16.0 to +42.0 V
- Operating temperature : –30 to + 85 ˚C
- Package : 319-pin TCP (Tape Carrier Package)

## PIN CONNECTIONS

**319-PIN TCP** TOP VIEW

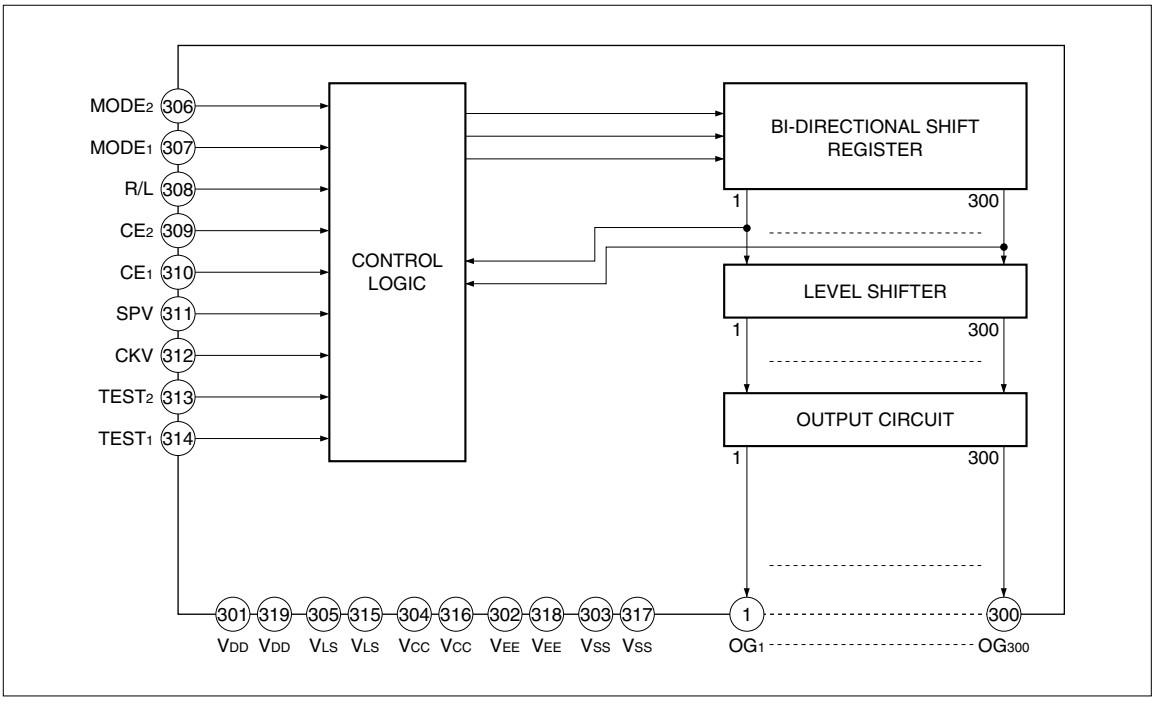



**NOTE :**
Doesn't prescribe TCP outline.

## PIN DESCRIPTION

| PIN NO. | SYMBOL | I/O | DESCRIPTION |
|---|---|---|---|
| 1 to 300 | $OG_1$-$OG_{300}$ | O | LCD drive output pins |
| 301, 309 | $V_{DD}$ | – | Power supply pins for LCD drive |
| 302, 318 | $V_{EE}$ | – | Power supply pins for LCD drive |
| 303, 317 | $V_{SS}$ | – | Power supply pins for logic system |
| 304, 316 | $V_{CC}$ | – | Power supply pins for logic system |
| 305, 315 | $V_{LS}$ | – | Power supply pins for input level shifter |
| 306, 307 | $MODE_2$, $MODE_1$ | I | Output mode selection pins |
| 308 | R/L | I | Pin for selecting bi-directional shift register and setting cascade sequence |
| 309, 310 | $CE_2$, $CE_1$ | I | Cascade sequence setting pins |
| 311 | SPV | I | Vertical scanning start pulse input pin |
| 312 | CKV | I | Vertical shift clock input pin |
| 313, 314 | $TEST_2$, $TEST_1$ | I | IC test pins |

## BLOCK DIAGRAM



## FUNCTIONAL OPERATIONS OF EACH BLOCK

| BLOCK | FUNCTION |
|---|---|
| Control Logic | Used to create signals necessary for mode selecting signal, cascade sequence setting signal and for operation of bi-directional shift register. |
| Bi-directional Shift Register | Used as transfer circuit of LCD drive output start signal. It is possible to set LCD drive output sequence of $OG_1 \rightarrow OG_{300}$ direction or $OG_{300} \rightarrow OG_1$ direction. |
| Level Shifter | Used as circuit which shifts LCD drive output signals transferred by bi-directional shift register to $V_{DD}$-$V_{EE}$ level. |
| Output Circuit | Configured with output buffers to output $V_{DD}$-$V_{EE}$ level. |

## INPUT/OUTPUT CIRCUITS

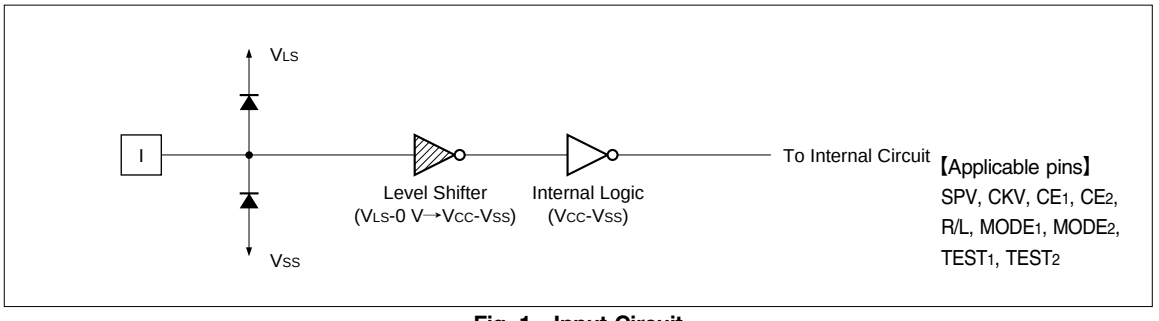



**Fig. 1 Input Circuit**

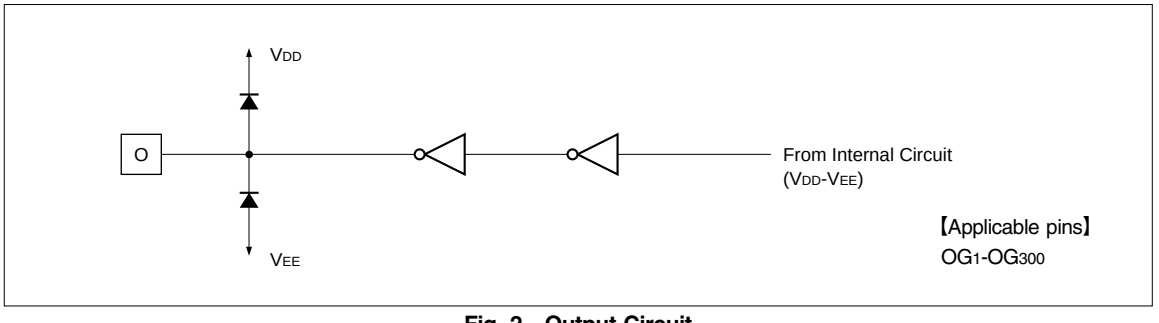



**Fig. 2 Output Circuit**

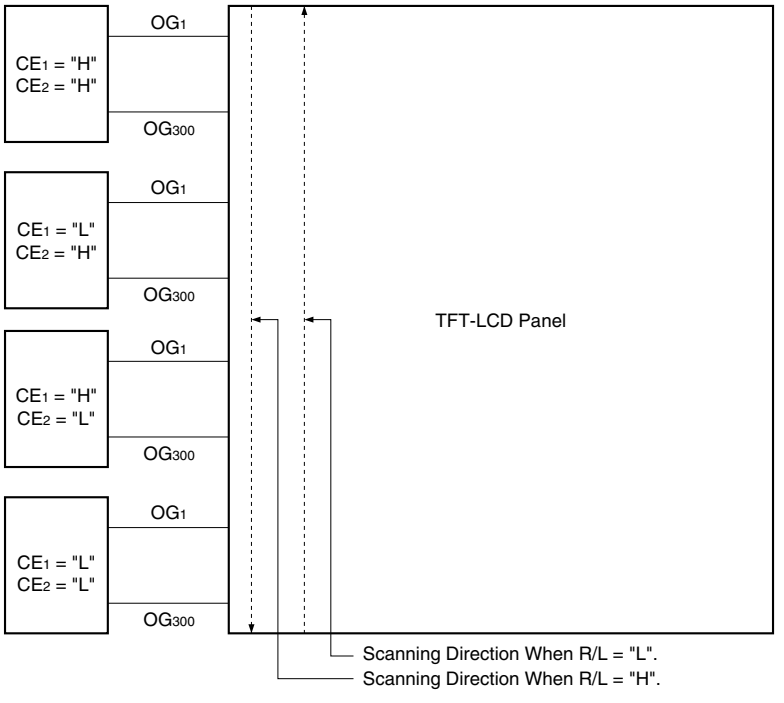
# FUNCTIONAL DESCRIPTION

## Pin Functions

<table>
<tr><th>SYMBOL</th><th>FUNCTION</th></tr>
<tr><td>$V_{DD}$</td><td>Used as power supply pin for high level LCD drive.</td></tr>
<tr><td>$V_{LS}$</td><td>Used as power supply pin for input level shifters.</td></tr>
<tr><td>$V_{CC}$</td><td>Used as power supply pin for logic system, normally connected to $V_{SS}$ + 5.0 V.</td></tr>
<tr><td>$V_{EE}$</td><td>Used as power supply pin for low level LCD drive.</td></tr>
<tr><td>$V_{SS}$</td><td>Used as logic system power supply pin.</td></tr>
<tr><td>CKV</td><td>Used as vertical shift clock pulse input pin.</td></tr>
<tr><td>SPV</td><td>Used as vertical scanning start pulse input pin. (At least, input one cycle of CKV during "L" period of SPV.)</td></tr>
<tr><td>$MODE_1$<br>$MODE_2$</td><td>Used as input pins for selecting output mode.<br>Output mode is set as shown in the table below by setting $MODE_1$ pin and $MODE_2$ pin.
<table>
<tr><th>$MODE_1$</th><th>$MODE_2$</th><th>Output mode</th></tr>
<tr><td>H</td><td>H</td><td>Normal mode (1-pulse scanning)</td></tr>
<tr><td>L</td><td>H</td><td>Continuous 2-pulse mode</td></tr>
<tr><td>H</td><td>L</td><td>Jumping 2-pulse mode</td></tr>
<tr><td>L</td><td>L</td><td>Set all outputs to $V_{EE}$ level.</td></tr>
</table></td></tr>
<tr><td>R/L</td><td>Used as input pin for selecting the shift direction of bi-directional shift register and for setting the sequence of cascade connection.<br>LCD drive outputs shift from $OG_1$ to $OG_{300}$ when set to "H". LCD drive outputs shift from $OG_{300}$ to $OG_1$ when set to "L". At the same time, cascade sequence is set as shown in the table below.</td></tr>
<tr><td>$CE_1$<br>$CE_2$</td><td>Used as input pins for setting of chip cascade sequence. (Max. 4 cascades)
<table>
<tr><th rowspan="2">$CE_1$</th><th rowspan="2">$CE_2$</th><th colspan="2">Cascade sequence</th></tr>
<tr><th>R/L = "H"</th><th>R/L = "L"</th></tr>
<tr><td>H</td><td>H</td><td>1st</td><td>4th</td></tr>
<tr><td>L</td><td>H</td><td>2nd</td><td>3rd</td></tr>
<tr><td>H</td><td>L</td><td>3rd</td><td>2nd</td></tr>
<tr><td>L</td><td>L</td><td>4th</td><td>1st</td></tr>
</table>With above setting, sets the cascade sequence signal inside the IC.</td></tr>
<tr><td>$TEST_1$<br>$TEST_2$</td><td>Used as input pins for IC testing.<br>Must be set to "H".</td></tr>
<tr><td>$OG_1$-$OG_{300}$</td><td>Used as output pins for LCD drive output, and which output data at 2 levels.<br>• Selecting data is output at $V_{DD}$ level .<br>• Non-selecting data is output at $V_{EE}$ level .</td></tr>
</table>

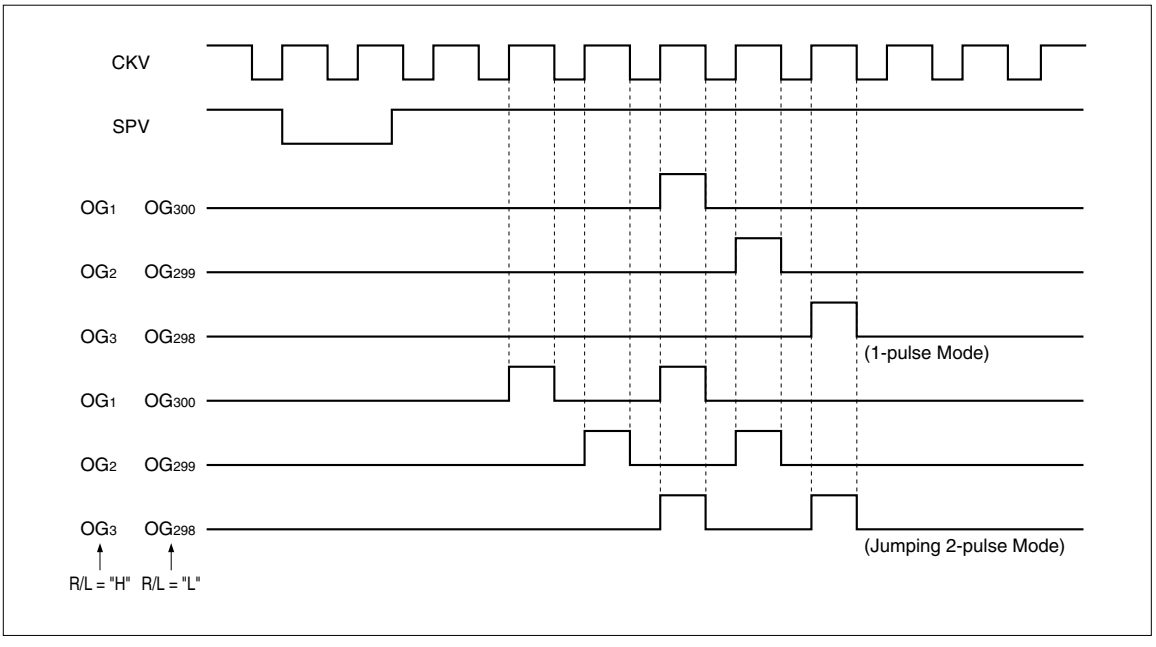
## Functional Operations

(1) Example of Cascade Sequence (One Side Assembled)

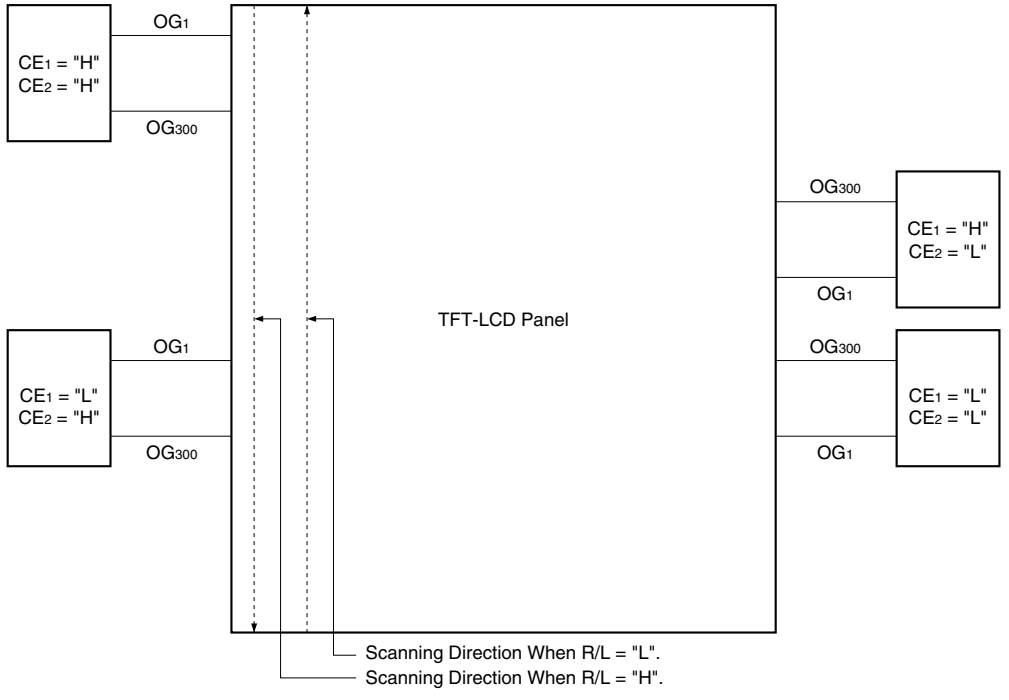



* At this time, normal mode (scanning with 1 pulse) is set when $MODE_1$ = "H" and $MODE_2$ = "H", jumping 2-pulse mode (scanning with 2 pulses) is set when $MODE_1$ = "H" and $MODE_2$ = "L", continuous 2-pulse mode (scanning with 2 pulses) is set when $MODE_1$ = "L" and $MODE_2$ = "H", and output $V_{EE}$ level is set when $MODE_1$ = "L" and $MODE_2$ = "L".

(2) Example of Input/Output Timing (For 1st Cascade Sequence)

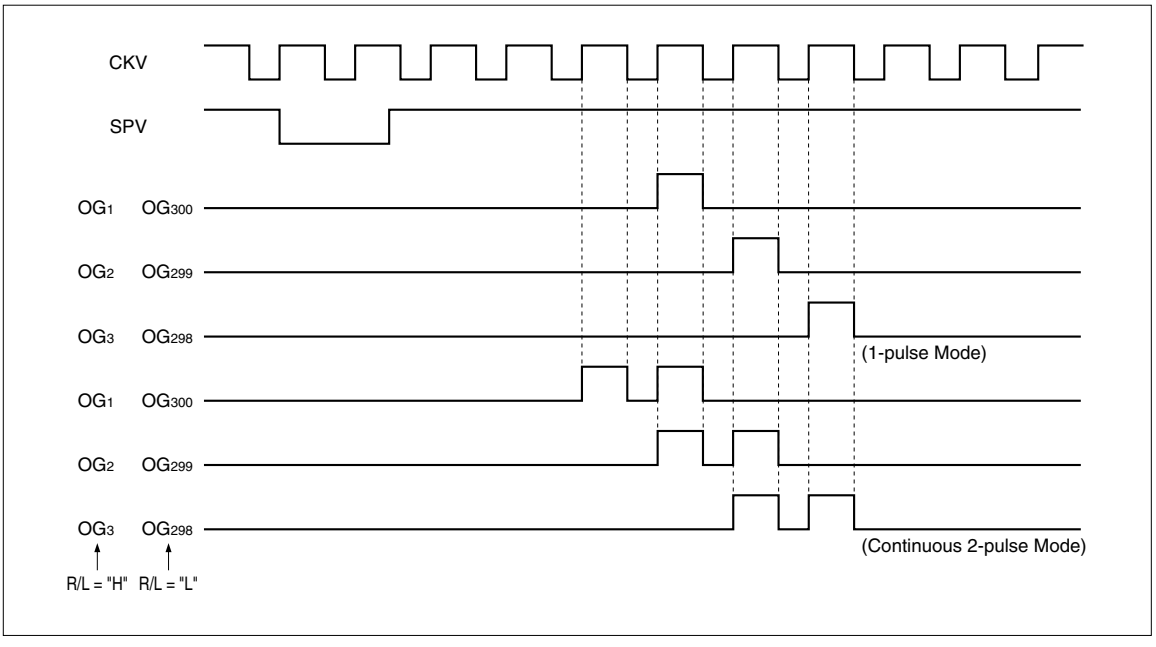


(3) Example of Cascade Sequence (Both Side Assembled)




∗ At this time, normal mode (scanning with 1 pulse) is set when $MODE_1$ = "H" and $MODE_2$ = "H", jumping 2-pulse mode (scanning with 2 pulses) is set when $MODE_1$ = "H" and $MODE_2$ = "L", continuous 2-pulse mode (scanning with 2 pulses) is set when $MODE_1$ = "L" and $MODE_2$ = "H", and output $V_{EE}$ level is set when $MODE_1$ = "L" and $MODE_2$ = "L".

(4) Example of Input/Output Timing (For 1st Cascade Sequence)



## PRECAUTIONS

**Precautions when connecting or disconnecting the power supply**

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. Therefore, when connecting the power supply, observe the following sequence.

Logic system power supply ($V_{LS}$) or internal logic system power supply ($V_{SS}$, $V_{CC}$; $V_{CC} > V_{SS}$) → logic input → LCD drive power supply ($V_{EE}$, $V_{DD}$)

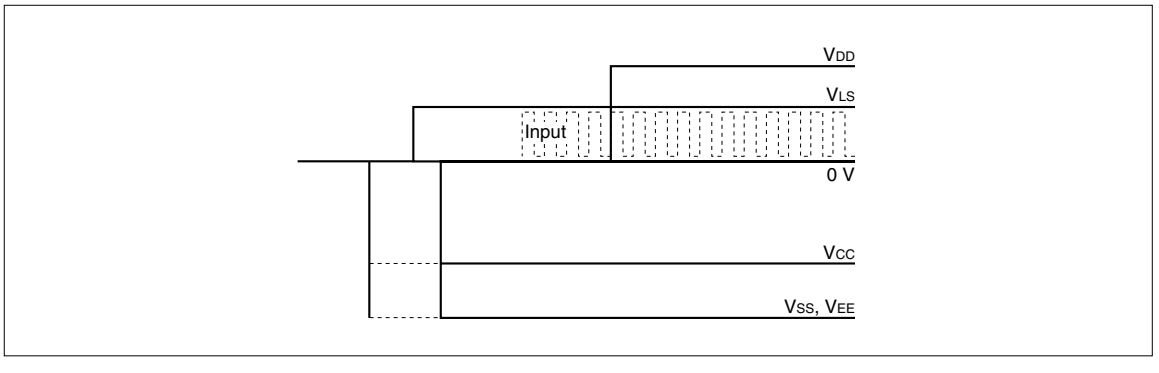
It is possible to set voltage $V_{EE}$ to the same as $V_{SS}$. When connecting the power supply when $V_{EE} = V_{SS}$, observe the following sequence and the recommended sequence figure shown below.

Logic system power supply ($V_{LS}$), internal logic system power supply ($V_{SS}$, $V_{CC}$; $V_{CC} > V_{SS}$) and low-level LCD drive power supply ($V_{EE}$) → logic input → high-level LCD drive power supply ($V_{DD}$)

When disconnecting the power supply, follow the reverse sequence.

Since the logic state of the internal circuit is unstable immediately after the logic system power is supplied, input CKV and SPV while initializing the internal circuit (minimum input clock number is 300 CKV).

$MODE_1$ and $MODE_2$ should be set to "L" during the initializing period for setting the LCD drive output to $V_{EE}$ level.




**Input pin setting**

Input pins other than CKV and SPV must be set to "H" or "L" level.

**Maximum ratings**

When connecting or disconnecting the power, this IC must be used within the range of the absolute maximum ratings.

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | APPLICABLE PINS | RATING | UNIT | NOTE |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | −0.3 to +45.0 | V | 1, 2 |
| | $V_{LS}$ | $V_{LS}$ | −0.3 to +7.0 | V | |
| | $V_{CC} - V_{SS}$ | $V_{CC}$, $V_{SS}$ | −0.3 to +7.0 | V | |
| | $V_{EE} - V_{SS}$ | $V_{EE}$, $V_{SS}$ | −0.3 to +45.0 | V | |
| | $V_{DD} - V_{EE}$ ($V_{SS}$) | $V_{DD}$, $V_{EE}$, $V_{SS}$ | −0.3 to +45.0 | V | |
| Input voltage | $V_{IN}$ | CKV, SPV, $CE_1$, $CE_2$, R/L, MODE1, MODE2, $TEST_1$, $TEST_2$ | −0.3 to $V_{LS}$ + 0.3 | V | |
| Storage temperature | $T_{STG}$ | | −45 to +125 | ˚C | |

**NOTES :**

1. $T_A$ = +25 ˚C
2. The maximum applicable voltage on any pin with respect to 0 V.

## RECOMMENDED OPERATING CONDITIONS

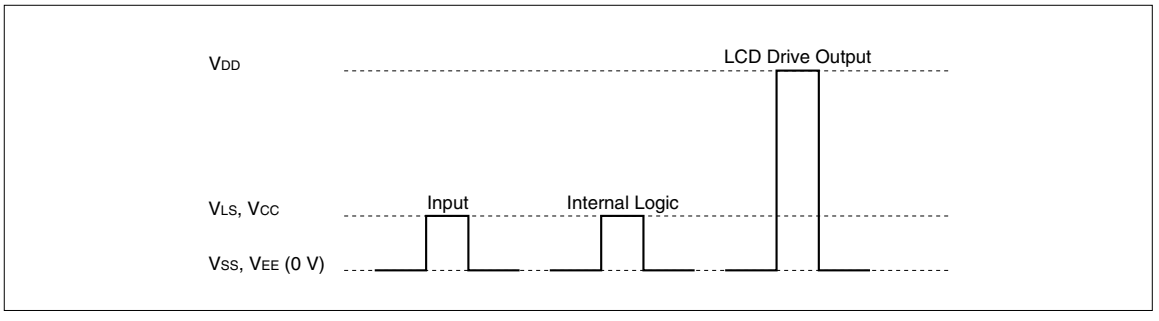
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | +5.5 | +9.0 | +42.0 | V | 1, 2 |
| | $V_{LS}$ | +3.0 | +5.0 | +5.5 | V | |
| | $V_{CC} - V_{SS}$ | +3.0 | +5.0 | +5.5 | V | |
| | $V_{EE} - V_{SS}$ | 0 | | +11.0 | V | |
| | $V_{DD} - V_{EE}$ ($V_{SS}$) | +16.0 | +25.0 | +42.0 | V | |
| Input voltage | $V_{IN}$ | 0 | | $V_{LS}$ | V | |
| Operating temperature | $T_{OPR}$ | −30 | | +85 | ˚C | |

**NOTES :**

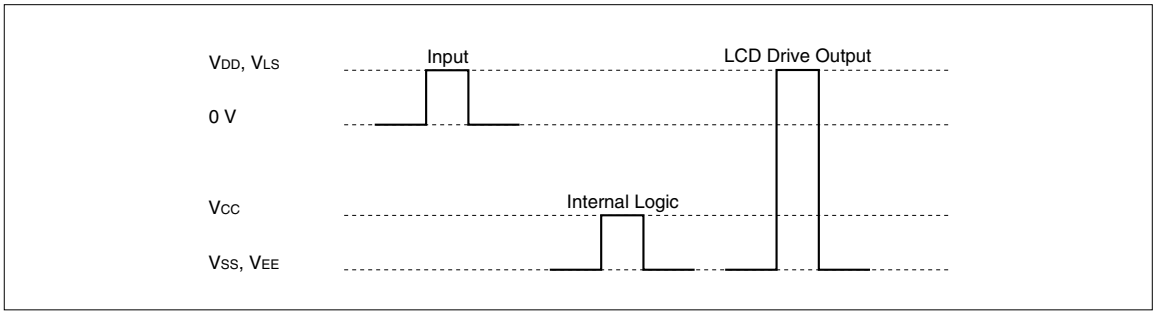
1. The applicable voltage on any pin with respect to 0 V.
2. Ensure that voltages are set as follows.
   $V_{SS}$, $V_{EE} \leq 0$ V
   $V_{CC} - V_{SS} = V_{LS} \pm 0.1$ V (For 3.3 V specifications)
   $V_{CC} - V_{SS} = V_{LS} \pm 0.2$ V (For 5.0 V specifications)
   $V_{CC} \leq V_{LS}$

When power supply pins are set as shown below, the LH1692 can output positive voltage and negative voltage to LCD drive output.

Example 1 : For Positive Voltage Output




Example 2 : For Negative Voltage Output



## ELECTRICAL CHARACTERISTICS

### DC Characteristics

($V_{LS}$ = +3.3±0.3 V (= $V_{CC}$ − $V_{SS}$), $V_{EE}$ = $V_{SS}$, $T_{OPR}$ = −30 to +85 °C)

| PARAMETER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL}$ | | CKV, SPV, MODE1, | | | 0.2$V_{LS}$ | V | |
| Input "High" voltage | $V_{IH}$ | | MODE2, CE1, CE2, R/L | 0.8$V_{LS}$ | | | V | |
| Output "Low" voltage | $V_{OL}$ | $I_{OL}$ = 0.4 mA | OG1-OG300 | | | $V_{EE}$ + 0.4 | V | |
| Output "High" voltage | $V_{OH}$ | $I_{OH}$ = −0.4 mA | | $V_{DD}$ − 0.4 | | | V | |
| Input "Low" current | $I_{IL}$ | $V_I$ = 0 V | CKV, SPV, MODE1, | | | 5.0 | µA | |
| Input "High" current | $I_{IH}$ | $V_I$ = $V_{LS}$ | MODE2, CE1, CE2, R/L | | | 5.0 | µA | 1 |
| Supply current (1) | $I_{DD}$ | For 1-pulse mode | | | | 60 | µA | 2 |
| | $I_{LS}$ | | | | | 130 | µA | |
| | $I_{CC}$ | | | | | 80 | µA | |
| | $I_{EE}$ | | | | | 50 | µA | |
| Supply current (2) | $I_{DD}$ | For jumping 2-pulse mode | | | | 130 | µA | 3 |
| | $I_{LS}$ | | | | | 200 | µA | |
| | $I_{CC}$ | | | | | 90 | µA | |
| | $I_{EE}$ | | | | | 50 | µA | |
| Supply current (3) | $I_{DD}$ | For continuous 2-pulse mode | | | | 130 | µA | 4 |
| | $I_{LS}$ | | | | | 200 | µA | |
| | $I_{CC}$ | | | | | 90 | µA | |
| | $I_{EE}$ | | | | | 90 | µA | |

**NOTES :**

1. All input pins : 3.3 V
2. CKV : Frequency = 31 kHz, "L" period width $t_{WL}$ = 16.2 µs
   SPV : Frequency = 60 Hz
   Other input pins : 3.3 V
   All output pins are opened.
3. CKV : Frequency = 31 kHz, "L" period width $t_{WL}$ = 16.2 µs
   SPV : Frequency = 60 Hz
   MODE2 : 0 V
   Other input pins : 3.3 V
   All output pins are opened.
4. CKV : Frequency = 31 kHz, "L" period width $t_{WL}$ = 16.2 µs
   SPV : Frequency = 60 Hz
   MODE1 : 0 V
   Other input pins : 3.3 V
   All output pins are opened.

($V_{LS}$ = +5.0±0.5 V (= $V_{CC}$ − $V_{SS}$), $V_{EE}$ = $V_{SS}$, $T_{OPR}$ = −30 to +85 °C)

| PARAMETER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL}$ | | CKV, SPV, $MODE_1$, | | | 0.2$V_{LS}$ | V | |
| Input "High" voltage | $V_{IH}$ | | $MODE_2$, $CE_1$, $CE_2$, R/L | 0.8$V_{LS}$ | | | V | |
| Output "Low" voltage | $V_{OL}$ | $I_{OL}$ = 0.4 mA | $OG_1$-$OG_{300}$ | | | $V_{EE}$ + 0.4 | V | |
| Output "High" voltage | $V_{OH}$ | $I_{OH}$ = −0.4 mA | | $V_{DD}$ − 0.4 | | | V | |
| Input "Low" current | $I_{IL}$ | $V_I$ = 0 V | CKV, SPV, $MODE_1$, | | | 5.0 | µA | |
| Input "High" current | $I_{IH}$ | $V_I$ = $V_{LS}$ | $MODE_2$, $CE_1$, $CE_2$, R/L | | | 5.0 | µA | 1 |
| Supply current (1) | $I_{DD}$ | For 1-pulse mode | | | | 60 | µA | 2 |
| | $I_{LS}$ | | | | | 180 | µA | |
| | $I_{CC}$ | | | | | 100 | µA | |
| | $I_{EE}$ | | | | | 50 | µA | |
| Supply current (2) | $I_{DD}$ | For jumping 2-pulse mode | | | | 130 | µA | 3 |
| | $I_{LS}$ | | | | | 300 | µA | |
| | $I_{CC}$ | | | | | 150 | µA | |
| | $I_{EE}$ | | | | | 50 | µA | |
| Supply current (3) | $I_{DD}$ | For continuous 2-pulse mode | | | | 130 | µA | 4 |
| | $I_{LS}$ | | | | | 300 | µA | |
| | $I_{CC}$ | | | | | 150 | µA | |
| | $I_{EE}$ | | | | | 50 | µA | |

**NOTES :**

1. All input pins : 5 V
2. CKV : Frequency = 31 kHz, "L" period width $t_{WL}$ = 16.2 µs
   SPV : Frequency = 60 Hz
   Other input pins : 5 V
   All output pins are opened.
3. CKV : Frequency = 31 kHz, "L" period width $t_{WL}$ = 16.2 µs
   SPV : Frequency = 60 Hz
   $MODE_2$ : 0 V
   Other input pins : 5 V
   All output pins are opened.
4. CKV : Frequency = 31 kHz, "L" period width $t_{WL}$ = 16.2 µs
   SPV : Frequency = 60 Hz
   $MODE_1$ : 0 V
   Other input pins : 5 V
   All output pins are opened.

## AC Characteristics

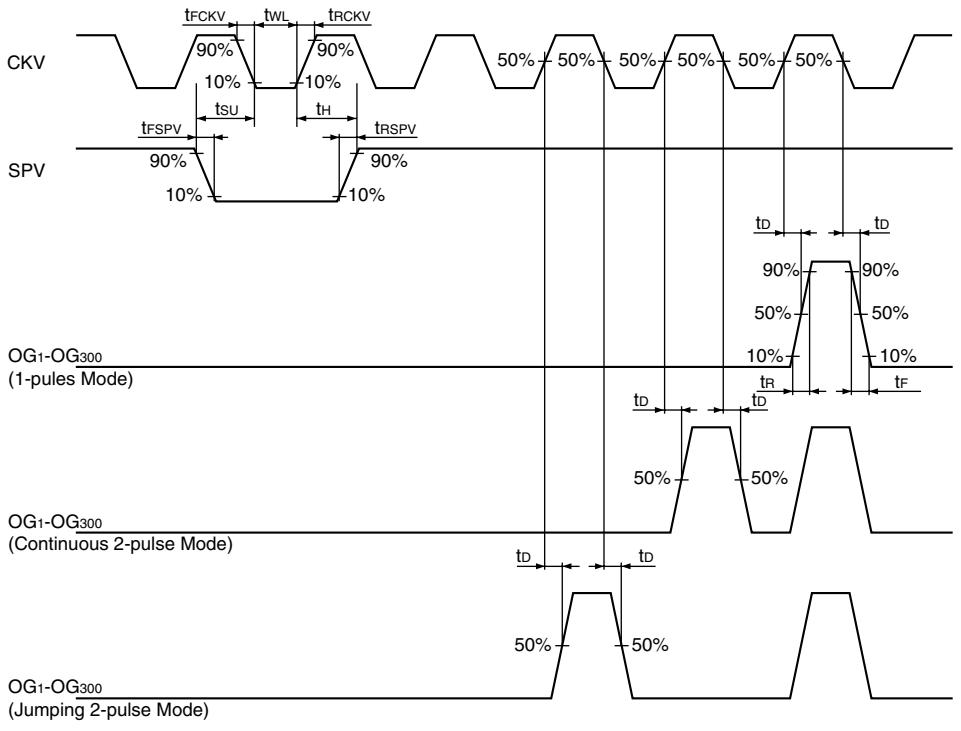
($V_{LS}$ = +3.3±0.3 V (= $V_{CC}$ – $V_{SS}$), $V_{EE}$ = $V_{SS}$, $T_{OPR}$ = –30 to +85 ˚C)

| PARAMETER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Clock frequency | $f_{CKV}$ | | CKV | | | 100 | kHz |
| "L" clock pulse width | $t_{WL}$ | | | 0.5 | | | µs |
| Clock rise time | $t_{RCKV}$ | | | | | 100 | ns |
| Clock fall time | $t_{FCKV}$ | | | | | 100 | ns |
| Data setup time | $t_{SU}$ | | CKV, SPV | 100 | | | ns |
| Data hold time | $t_H$ | | | 300 | | | ns |
| Pulse rise time | $t_{RSPV}$ | | SPV | | | 100 | ns |
| Pulse fall time | $t_{FSPV}$ | | | | | 100 | ns |
| Output transfer delay time | $t_D$ | $C_L$ = 500 pF | $OG_1$-$OG_{300}$ | | | 3.0 | µs |
| Output rise time | $t_R$ | | | | | 1.0 | µs |
| Output fall time | $t_F$ | | | | | 1.0 | µs |

($V_{LS}$ = +5.0±0.5 V (= $V_{CC}$ – $V_{SS}$), $V_{EE}$ = $V_{SS}$, $T_{OPR}$ = –30 to +85 ˚C)

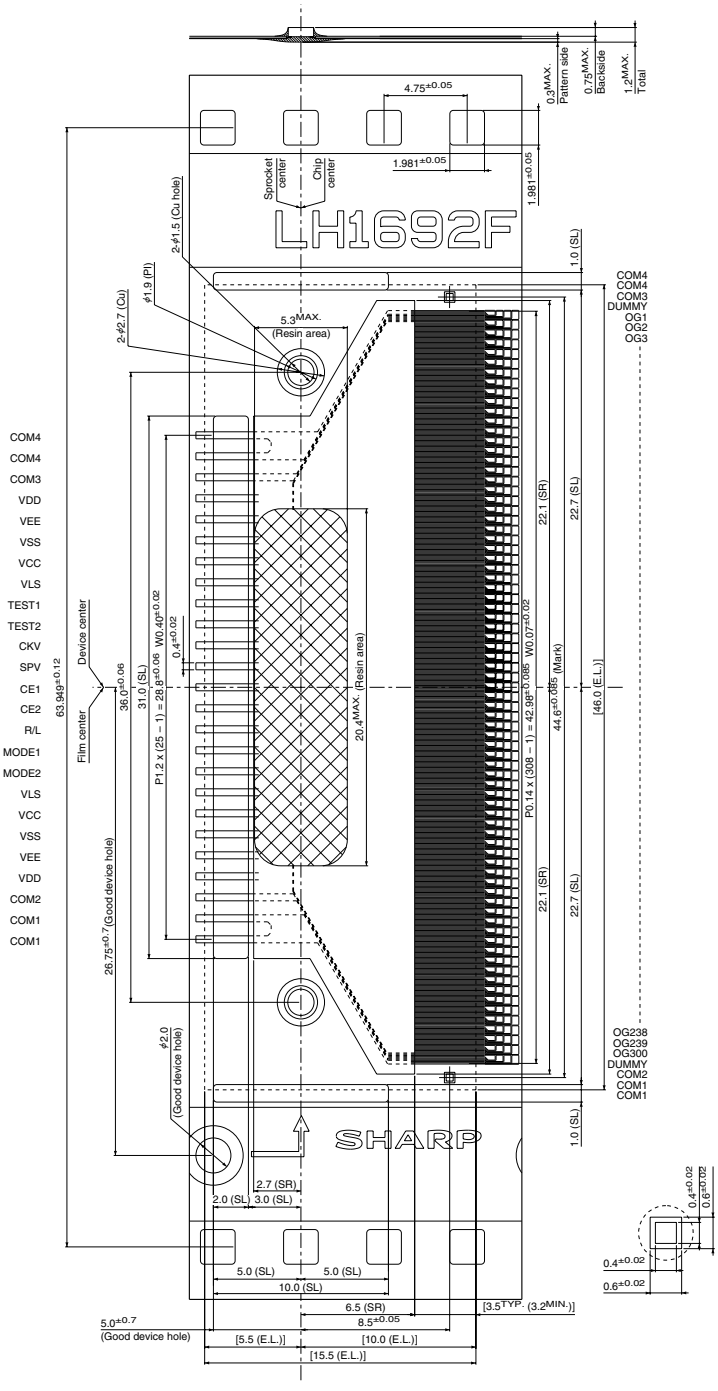
| PARAMETER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Clock frequency | $f_{CKV}$ | | CKV | | | 100 | kHz |
| "L" clock pulse width | $t_{WL}$ | | | 0.5 | | | µs |
| Clock rise time | $t_{RCKV}$ | | | | | 100 | ns |
| Clock fall time | $t_{FCKV}$ | | | | | 100 | ns |
| Data setup time | $t_{SU}$ | | CKV, SPV | 100 | | | ns |
| Data hold time | $t_H$ | | | 300 | | | ns |
| Pulse rise time | $t_{RSPV}$ | | SPV | | | 100 | ns |
| Pulse fall time | $t_{FSPV}$ | | | | | 100 | ns |
| Output transfer delay time | $t_D$ | $C_L$ = 500 pF | $OG_1$-$OG_{300}$ | | | 2.0 | µs |
| Output rise time | $t_R$ | | | | | 1.0 | µs |
| Output fall time | $t_F$ | | | | | 1.0 | µs |

## Timing Chart



## PACKAGE

(Unit : mm)




● Tape Material

| | |
|---|---|
| Substrate | UPILEX S75 |
| Adhesive | #7100 |
| Cu foil [thickness] | USLP 18 µm |
| Solder resist | Epoxy resin |

● Tape Specification

| | |
|---|---|
| Tape width | 70 mm |
| Tape type | Wide |
| Perforation pitch | 4 pitches |

**LH1692F**

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