DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT594
8-bit shift register with output register

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

8-bit shift register with output register 74HC/HCT594

FEATURES

- Synchronous serial input and output
- 8-bit parallel output
- Shift and storage register have independent direct clear and clocks
- 100 MHz (typ.)
- Output capability:
  - parallel outputs: bus driver
  - serial outputs: standard
- I_{CC} category: MSI

APPLICATIONS

- Serial-to parallel data conversion
- Remote control holding register

DESCRIPTION

The 74HC/HCT594 are high-speed, Si-gate CMOS devices, and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.
The 74HC/HCT594 contain an 8-bit, non-inverting, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clears are provided on both the shift and storage registers. A serial output (Q_7') is provided for cascading purposes.

Both the shift and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

QUICK REFERENCE DATA

GND = 0 V: T_{amb} = 250 C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	SH_{CP} to Q_7'		13	15	ns
	ST_{CP} to Q_n		13	15	ns
	$\overline{SH}_R$ to Q_n		11	14	ns
	$\overline{ST}_R$ to Q_n		11	14	ns
f_{max}	maximum clock frequency SH_{CP}, ST_{CP}		100	100	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	84	89	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$, where:
   f_i = input frequency in MHz; f_o = output frequency in MHz;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs;
   C_L = output load capacitance in pF; V_{CC} = supply voltage in V.
2. For HC, the condition is V_I = GND to V_{CC}; for HCT, the condition is V_I = GND to V_{CC} – 1.5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
PC74HC/HCT594P	16	DIL	plastic	SOT38C, P
PC74HC/HCT594T	16	SO	plastic	SOT109A

8-bit shift register with output register 74HC/HCT594

PINNING

SYMBOL	PIN	DESCRIPTION
Q_0 to Q_7	15 & 1 to 7	parallel data outputs
GND	8	ground (0 V)
Q_7'	9	serial data output
$\overline{SH}_R$	10	shift register reset (active LOW)
SH_{CP}	11	shift register clock input
ST_{CP}	12	storage register clock input
$\overline{ST}_R$	13	storage register reset active (LOW)
D_s	14	serial data input
V_{CC}	16	supply voltage

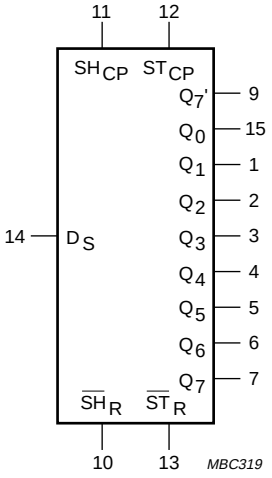


Fig.1 Logic symbol.

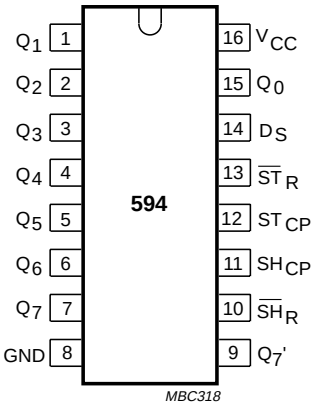


Fig.2 Pin configuration.

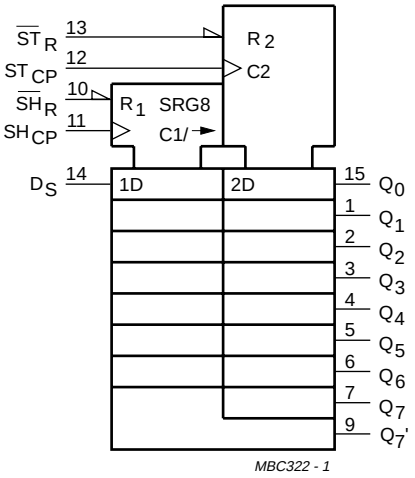


Fig.3 IEC logic symbol.

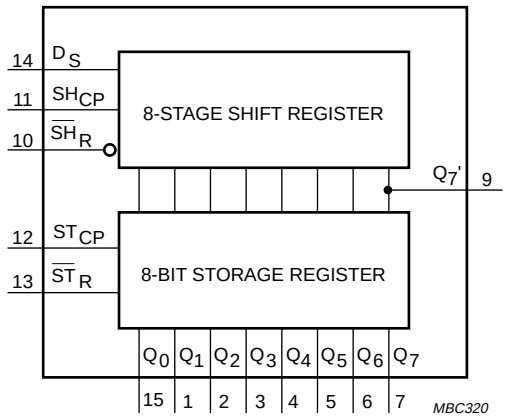


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTION
SH_{CP}	ST_{CP}	$\overline{SH}_R$	$\overline{ST}_R$	D_S	Q_7'	Q_n	
X	X	L	X	X	L	NC	a LOW level on $\overline{SH}_R$ only affects the shift registers.
X	X	X	L	X	NC	L	a LOW level on $\overline{ST}_R$ only affects the storage registers.
X	↑	L	H	X	L	L	empty shift register loaded into storage register.
↑	X	H	X	H	Q_6'	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q_6') appears on the serial output (Q_7').
X	↑	H	H	X	NC	Q_n'	contents of shift register stages (internal Q_n') are transferred to the storage register and parallel output stages.
↑	↑	H	H	X	Q_6n	Q_n'	contents of shift register shifted through. Previous contents of shift register transferred to the storage register and the parallel output stages.

Note

1. H = HIGH voltage level
   L = LOW voltage level
   ↑ = LOW-to-HIGH transition
   NC = no change
   X = don't care.

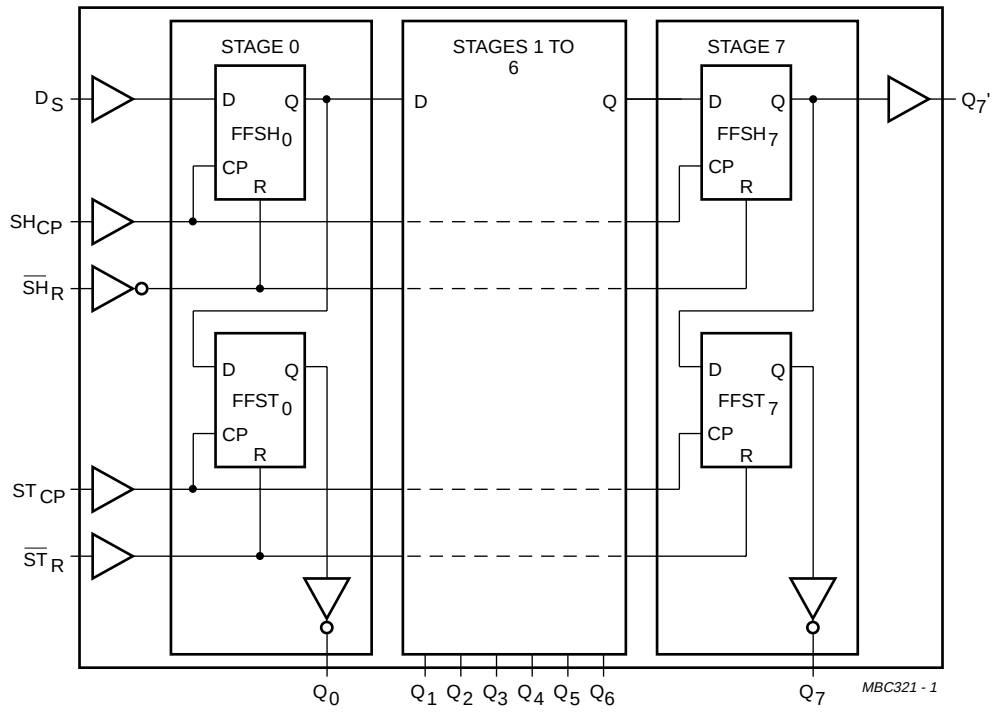


Fig.5 Logic diagram.

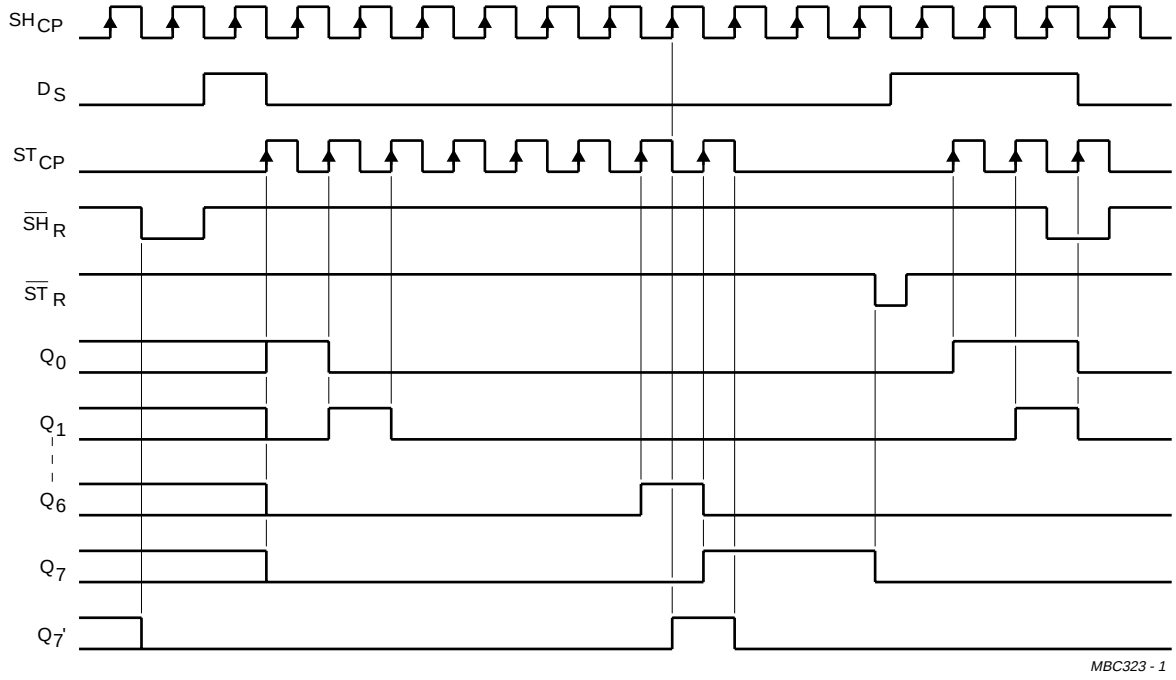


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics, see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: parallel outputs, bus driver; serial output, standard.
I_{CC} category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	– – –	44 16 14	150 30 26	– – –	185 37 31	– – –	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.7
	propagation delay ST_{CP} to Q_n	– – –	44 16 14	150 30 26	– – –	185 37 31	– – –	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.8
t_{PHL}	propagation delay $\overline{SH}_R$ to Q_7'	– – –	39 14 12	150 30 26	– – –	185 37 31	– – –	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.11
	propagation delay $\overline{ST}_R$ to Q_n	– – –	39 14 12	125 25 21	– – –	155 31 26	– – –	185 37 31	ns ns ns	2.0 4.5 6.0	Fig.12
t_W	shift clock pulse width HIGH or LOW	80 16 14	10 4 3	– – –	100 20 17	– – –	120 24 20	– – –	ns ns ns	2.0 4.5 6.0	Fig.7
	storage clock pulse width HIGH or LOW	80 16 14	10 4 3	– – –	100 20 17	– – –	120 24 20	– – –	ns ns ns	2.0 4.5 6.0	Fig.8
	shift and storage reset pulse width HIGH or LOW	80 16 14	14 5 4	– – –	100 20 17	– – –	120 24 20	– – –	ns ns ns	2.0 4.5 6.0	Fig.11 and Fig.12
t_{su}	set-up time D_s to SH_{CP}	100 20 17	10 4 3	– – –	125 25 21	– – –	150 30 26	– – –	ns ns ns	2.0 4.5 6.0	Fig.9
	set-up time $\overline{SH}_R$ to ST_{CP}	100 20 17	14 5 4	– – –	125 25 21	– – –	150 30 26	– – –	ns ns ns	2.0 4.5 6.0	Fig.10
	set-up time SH_{CP} to ST_{CP}	100 20 17	17 6 5	– – –	125 25 21	– – –	150 30 26	– – –	ns ns ns	2.0 4.5 6.0	Fig.8

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time D_s to SH_{CP}	25 5 4	–8 –3 –2	– – –	30 6 5	– – –	35 7 6	– – –	ns ns ns	2.0 4.5 6.0	Fig.9
t_{rem}	removal time $\overline{SH}_R$ to SH_{CP}, $\overline{ST}_R$ to ST_{CP}	50 10 9	–14 –5 –4	– – –	65 13 11	– – –	75 15 13	– – –	ns ns ns	2.0 4.5 6.0	Fig.11 and Fig.12
f_{max}	maximum clock frequency SH_{CP} or ST_{CP}	6.0 30 35	30 92 109	– – –	4.8 24 28	– – –	4.0 20 24	– – –	MHz MHz MHz	2.0 4.5 6.0	Fig.7 and Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics, see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: parallel outputs, bus driver; serial output, standard.

I_{CC} category: MSI.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the following table.

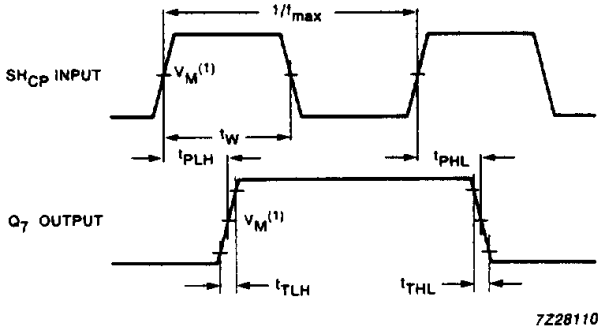
INPUT	UNIT LOAD COEFFICIENT
D_s	0.25
$\overline{SH}_R$	1.50
SH_{CP}	1.50
ST_{CP}	1.50
$\overline{ST}_R$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

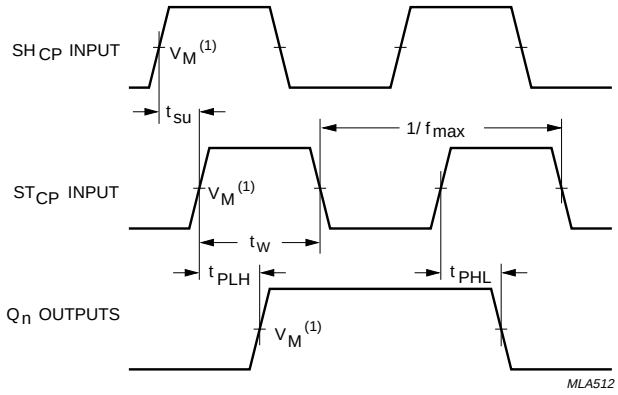
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	–	18	32	–	40	–	48	ns	4.5	Fig.7
	propagation delay ST_{CP} to Q_n	–	18	32	–	40	–	48	ns	4.5	Fig.8
t_{PHL}	propagation delay $\overline{SH}_R$ to Q_7'	–	17	30	–	38	–	45	ns	4.5	Fig.11
	propagation delay $\overline{ST}_R$ to Q_n	–	17	30	–	38	–	45	ns	4.5	Fig.12
t_W	shift clock pulse width HIGH or LOW	16	4	–	20	–	24	–	ns	4.5	Fig.7
	storage clock pulse width HIGH or LOW	16	4	–	20	–	24	–	ns	4.5	Fig.8
	shift and storage reset pulse width HIGH or LOW	16	6	–	20	–	24	–	ns	4.5	Fig.11 and Fig.12
t_{su}	set-up time D_s to SH_{CP}	20	4	–	25	–	30	–	ns	4.5	Fig.9
	set-up time $\overline{SH}_R$ to ST_{CP}	20	6	–	25	–	30	–	ns	4.5	Fig.10
	set-up time SH_{CP} to ST_{CP}	20	7	–	25	–	30	–	ns	4.5	Fig.8
t_h	hold time D_s to SH_{CP}	5	–3	–	6	–	7	–	ns	4.5	Fig.9
t_{rem}	removal time $\overline{SH}_R$ to SH_{CP}, $\overline{ST}_R$ to ST_{CP}	10	–5	–	13	–	15	–	ns	4.5	Fig.11 and Fig.12
f_{max}	maximum clock frequency SH_{CP} or ST_{CP}	30	92	–	24	–	20	–	MHz	4.5	Fig.7 and Fig.8

AC WAVEFORMS



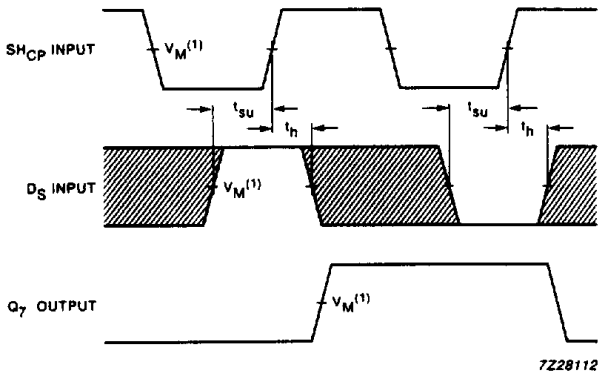
(1) HC: V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V

Fig.7 Waveforms showing the shift clock (SH_{CP}) to output (Q_7') propagation delays, the shift clock pulse width and the maximum shift clock frequency.



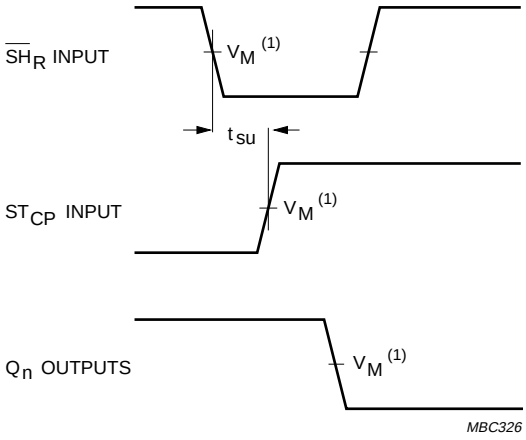
(1) HC: V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V

Fig.8 Waveforms showing the storage clock (ST_{CP}) to output (Q_n) propagation delays, the storage clock pulse width, maximum storage clock frequency and the shift clock to storage clock set-up time.



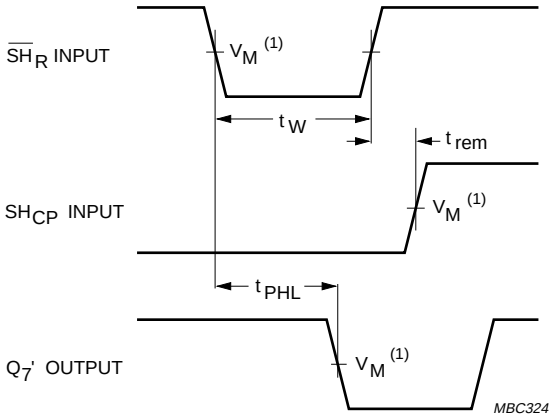
(1) HC: V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V

Fig.9 Waveforms showing the data set-up and hold times for the D_s input.



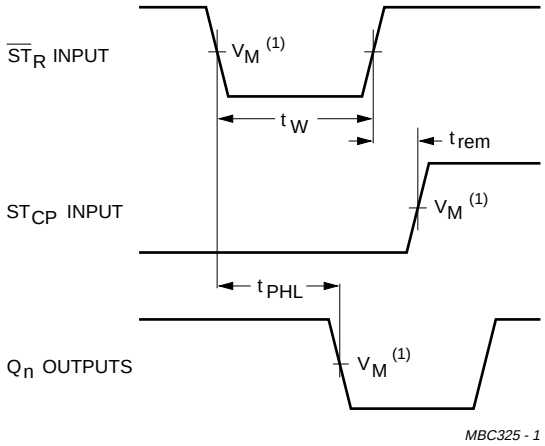
(1) HC: V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V

Fig.10 Waveforms showing the set-up time from shift reset ($\overline{SH}_R$) to storage clock (ST_{CP}).



(1) HC: V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V

Fig.11 Waveforms showing the shift reset ($\overline{SH}_R$) pulse width, the shift reset to output (Q_7') propagation delay and the shift reset to shift clock (SH_{CP}) removal time.



(1) HC: V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V

Fig.12 Waveforms showing the storage reset ($\overline{ST}_R$) pulse width, the storage reset to outputs (Q_n) propagation delay and the storage reset to storage clock (ST_{CP}) removal time.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.