SPECIFICATION

for

MRD520A

Dual Channel F2F Decoder IC

Uniform Industrial Corp.

APPROVED BY	CHECK BY	PREPARED BY

CONTENTS

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Dual Channel F2F Decoder IC
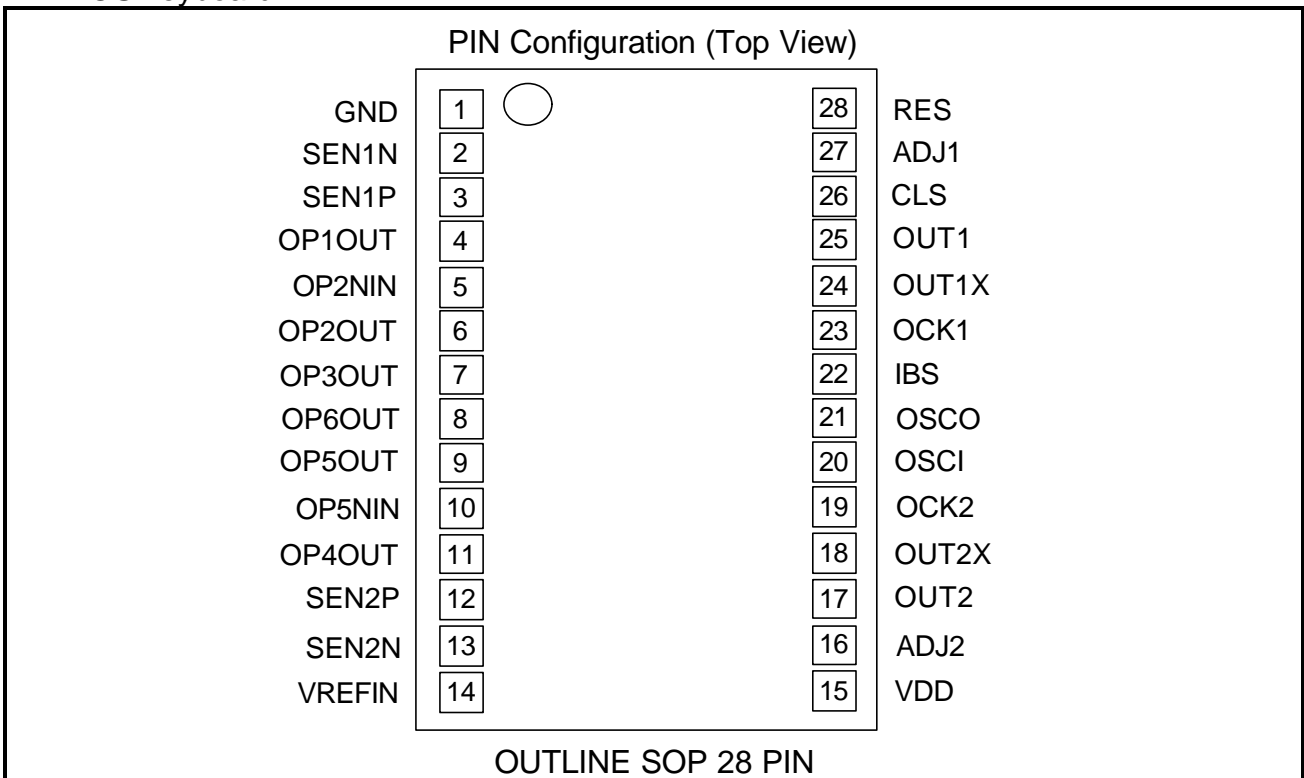
1. DESCRIPTION

The MRD520A is a 1.2um CMOS integrated circuit for purpose of amplification and decoding for F2F magnetic stripe encoding card reader.

2. FEATURES

- Integrated Amplification Circuitry for magnetic head signals.
- Number of start bits (4/8 bits) to ignore selectable.
- Both output polarity supported.
- Adjustable read data output clock pulse width.
- Dual channel support for 75/210 BPI recording density.
- Magnetic head data input frequency range from 300 bit/sec to 12600 bit/sec.
- Idle mode controllable by external hardware or micro-processor.

3. APPLICATIONS

- Magnetic stripe card reader.
- POS keyboard.

PIN Configuration (Top View)

Pin	Name		Pin	Name
GND	1		28	RES
SEN1N	2		27	ADJ1
SEN1P	3		26	CLS
OP1OUT	4		25	OUT1
OP2NIN	5		24	OUT1X
OP2OUT	6		23	OCK1
OP3OUT	7		22	IBS
OP6OUT	8		21	OSCO
OP5OUT	9		20	OSCI
OP5NIN	10		19	OCK2
OP4OUT	11		18	OUT2X
SEN2P	12		17	OUT2
SEN2N	13		16	ADJ2
VREFIN	14		15	VDD

OUTLINE SOP 28 PIN

4. PIN DESCRIPTION

1	GND	
2	SEN1N	Input from magnetic head
3	SEN1P	Input from magnetic head
4	OP1OUT	Amplifier OP1 output
5	OP2NIN	Amplifier OP2 - input
6	OP2OUT	Amplifier OP2 output
7	OP3OUT	Amplifier OP3 output
8	OP6OUT	Amplifier OP6 output
9	OP5OUT	Amplifier OP5 output
10	OP5NIN	Amplifier OP5 - input
11	OP4OUT	Amplifier OP4 output
12	SEN2P	Amplifier OP4 + input
13	SEN2N	Amplifier OP4 - input
14	VREFIN	Reference voltage for analog signal processing
15	VDD	
16	ADJ2	Adjust read out clock pulse width for F2F channel 2
17	OUT2	Positive read out data for F2F channel 2
18	OUT2X	Negative read out data for F2F channel 2
19	OCK2	Negative read out clock for F2F channel 2
20	OSCI	RC oscillator input
21	OSCO	RC oscillator output
22	IBS	Select ignore leading bit, "LOW" for 4 bits and "HIGH" for 8 bits
23	OCK1	Negative read out clock for F2F channel 1
24	OUT1X	Negative read out data for F2F channel 1
25	OUT1	Positive read out data for F2F channel 1
26	CLS	Card Loading Signal output, "LOW" after ignore bits, "HIGH" if no input for around 12.5mS
27	ADJ1	Adjust read out clock pulse width for F2F channel 1
28	RES	Power on reset, LOW reset the logic circuit and enter idle mode. Approx. 10mS after HIGH level to normal function

5. FUNCTION DESCRIPTION

Data signal inputs read from a magnetic card via a magnetic head are fed into the SEN1P and SEN1N (SEN2P and SEN2N) pins, amplified and wave shaped by internal analog circuitry, then converted to logic level F2F data format. Once the F2F signals are detected, the decoding logic ignores the leading 4 or 8 bits (set by IBS pin), via the ignored bits the reference bit length is determined. The succeeding inputs are identified as bit 0 or 1 by the average bit length of preceding two bits, if the data toggles before 70% of the reference bit length then the data is identified as a "1" bit and the next data toggle regarded as the beginning of next data bit. If the data toggles after 70% of the reference bit length then the data is identified as a "0" bit and the current data toggle is as the beginning of next data.

After the ignored bits, then pin CLS will be pulled low, the succeeding data bit will be shifted out after the beginning of next data bit.

The pin OCK1 (OCK2) will be pulled low after the next data is detected and a 12uS delay inserted, it will be kept low for 14 to 60uS depending on the external resistor connected to pin ADJ1 (ADJ2). If the next bit comes before OCK1 (OCK2) goes high, then OCK1 (OCK2) will be forced to pull high and then begins next cycle, it means that the data signals will be ready before OCK1 (OCK2) goes low and stay valid till 12uS before next down edge of OCK1 (OCK2).

6. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Supply Voltage	VDD	-0.5 to +7.0	V
VIN1	Input Voltage	IBS,OSCI,RES,ADJ1,ADJ2	-0.5 to VCC +0.5	V
VIN2	Input Voltage	OP2NIN,OP5NIN	-0.5 to VCC +0.5	V
IO	Output Current	OP1OUT,OP2OUT,OP3OUT, OP4OUT,OP5OUT,OP6OUT, OSCO2,OUT2,OUT2X,OUT1, OUT1X,OCK1,OCK2	-10 to +10	mA
VID	Differential Input Voltage	SEN1P ~ SEN1N, SEN2P ~SEN2N	-1.0 to +1.0	V
TOPR	Operating Temperature		-10 to +70	
TSTG	Storage Temperature		-50 to +140	

7. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
VCC	Supply Voltage		4.5	5	5.5	V
VIH	Input High Voltage	IBS, RES	VCC -0.5		VCC +0.5	V
VIL	Input Low Voltage	IBS, RES	-0.5	0	0.5	V
IOH	Output High Source Current at VOH=VCC -0.4	OCK1,OUT1,OUT1X, OCK2, OUT2,OUT2X	-1.5			mA
IOH	Output High Source Current at VOH=VCC -0.4	CLS	-0.1			mA
IOL	Output Low Sink Current at VOL=0.4	OCK1,OUT1,OUT1X, OCK2,OUT2, OUT2X,CLS	3			mA
VIN	Differential Input Voltage	SEN1P ~ SEN1N SEN2P ~ SEN2N	5		80	mV
FIN	Input Frequency	SEN1P ~ SEN1N SEN2P ~ SEN2N	300		13000	Hz
FOSC	Oscillation Frequency			2.3		MHz
ROSC	External resistor between OSCI & OSCO			30		Kohm
IOPR	Signal input at 12.6K bps			3.4	4.0	mA
ISBY	No signal input			2.5	3.0	mA
IDLE	Reset = Vss			1.6	2.0	mA

8. APPLICATION CIRCUIT
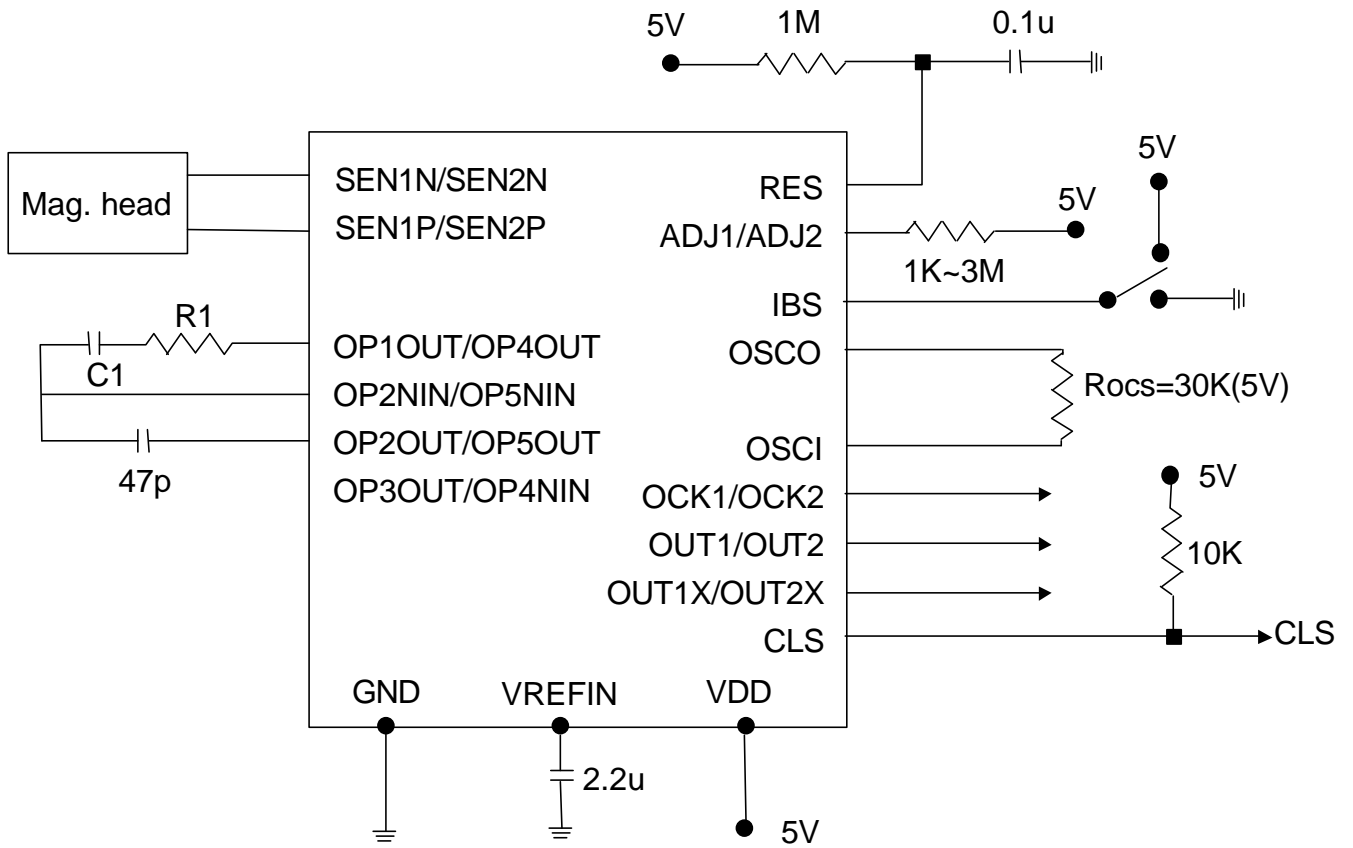
Note :

	TK1	TK2
R1	3.3K	22K
C1	3300p	4700p

9. TIMING DIAGRAM FOR MRD520A
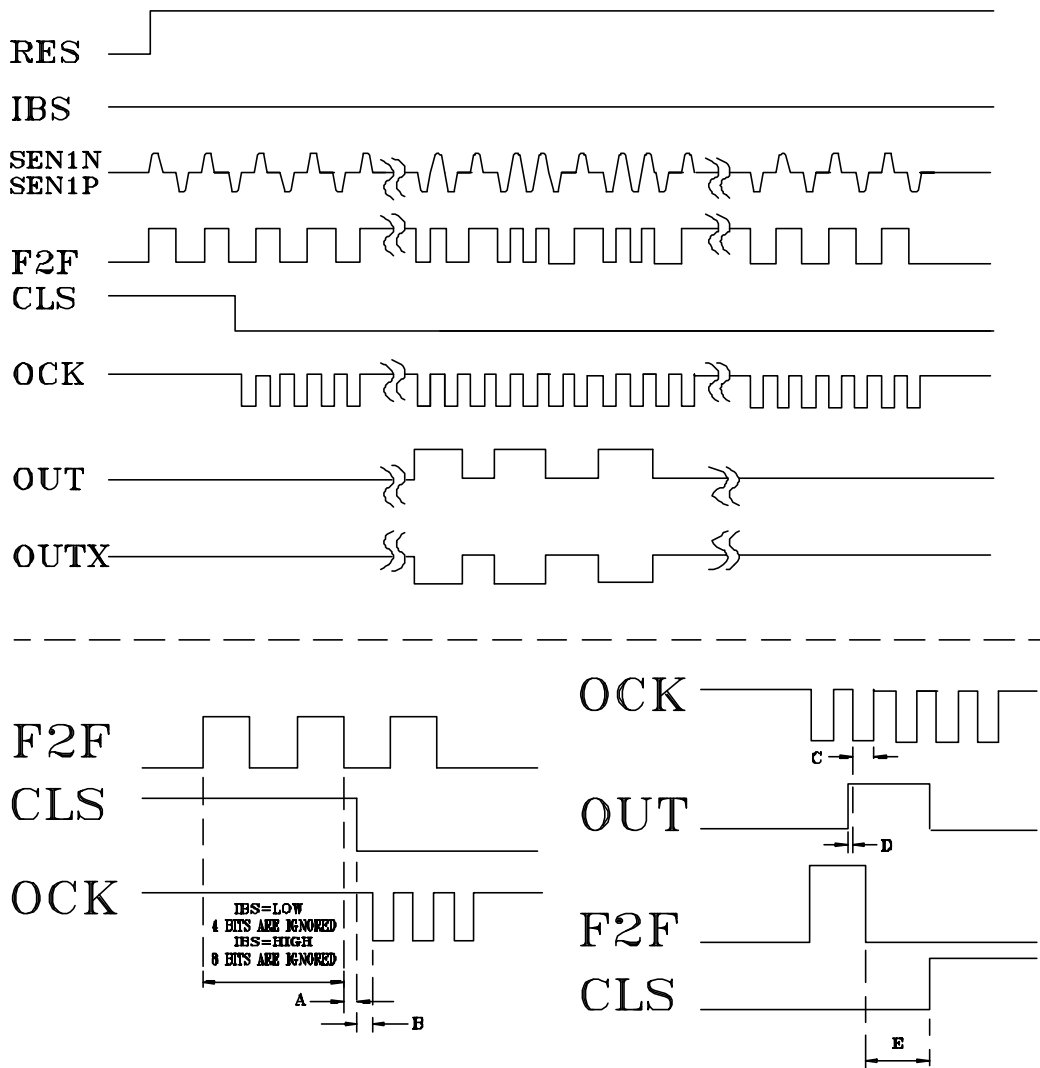
Time width of the A, B, C, D, E :

A   Approximate 2.4uS
B   One data bit
C   Adjustable from 14uS to 60uS
D   Approximate 12uS
E   Approximate 12.5mS if Rosc=30K

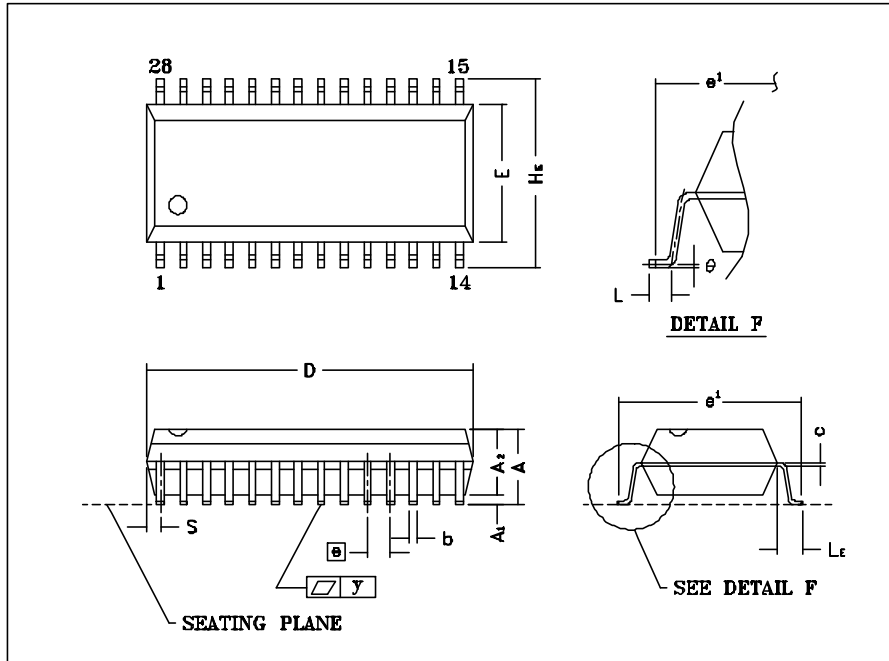# 10. OUTLINE DIMENSION

Symbol	Dimensions in inch	Dimensions in mm
A	0.110 Max.	2.79 Max.
A1	0.004 Min.	0.10 Min.
A2	0.093 +/-0.005	2.36 +/-0.13
b	0.016 +0.004 -0.002	0.410 +0.10 -0.05
c	0.010 +0.004 -0.002	0.254 +0.10 -0.05
D	0.705 typ (0.725 Max)	17.91 typ (18.42 Max)
E	0.295 +/-0.005	7.49 +/-0.13
$\boxed{e}$	0.050 +/-0.006	1.270 +/-0.15
e^1	0.370 NOM	9.40 NOM
H_E	0.406 +/-0.012	10.31 +/-0.31
L	0.036 +/-0.008	0.91 +/-0.20
L_E	0.055 +/-0.008	1.40 +/-0.20
S	0.043 Max.	1.09 Max.
y	0.006 Max.	0.15 Max.
	0° ~ 10°	0° ~ 10°

Note :
   a The max. value of dimension D included end flash.
   b The dimension E exclude resin lins.
   c The dimension E is for PCB surface mount pad pitch design reference only.
   d The dimension S included end flash.
   e All dimension are based in British system.