4M x 4Bit CMOS Quad CAS DRAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x 4 bit Quad $\overline{CAS}$ with Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle (2K Ref. or 4K Ref.), access time (-5 or -6), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. Four separate $\overline{CAS}$ pins provide for seperate I/O operation allowing this device to operate in parity mode.

This 4Mx4 Fast Page Mode Quad $\overline{CAS}$ DRAM family is fabricated using Samsung′s advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- **Part Identification**

  - KM44C4003C/C-L (5V, 4K Ref.)
  - KM44C4103C/C-L (5V, 2K Ref.)

- **Active Power Dissipation**

Unit : mW

Speed	Refresh Cycle	
	4K	2K
-5	495	605
-6	440	550

- **Refresh Cycles**

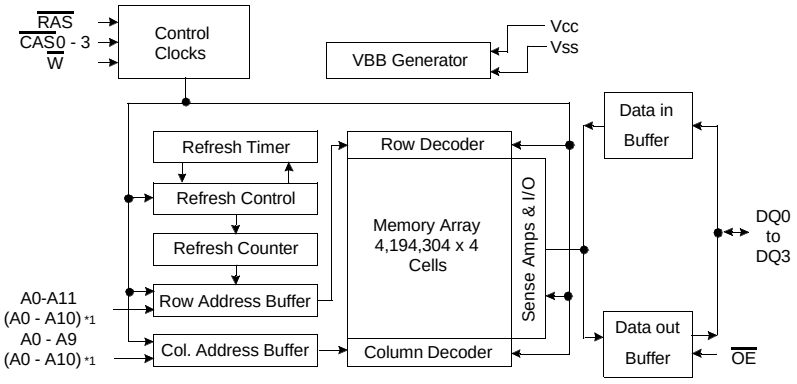
Part NO.	Refresh cycle	Refresh period	
		Normal	L-ver
C4003C	4K	64ms	128ms
C4103C	2K	32ms	

- **Performance Range**

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}	Remark
-5	50ns	13ns	90ns	35ns	5V/3.3V
-6	60ns	15ns	110ns	40ns	5V/3.3V

- Fast Page Mode operation
- Four seperate $\overline{CAS}$ pins provide for separate I/O operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast paralleltest mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 2K Refresh

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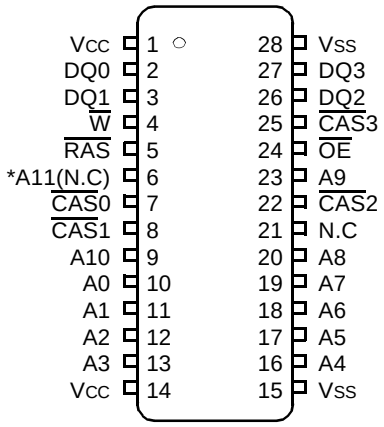
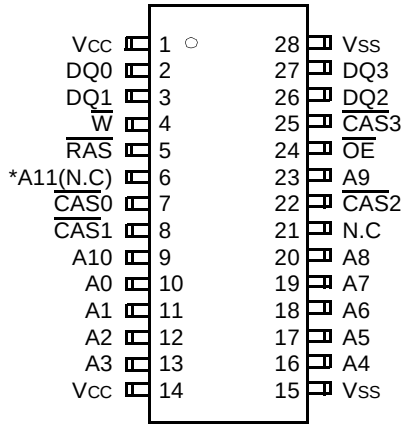
PIN CONFIGURATION (Top Views)

• **KM44C40(1)03CK**



• **KM44C40(1)03CS**



*A11 is N.C for KM44C4103C(5V, 2K Ref. product)

K : 300mil 28 SOJ
S : 300mil 28 TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A10	Address Inputs (2K Product)
DQ0 - 3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$0~$\overline{CAS}$3	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC} Inputs	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1.0*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}
*2 : -2.0/20ns, Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤V_{IN}+0.5V, all other input pins not under test=0 Volt)	$I_{I(L)}$	-5	5	uA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})	$I_{O(L)}$	-5	5	uA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			KM44C4003C	KM44C4103C	
I_{CC1}	Don't care	-5 -6	90 80	110 100	mA mA mA
I_{CC2}	Normal L	Don't care	2 1	2 1	mA mA
I_{CC3}	Don't care	-5 -6	90 80	110 100	mA mA mA
I_{CC4}	Don't care	-5 -6	80 70	90 80	mA mA mA
I_{CC5}	Normal L	Don't care	1 250	1 250	mA uA
I_{CC6}	Don't care	-5 -6	90 80	110 100	mA mA mA
I_{CC7}	L	Don't care	300	300	uA
I_{CCS}	L	Don't care	250	250	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @t_{RC}=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @t_{PC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V,

DQ=Don't care, T_{RC}=31.25us(4K/L-ver), 62.5us(2K/L-ver), T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11=V_{CC}-0.2V or 0.2V,

DQ0 ~ DQ3=V_{CC}-0.2V, 0.2V or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6} address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$x, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition : V_{CC}=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V

Parameter	Symbol	-5		-6		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5,18
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3,18
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	14
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	17
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4,16
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	15
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	16
Column address hold time	t_{CAH}	10		10		ns	16
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to	t_{RCH}	0		0		ns	8,15
Read command hold time referenced to	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	14
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	17

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		Units	Notes
		Min	Max	Min	Max		
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period (2K, Normal)	t_{REF}		32		32	ms	
Refresh period (4K, Normal)	t_{REF}		64		64	ms	
Refresh period (L-ver)	t_{REF}		128		128	ms	
Write command set-up time	t_{WCS}	0		0		ns	7,16
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7,14
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	15
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3,15
Fast Page mode cycle time	t_{PC}	35		40		ns	19
Fast Page read-modify-write cycle time	t_{PRWC}	76		85		ns	19
$\overline{CAS}$ precharge time (Fast Page cycle)	t_{CP}	10		10		ns	20
$\overline{RAS}$ pulse width (Fast Page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	21
$\overline{OE}$ to data delay	t_{OED}	13		15		ns	22
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	6
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		ns	11
Write command hold time (Test mode in)	t_{WTH}	10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		us	25,26,27
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	90		110		ns	25,26,27
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		ns	25,26,27
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	t_{CLCH}	5		5		ns	13,24

TEST MODE CYCLE

(Note 11)

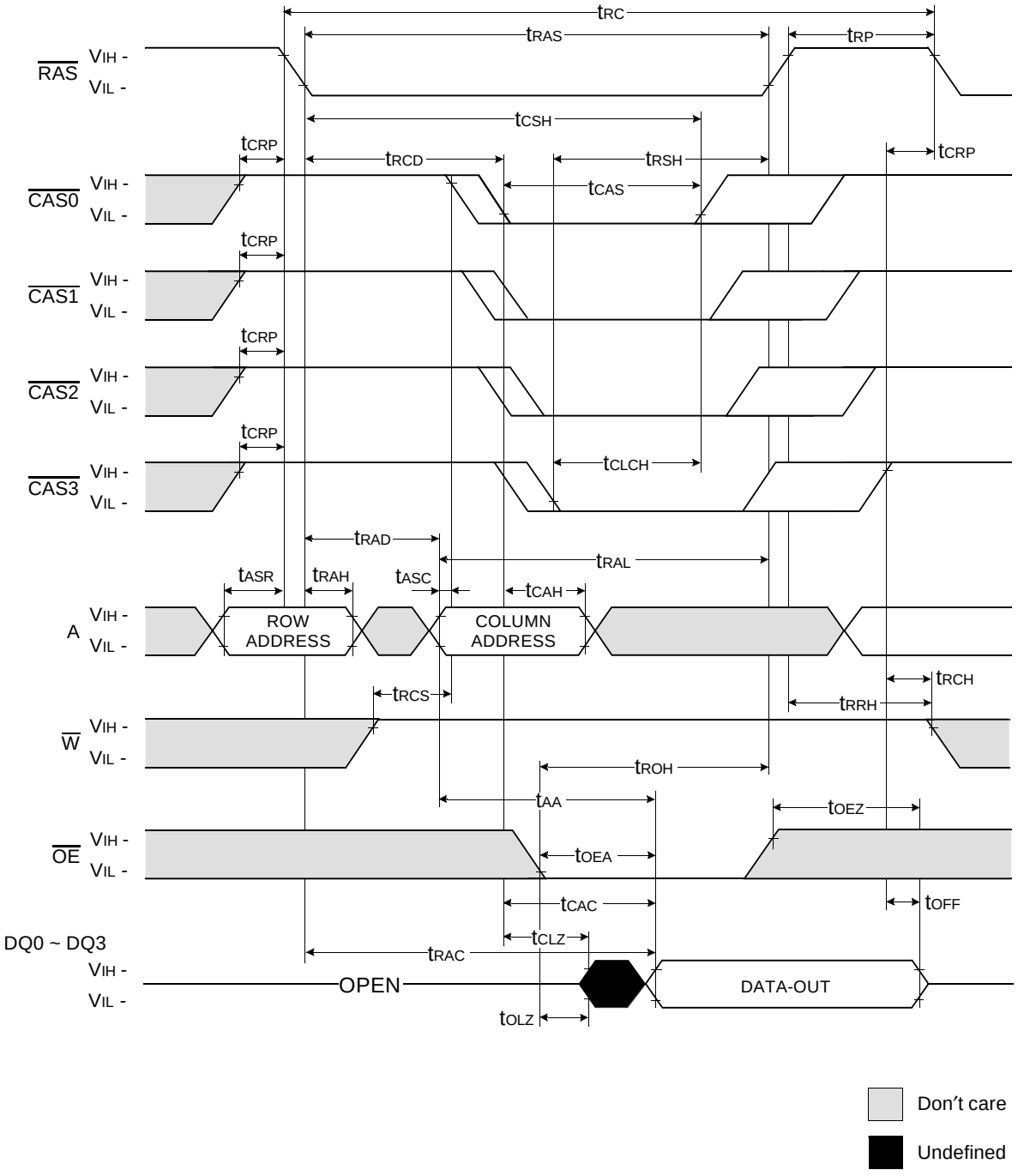
Parameter	Symbol	-5		-6		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		ns	
Read-modify-write cycle time	t_{RWC}	138		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65	ns	3,4,10,12
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,12
Access time from column address	t_{AA}		30		35	ns	3,10,12
$\overline{RAS}$ pulse width	t_{RAS}	55	10K	65	10K	ns	
$\overline{CAS}$ pulse width	t_{CAS}	18	10K	20	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	55		65		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	41		45		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	78		90		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	53		60		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	58		65		ns	7
Fast Page mode cycle time	t_{PC}	40		45		ns	
Fast Page read-modify-write cycle time	t_{PRWC}	81		90		ns	
$\overline{RAS}$ pulse width (Fast Page cycle)	t_{RASP}	55	200K	65	200K	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3
$\overline{OE}$ access time	t_{OEA}		18		20	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	
$\overline{OE}$ command hold time	t_{OEH}	18		20		ns	

NOTES

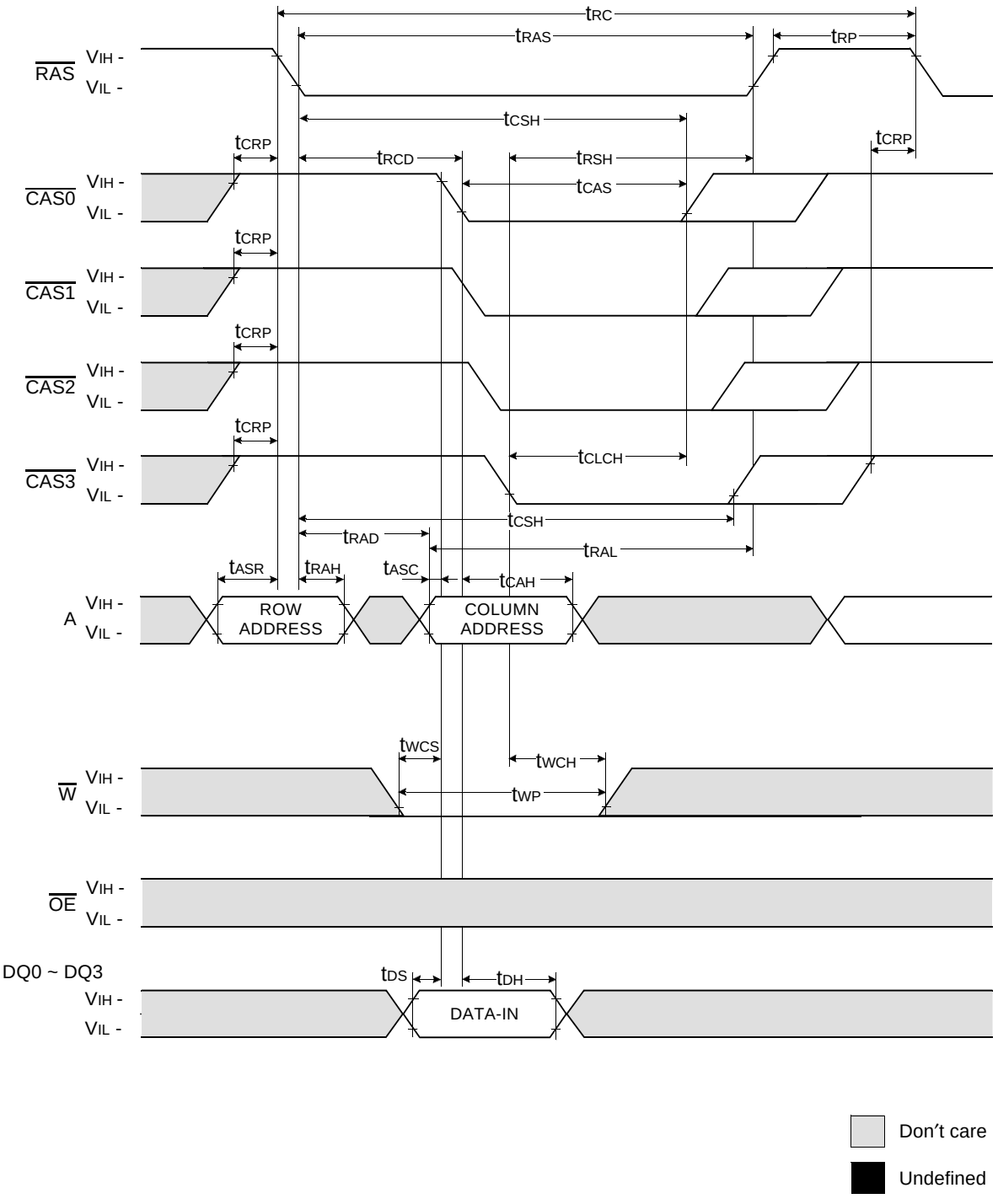
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.
   Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only.
   If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. t_{RCH} and t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the first $\overline{CAS}$ falling edge in early write cycles and to $\overline{W}$ falling edge in $\overline{OE}$ controlled write cycle and read-modify-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only.
    If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the values of t_{RAC}, t_{AA} and t_{CAC} are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
13. In order to hold the address latched by the first $\overline{CAS}$ going low, the parameter t_{CLCH} must be met.
14. The last $\overline{CAS}$x edge to go low.
15. The last $\overline{CAS}$x edge to go high.
16. The first $\overline{CAS}$x edge to go low.
17. The first $\overline{CAS}$x edge to go high.
18. Output parameter is refrenced to corresponding $\overline{CAS}$x input.
19. The last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
20. The last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
21. The first DQx controlled by the first $\overline{CAS}$x to go low.
22. The last DQx controlled by the last $\overline{CAS}$x to go high.
23. Each $\overline{CAS}$x must meet minimum pulse width.
24. The last falling $\overline{CAS}$x edge to the first rising $\overline{CAS}$x edge.
25. If $t_{RASS} \geq 100$us, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.
26. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(4K)/2048(2K) cycles of burst refresh must be executed within 64ms/32ms before and after self refresh, in order to meet refresh specification.
27. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval, $\overline{CAS}$-before-$\overline{RAS}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

READ CYCLE

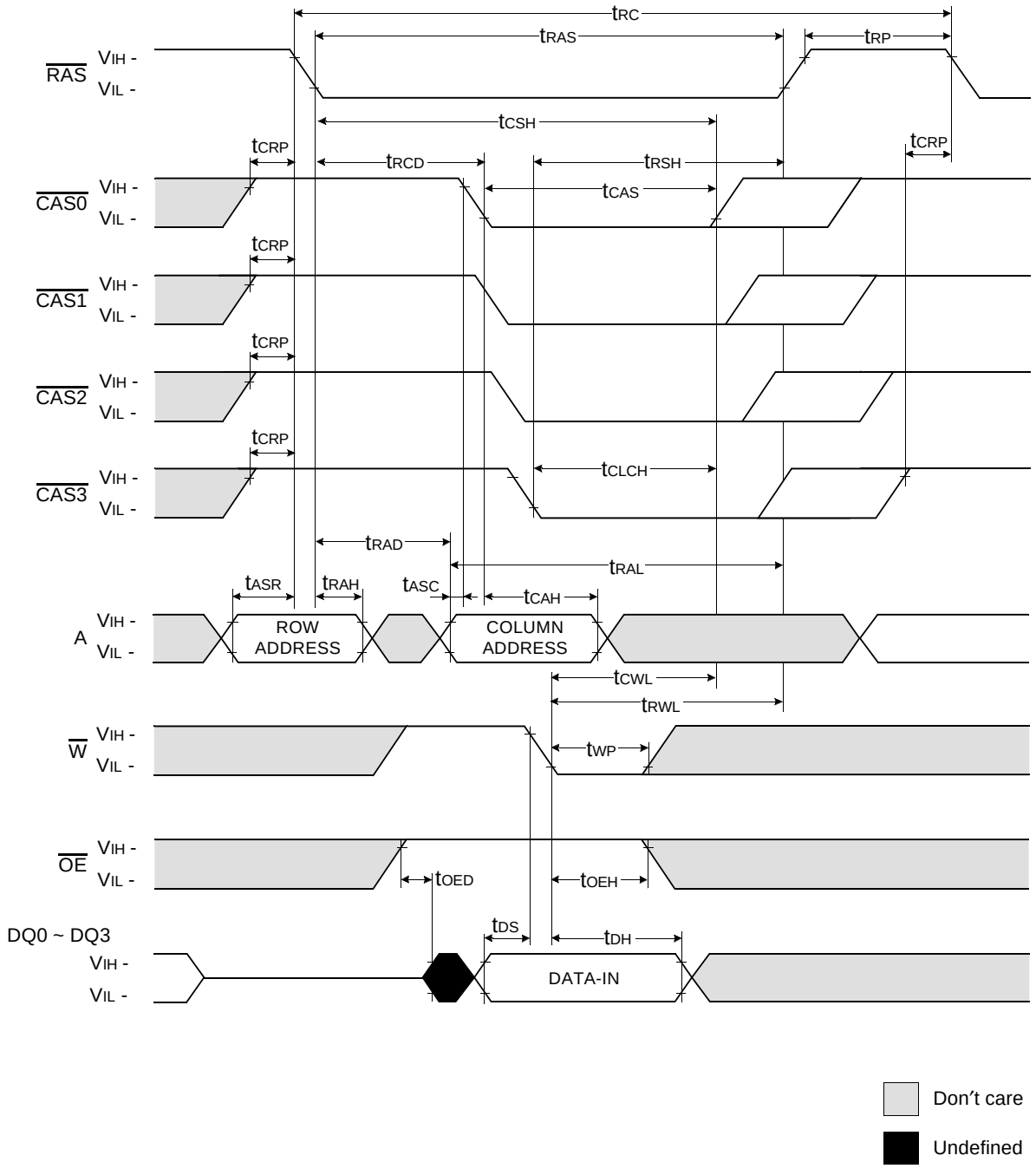
NOTE : D_{OUT} = OPEN



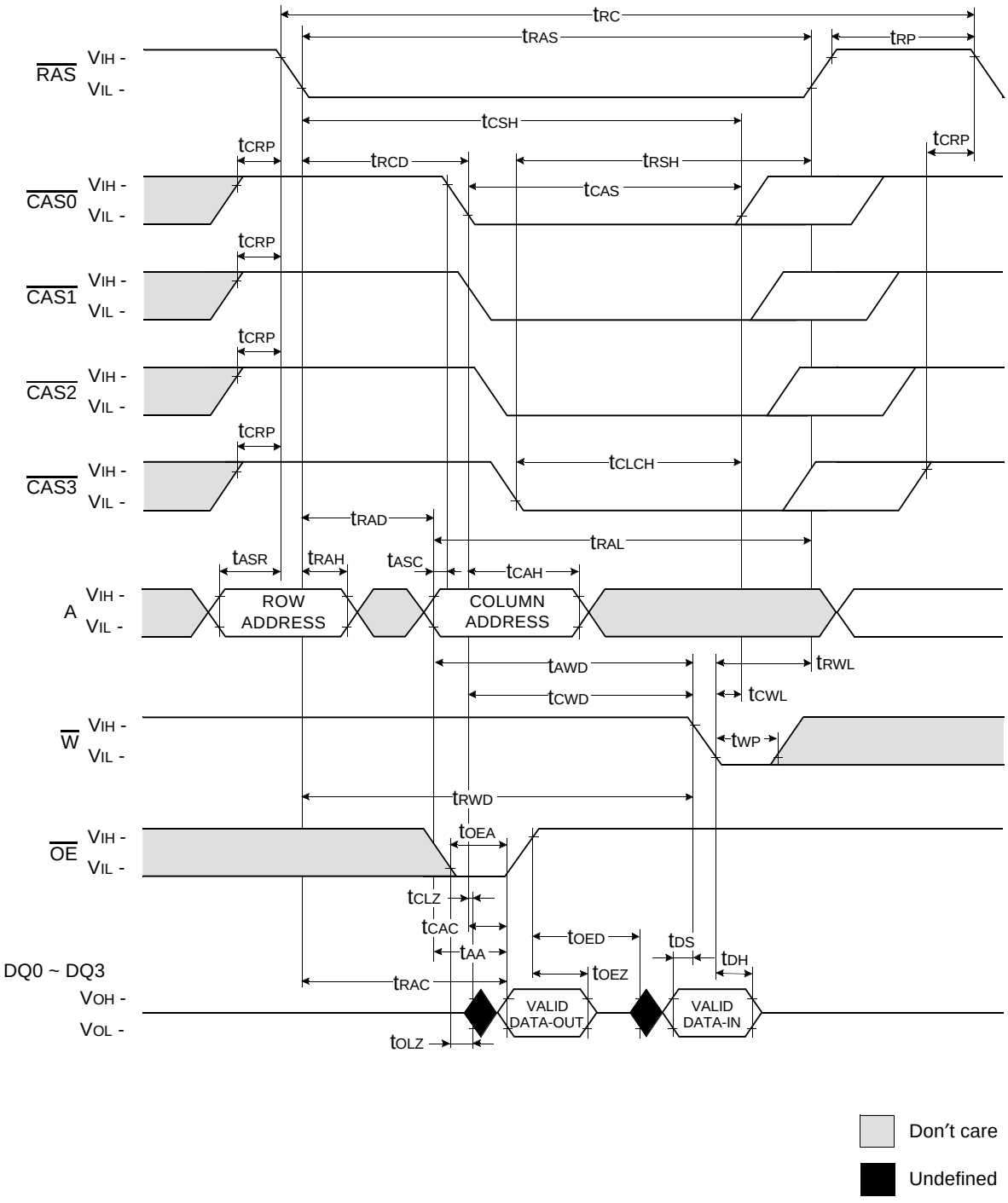
WRITE CYCLE (EARLY WRITE)



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

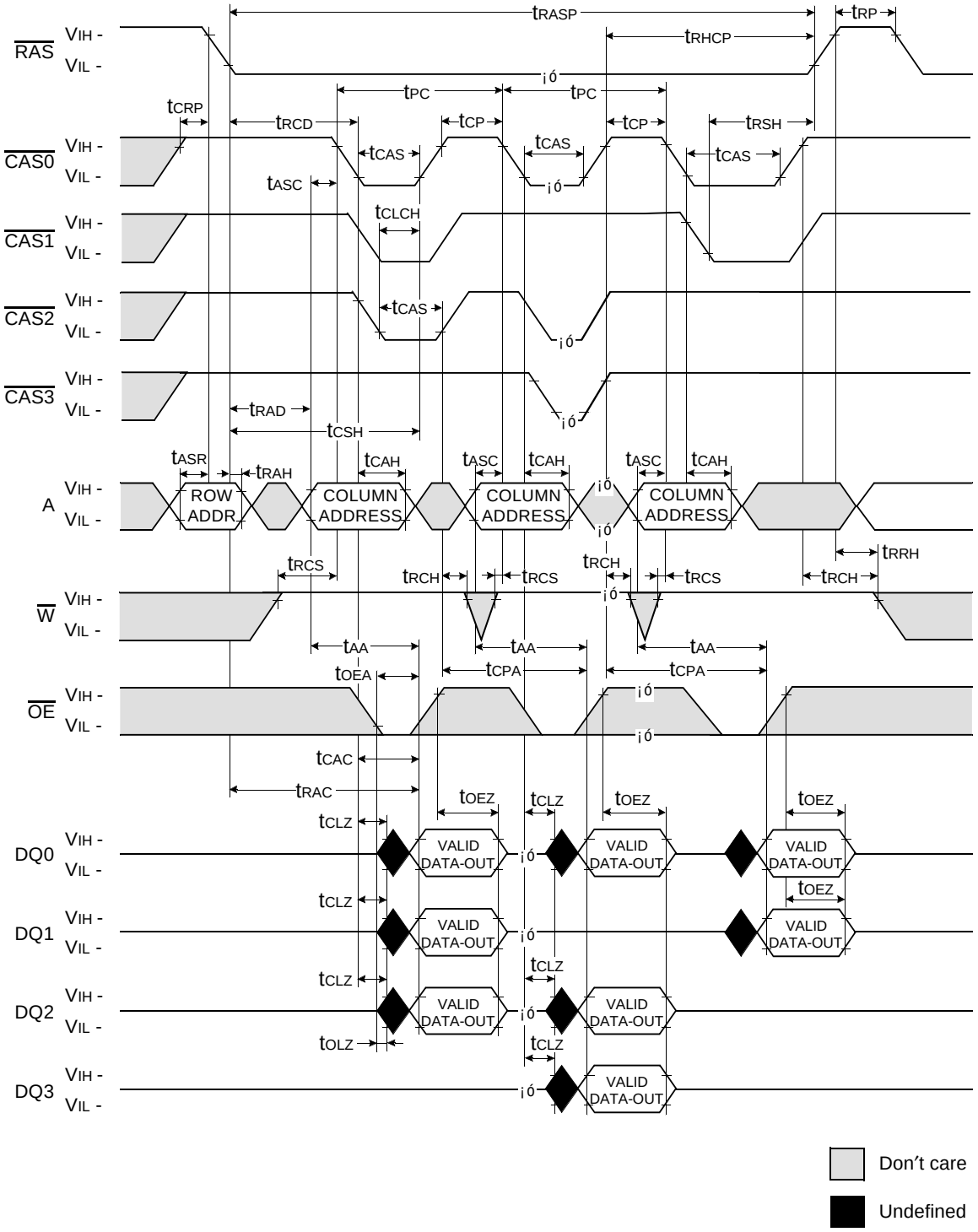


READ - MODIFY - WRTIE CYCLE

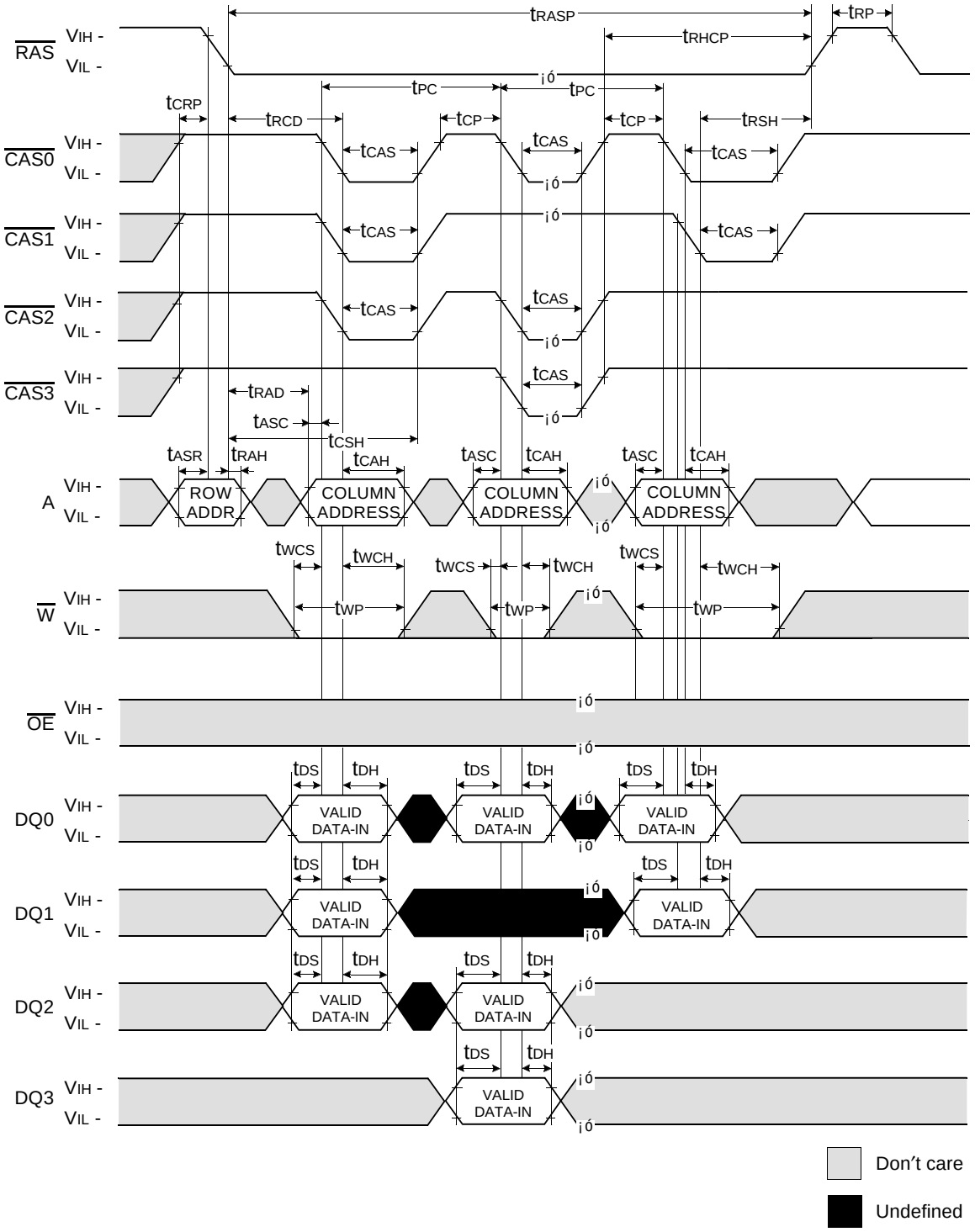


FAST PAGE READ CYCLE

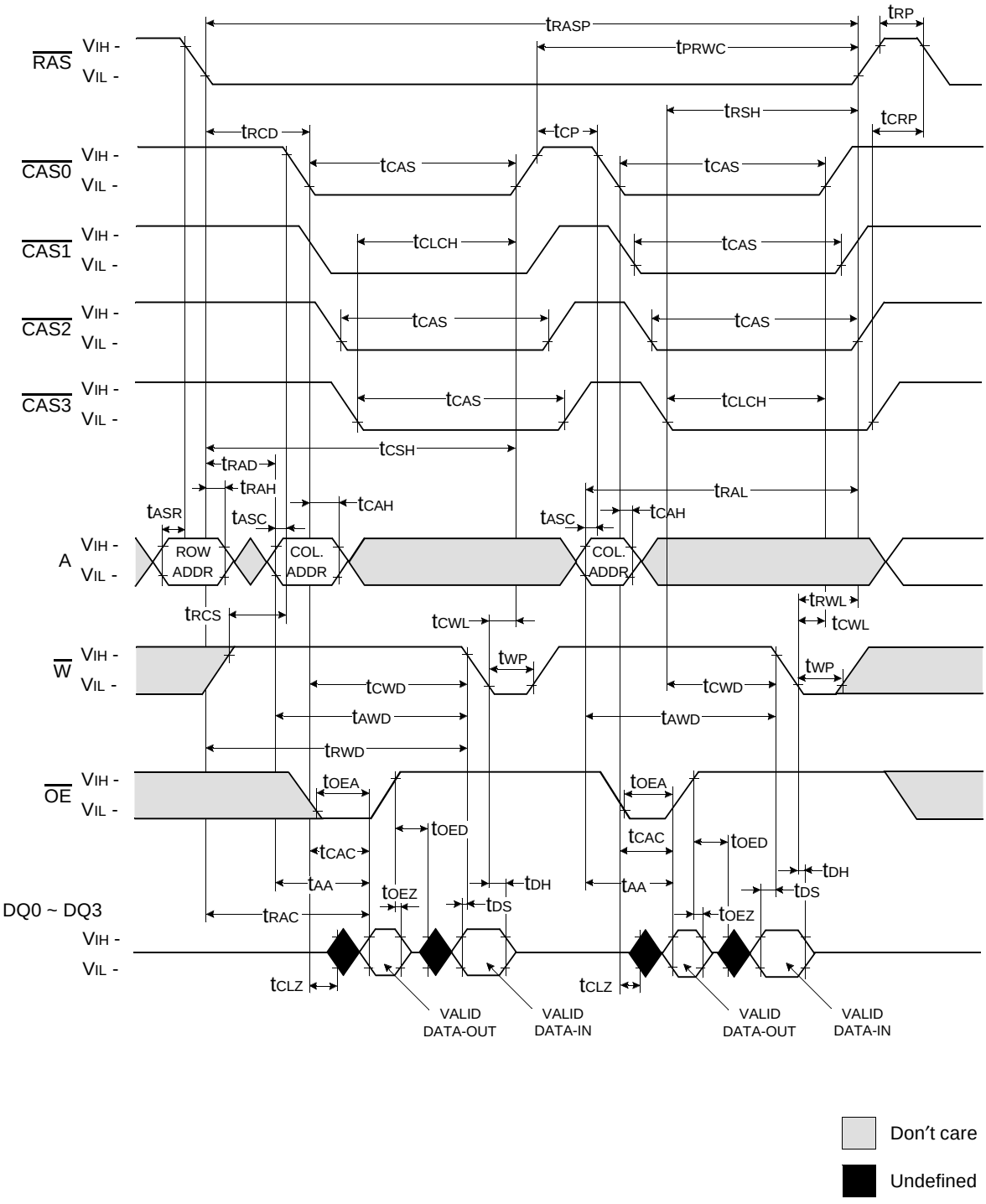
NOTE : DOUT = OPEN



FAST PAGE WRITE CYCLE (EARLY WRITE)



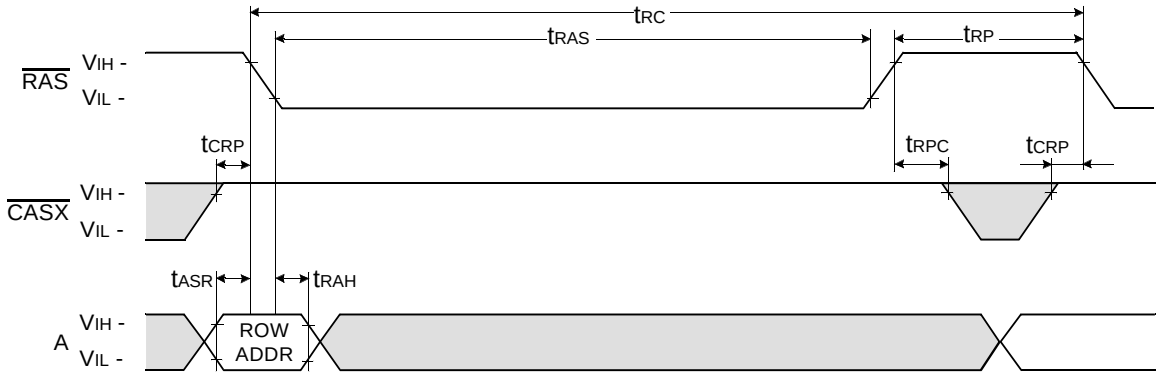
FAST PAGE READ - MODIFY - WRITE CYCLE



$\overline{RAS}$ - ONLY REFRESH CYCLE

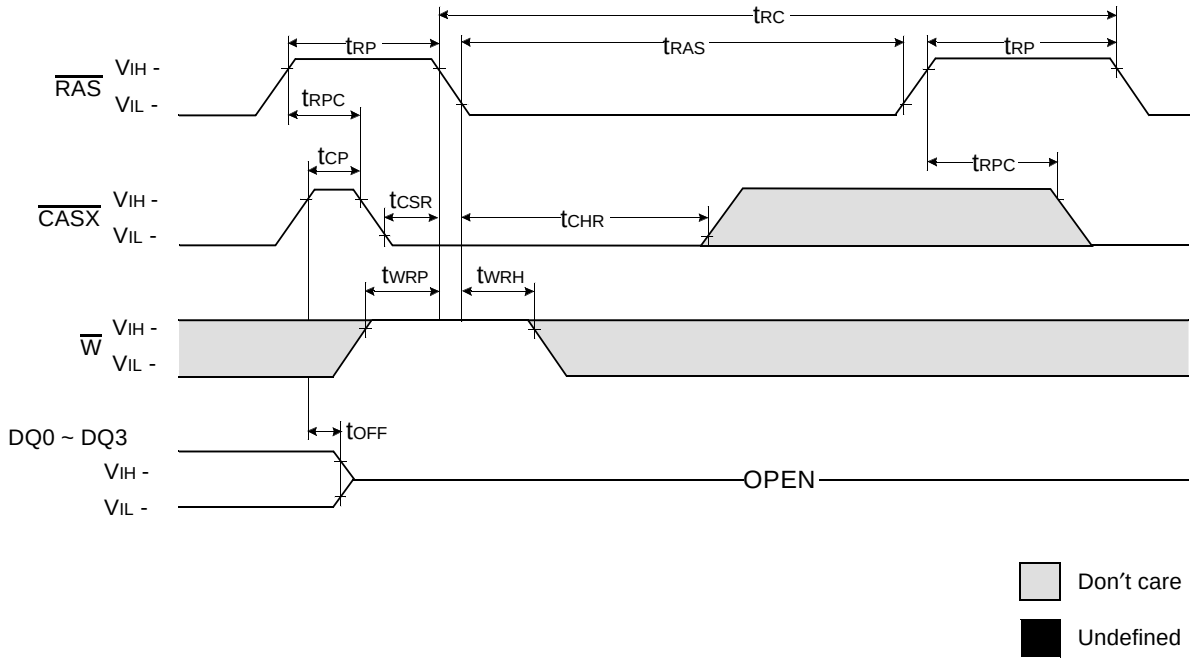
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN

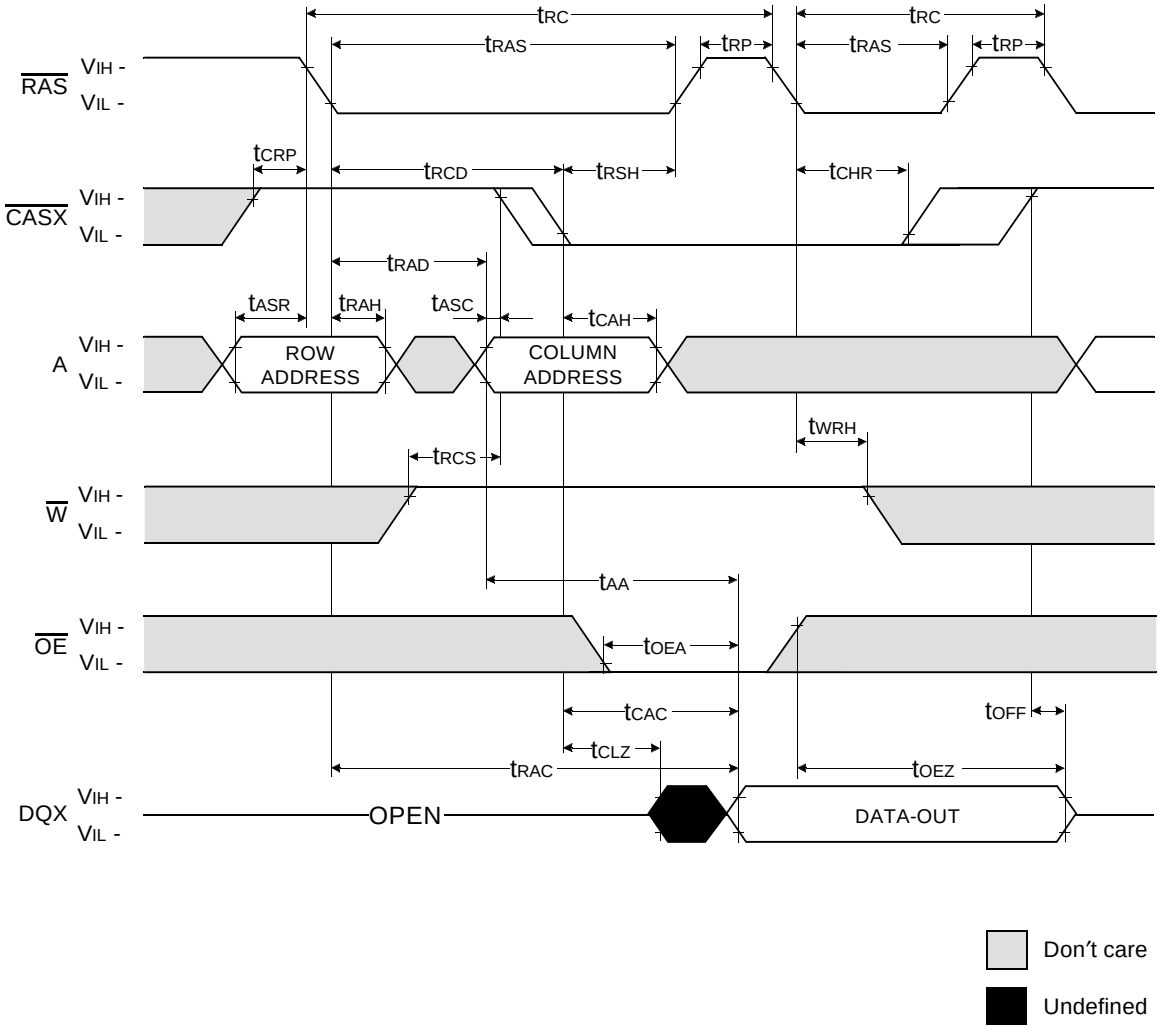


$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care

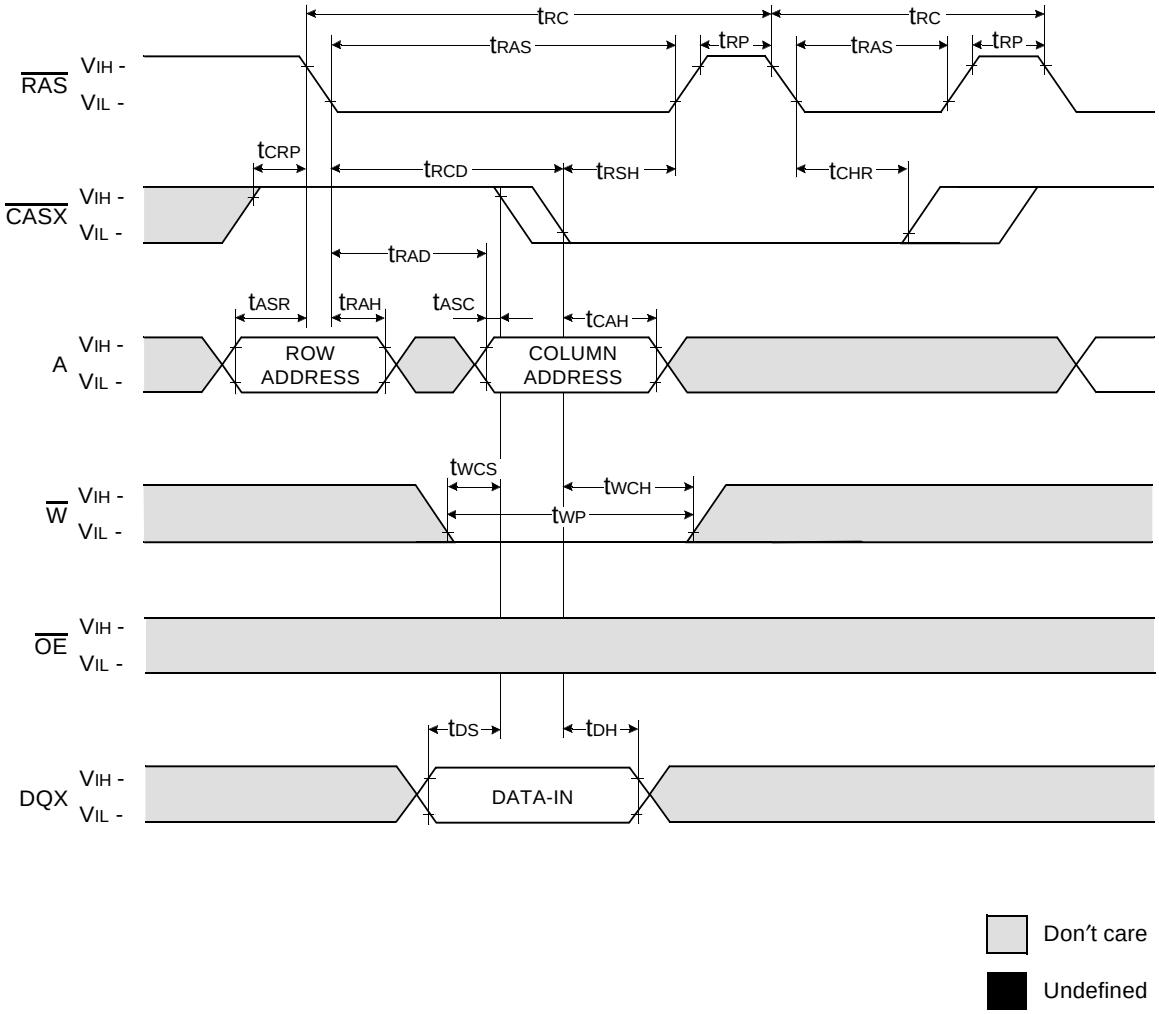


HIDDEN REFRESH CYCLE (READ)



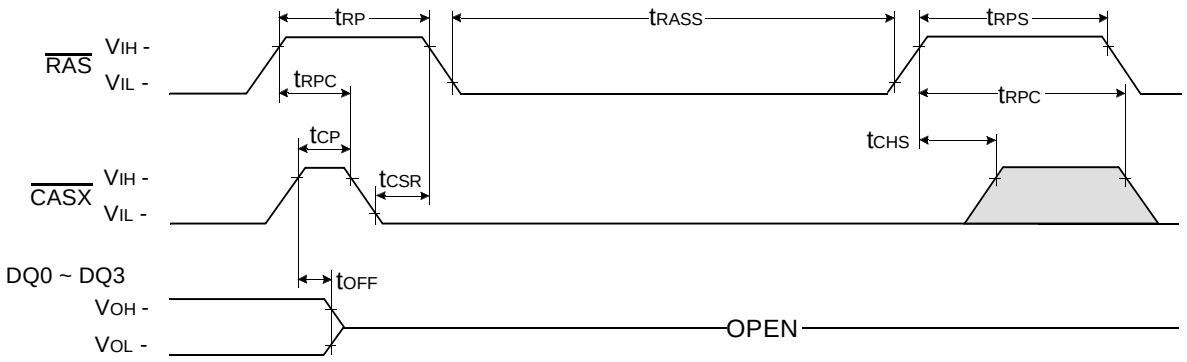
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



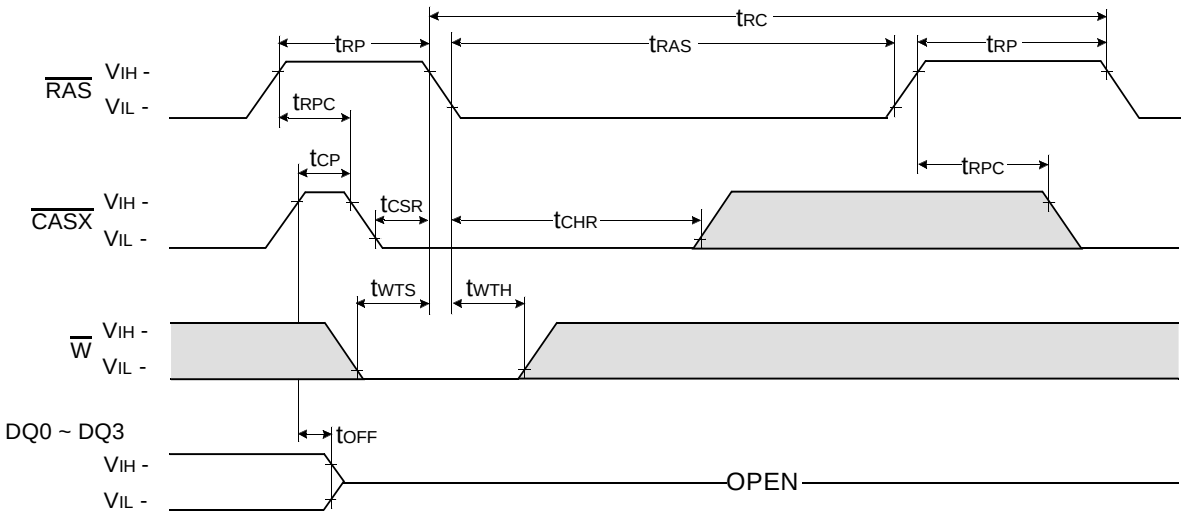
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care



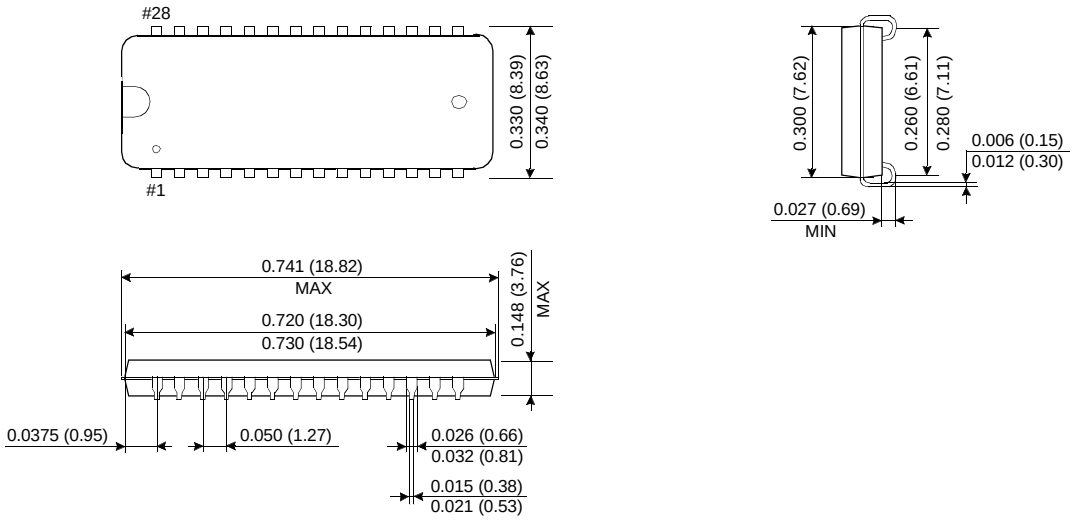
Don't care

Undefined

PACKAGE DIMENSION

28 SOJ 300mil

Units : Inches (millimeters)



28 TSOP(II) 300mil

Units : Inches (millimeters)