2

MC6173

MOS
(N-CHANNEL, SILICON-GATE)

2400 bps
DEMODULATOR

2400 bps DIGITAL DEMODULATOR

The MC6173 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.
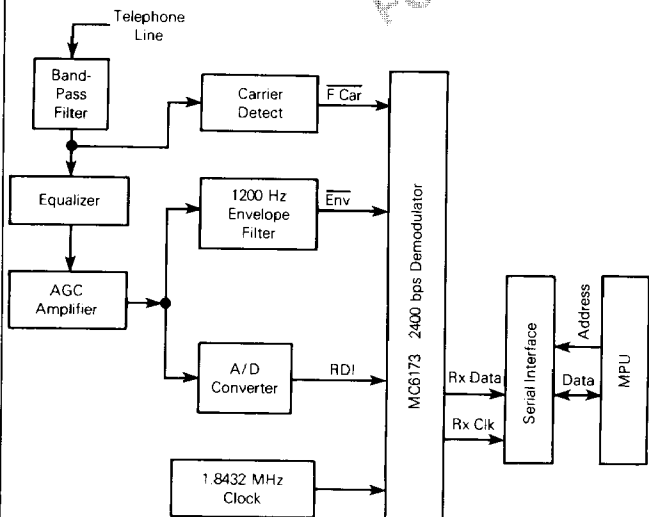
The demodulator provides the necessary demodulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6173 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data communication terminals, and I/O interfaces for counters.

N-channel silicon gate technology permits the MC6173 to operate using a single voltage supply and be fully TTL compatible.

The demodulator is compatible with the M6800 microcomputer family, and provides medium-speed data communications capability.

- Compatible with MC6172 Modulator
- 511-Bit CCITT V.52 Test Pattern
- Terminal Interfaces Are TTL Compatible
- Compatible Functions for 201B/C and V.26 Data Sets
- CCITT and U.S. Phase Options
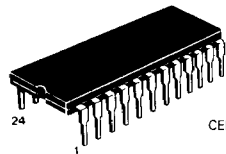- 1200/2400 bps Operation
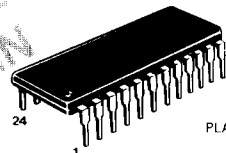

L SUFFIX
CERDIP PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 709

FIGURE 1 — TYPICAL APPLICATIONS

PIN ASSIGNMENT

V_{SS}	1	24	DRS
$\overline{FCar}$	2	23	RDI
$\overline{DCD}$	3	22	TStr
90° Eye	4	21	DBC
0° Eye	5	20	Rx Clk
ADC	6	19	CCor
0° Car	7	18	$\overline{TPE}$
ADS	8	17	PSS
Rx Data	9	16	$\overline{TEn}$
$\overline{Env}$	10	15	$\overline{CarS}$
$\overline{NSync}$	11	14	Clk
V_{CC}	12	13	TClk
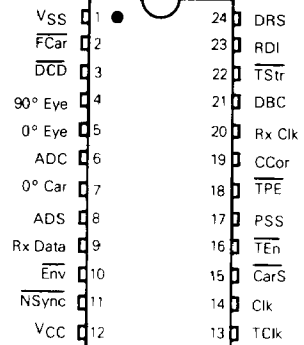
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to $+7.0$	V
Input Voltage	V_{in}	-0.3 to $+7.0$	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-55 to $+150$	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{SS}).

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DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0 \pm 0.25$ Vdc, $V_{SS}=0$, $T_A = T_L$ to T_H all outputs loaded as shown in Figure 3 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	$V_{SS}+2.0$	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	$V_{SS}+0.8$	V
Input Current ($V_{in}=V_{IL}$) Pins 3, 11, 13, 15, 16, 17, 18, 22, 24	I_{IL}	—	—	-0.2	mA
Input Leakage Current ($V_{in}=5.25$ Vdc, $V_{CC}=V_{SS}$) Pins 2, 10, 14, 23	I_{in}	—	—	2.5	μA
Output High Voltage ($I_{OH}=-0.04$ mA, Load A) ($I_{OH}=0.0$ mA, Load B)	V_{OH1} V_{OH2}	$V_{SS}+2.4$ $V_{CC}-0.5$ V	— —	V_{CC} V_{CC}	V
Output Low Voltage ($I_{OL}=1.6$ mA, Load A)	V_{OL}	V_{SS}	—	$V_{SS}+0.4$	V
Input Capacitance ($f=0.1$ MHz, $T_A=25$°C)	C_{in}	—	5.0	—	pF
Internal Power Dissipation (measured at $T_A=T_L$) (All Inputs at V_{SS} except Pin 13 = 57.6 kHz and ALL Outputs Open)	P_{Int}	—	—	630	mW
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r t_f	— —	— —	40 40	ns
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% Points)	t_r, t_f	—	—	1.0*	μs
Output Transition Times (From 10% to 90% Points)	t_r, t_f	—	—	5.0	μs
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	—	70	%
Data Setup Time	t_{DS}	770	—	—	ns
Rx Data Setup Time	t_{su}	35	—	—	μs
Data Hold Time	$t_{h(D)}$	0	—	—	ns
Rx Data Hold Time	t_h	35	—	—	μs
Data-Clamp Delay Time Option 1 Option 2 Option 3 Option 4	t_{DCD1} t_{DCD2} t_{DCD3} t_{DCD4}	5.7 4.135 20.795 104.135	6 4.17 20.83 104.17	6.3 4.205 20.865 104.205	ns ms ms ms
A/D Clock to A/D Strobe Delay Time	t_{ADCD}	1.06	—	1.11	μs
Envelope-to-Dibit Clock Delay Time	t_{ED}	140	—	220	μs
Clock Frequency, $\pm 0.005\%$	f_{Clk}	—	1.8432	—	MHz
A/D Clock Cycle Time ($f_{Clk}/4$)	t_{cyc}	—	2.17	—	μs
A/D Clock Pulse Width	$t_{w(ADC)}$	940	1000	1040	ns
A/D Strobe Pulse Width	$t_{w(ADS)}$	—	10.85	—	ns
New Sync Input Pulse Width	t_w (NSync)	0.84	—	—	ms

*Maximum input transition times are ≤ 0.1X pulse width or the specified maximum of 1.0 μs, whichever is smaller.

MOTOROLA TELECOMMUNICATIONS DEVICE DATA
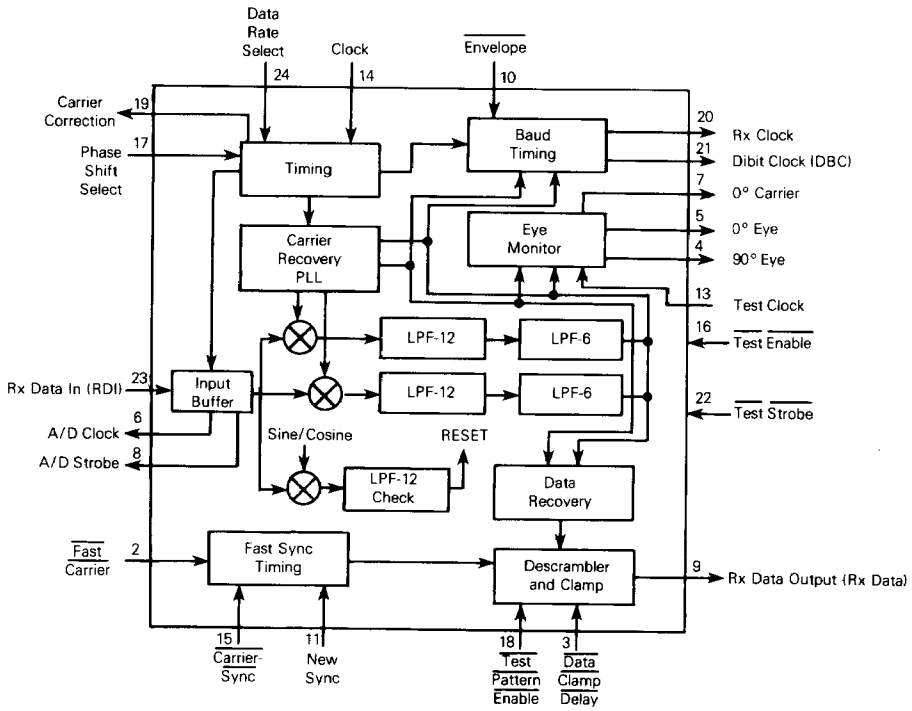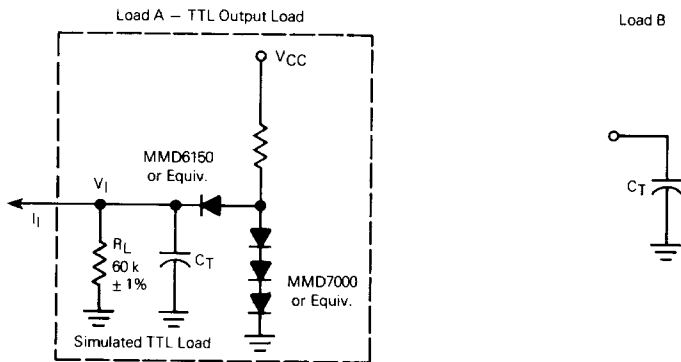
FIGURE 2 — DEMODULATOR BLOCK DIAGRAM

FIGURE 3 — OUTPUT TEST LOADS

C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances

GENERAL DESCRIPTION

The MC6173 Phase-Shift Key (PSK) Demodulator serves as an integral part of a system to recover synchronous data from an 1800 Hz PSK modulated carrier. Data rates of 1200 and 2400 bits-per-second are available. In the case of 1200 bps operation, the MC6173 detects phase shifts of 0 to 180 degrees to represent digital "0s" and "1s". When 2400 bps operations is desired, the MC6173 detects phase shifts of 0, 90, 180, and 270 (option A) or 45, 135, 225, and 315 (option B) degrees to represent two bits of data called dibits. These phase shifts decode to 00, 01, 10, and 11, respectively. In either data rate, the 1800 Hz carrier is modulated at a 1200 rate.

Figure 1 shows the MC6173 demodulator in a typical application. The band-pass filter, equalizer, analog-to-digital (A/D) converter, 1200 Hz envelope filter, AGC amplifier, and 1800 Hz carrier detector are external to the MC6173. The band-pass filter passes roughly 300 Hz to 3000 Hz eliminating noise, 60 Hz and 120 Hz pickup, and harmonics of 1800 Hz. The output of this filter is fed to the equalizer which adjusts phase versus amplitude such that a constant amplitude is maintained regardless of phase and is fed into the carrier detect circuit. The AGC amplifier provides a constant level signal regardless of the input level from the equalizer. The output of the AGC amplifier drives two basic sections of external circuitry, i.e., the A/D converter, and 1200 Hz envelope filter.

The A/D converter samples each 1200 Hz cycle or dibit 12 times. After each sample, digital data is clocked serially to the MC6173 receiver data input (RDI). The MC6173 generates the sampling clock for AD Strobe (ADS) and the serial clock (ADC) from the 1.8432 MHz internal oscillator.

The 1200 Hz envelope filter recovers the 1200 Hz component of the equalizer output during fast training and generates a 1200 Hz square wave. This square wave is connected to the envelope (Env) input and is used for internal timing.

The carrier detect circuit is used to signal the fast carrier (FCar) input that a carrier is present. Immediately after FCar has received a negative transition, the internal phase-lock loop temporarily widens its band width so that it can quickly adjust the internal timing of the MC6173 with respect to the 1200 Hz Env input (this is called fast Sync or fast training). The timing adjustments are made so that each dibit can be sampled at the most advantageous places.

The internal circuitry digests the dibit samples and produces the digital data (Rx Data) along with the receive data clock (Rx Clk). These two signals are used to drive a serial-to-parallel interface such as an MC6852 Synchronous Serial Interface Adapter.

PIN DESCRIPTION

FAST CARRIER (FCar), Pin 2 — A negative transition on this input will force a period of approximately 8.3 ms of fast training for both baud and carrier timing.* Fast Sync or fast

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*The postive transition of the 1200 Hz signal, present at the Env input, provides a divide-by-20 counter with every other clock. This will cause approximately 8.3 ms of fast training to the incoming signal at the demodulator.

training allows for large corrections to be made in the internal timing of the demodulator. After the fast training period, the timing should be reasonably well adjusted. Small adjustments are made automatically to maintain proper phase relationships internally after the fast-train period.

The FCar input, which normally comes from the carrier threshold detect circuits, must remain at a low level during the entire period of baud and carrier synchronization.

A positive level on the FCar input will disable the baud and carrier correction circuitry. Baud and carrier timing are then direct derivatives of the 1.8432 MHz clock as illustrated in Figure 4.

The first positive edge of the envelope (Env) input will be totally asynchronous to the demodulator. This will be ± ½ cycle of the 2400 clock (±208 μs). The nine following positive edges will introduce added tolerance equal to nine times the offset of Env from the absolute 1200 Hz (as defined by the 1.8432 MHz ±0.005% clock). Thus . . .

$$\text{Max Fast Train Time} = 4.17 \text{ ms} + 9/f_{Env} + 0.21 \text{ ms}$$
$$= 4.38 \text{ ms} + 9/f_{Env}$$
$$\text{Min Fast Train Time} = 4.17 \text{ ms} - 0.21 \text{ ms} + 9/f_{Env}$$
$$= 3.96 \text{ ms} + 9/f_{Env}$$

DATA-CLAMP DELAY (DCD), Pin 3 — Data-clamp delay enables the selection of one of four delays during which Rx Data is held to a logic-high condition. This delay is measured from the negative edge of FCar. The four options are available at one pin through the use of the internal multiplexing in the demodulator. Options 3 and 4 are available by demultiplexing the dibit clock as demonstrated in Figure 5. The available delay options are listed in Table 1, these times will be approximate due to their direct relationship to the Env input during the first 8.3 ms. Also, these times are further dependent upon carrier offset. The delays given in Table 1 assume no carrier offset and that Env is synchronous with the Tx Clk. Figure 4 is illustrative of the timing and sequencing of this circuit.

A scheme for programming the data-clamp delay is illustrated in Figure 5. The DCD input may either be a constant high or low level which will produce options 1 and 2. If the input "A" is exclusive ORed with the dibit clock options 3 and 4 are produced at the same input pin.

ENVELOPE (Env), Pin 10 — The envelope input comes from the 1200 Hz envelope detection circuitry. Envelope detection will normally consist of a 1200 Hz filter and a voltage comparator to generate an approximate limited square wave. This is normally derived from a constant mark signal sent by the modulator for Sync acquisition purposes.

Each positive edge that is input to Env will reset both baud timing and the dibit clock to a logic "0". The optimum timing of the positive transition at the Env input will be t_{ED} prior to the falling edge of the dibit clock. Timing is illustrated in Figure 6.

Env will be effective in the training of baud timing and dibit clock only if FCar is in the active low state.

Minimum positive pulse width at the Env is ≥2.17 μs.

NEW-SYNC (NSync), Pin 11 — This input port is normally controlled by the business machine. If FCar is at an active low, then an active low pulse in excess of 0.84 ms on the NSync lead will put the demodulator into the fast-Sync

FIGURE 4 — DEMODULATOR SYNC TIMING DIAGRAM
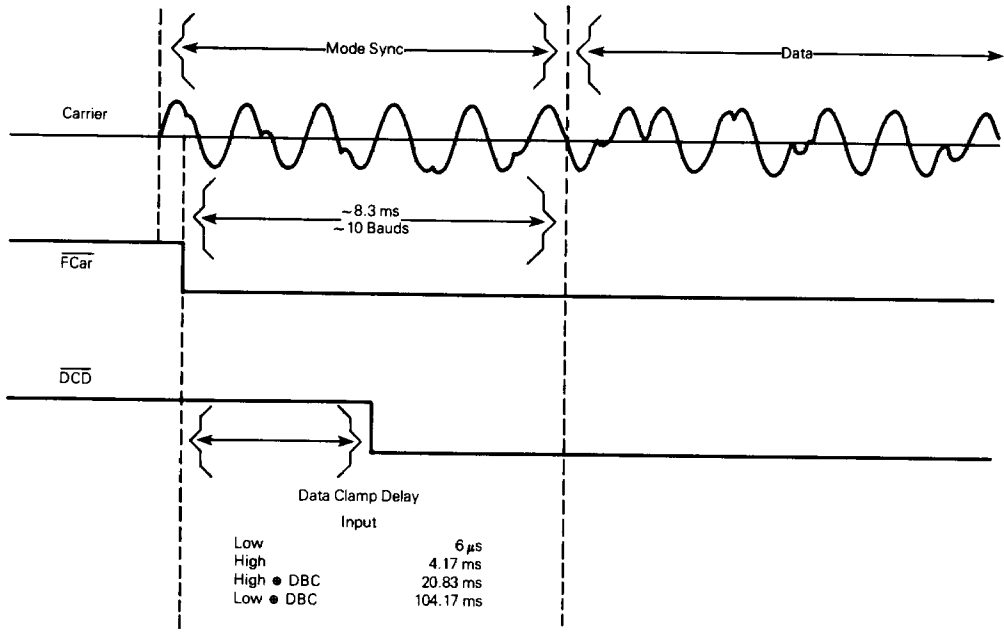
TABLE 1 — DATA-CLAMP DELAY OPTIONS

Option	A	C	$\overline{DCD}$	Data-Clamp Delay
1	1	0	0	6 μs
2	0	0	1	4.17 ms ± 35 μs
3	.1	DBC	DBC	20.83 ms ± 35 μs
4	0	DBC	$\overline{DBC}$	104.17 ms ± 35 μs

FIGURE 5 — DATA-CLAMP DELAY DEMULTIPLEXER
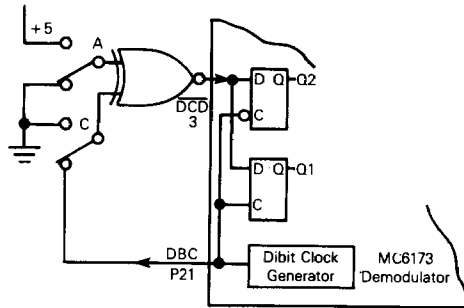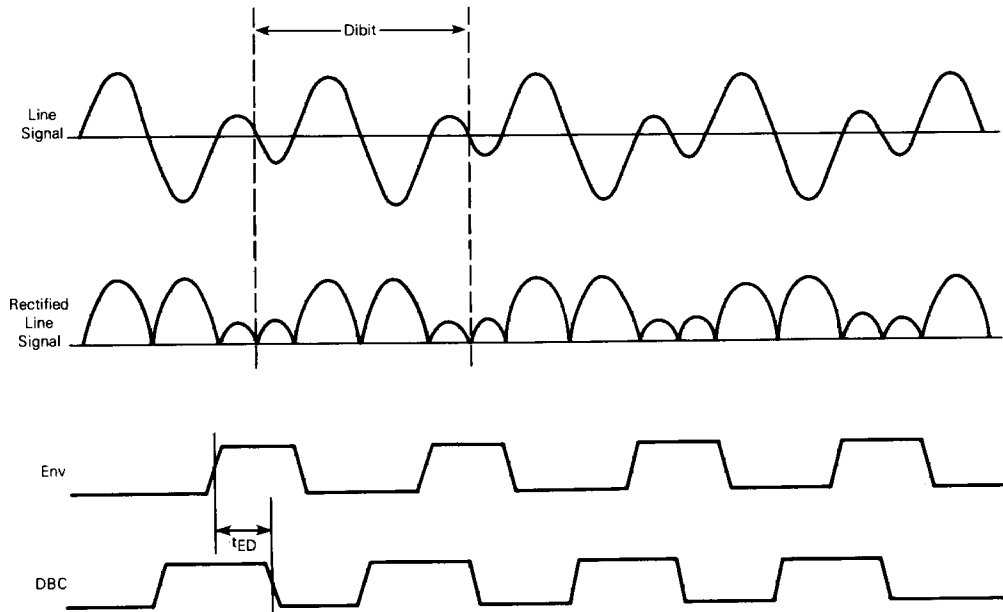
FIGURE 6 — ENVELOPE CLOCK TIMING DIAGRAM

or fast-train mode (these terms are synonymous).

Activation of NSync allows large corrections to be made to both baud and carrier timing similar to initial activation of the FCar lead. These corrections will be applied for approximately 8.3 ms. The receiver must complete the 8.3 ms period of fast Sync before another NSync is recognized.

CARRIER-SYNC (CarS), Pin 15 — When CarS is taken to an active low, baud timing will be taken from the Env input. In addition, the slow carrier correction will be doubled in the 2400 baud mode as defined by the data-rate select (DRS) and phase-shift select (PSS) inputs. (This is not the same as the fast training that is incorporated when FCar or NSync are active, which is a changing of the bandwidth of the internal phase-lock loop [PLL]). This widening of the PLL band width will allow a faster search and lock on the 1800 Hz carrier. This Carrier-Sync mode will remain active as long as CarS is held in the active state. The normal application of this option would be to extend the training or Sync time under the mark input data condition that exceeds 8.3 ms.

If FCar is at a logic "1" inactive state, this input is ignored by the demodulator.

A/D CLOCK (ADC), Pin 6 — This output will allow, in a serial format, the six A/D data bits plus sign information to be synchronously clocked into the demodulator. (See Figure 8.)

There are nine 1 μs positive pulses occuring at a 460 kHz rate. The first pulse, along with ADS, is used to begin the A/D conversion sequence. The next seven positive edges strobe data serially from the A/D converter to the demodulator input (RDI) enabling the demodulator to properly decode the A/D data.

This signal is also used to clock 0 and 90 degree eye data out of the demodulator. This is described in the Eye Pattern section. When TEn is low, ADC monitors check accumulator output (see TEn).

A/D STROBE (ADS), Pin 8 — A positive going, approximately 11 μs, pulse is used as an enable signal for a sample and hold circuit prior to the A/D converter. The negative edge of this pulse is used to start the conversion process. Pulse rate of this signal is 14.4 kHz which allows each dibit to be sampled 12 times. (See Figure 7.) When TEn is low, ADS monitors zero crossings (see TEn).

RECEIVER DATA INPUT (RDI), Pin 23 — The digital decode of the line signal magnitude, as sampled by the A/D, is input to the demodulator at this port. The data format is scaled binary. This sign bit occurs on the second A/D clock, followed by six magnitude bits which begin with the most-significant bit as shown in Figure 8. The data is strobed syn-

FIGURE 7 — ANALOG TO DIGITAL SAMPLE SCHEME
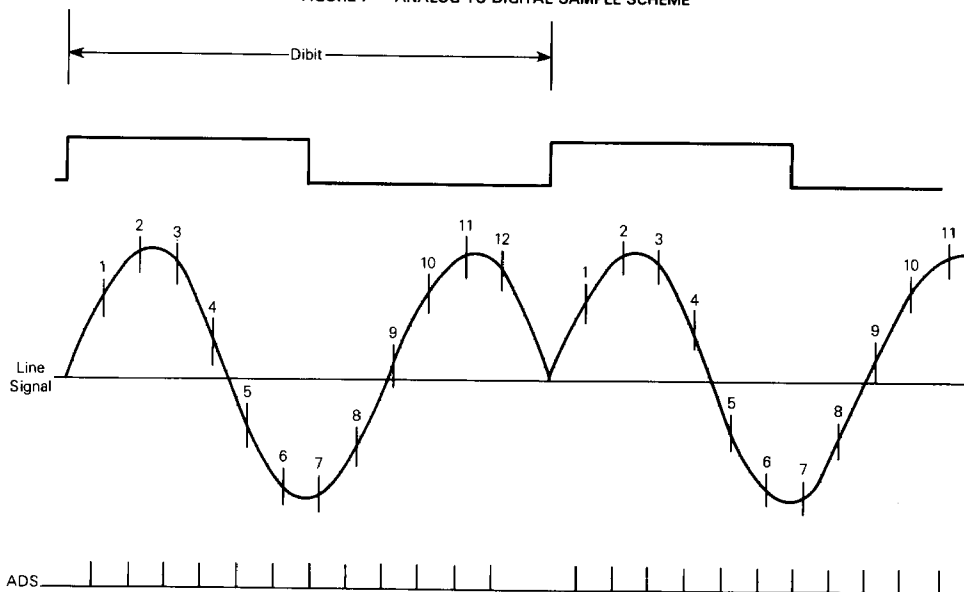
chronously with the positive edges of the ADC.

A logic one in the sign bit slot will represent a positive value. The magnitude of the six data bits increases from 000000 to 111111 with all ones always representing the most-positive value as illustrated below:

Sign	MSB					LSB	Value
1	1	1	1	1	1	1	+63
1	0	0	0	0	0	0	0
0	1	1	1	1	1	1	−0
0	0	0	0	0	0	0	−63

RECEIVE DATA OUTPUT (Rx Data), Pin 9 — This pin is the demodulator output for mark and space serial data. Data is synchronous with the receiver clock output with the positive going edge of the receiver clock occurring in the center of the data bit. A mark is represented by a logic high ("1") level except for the conditions described under PSS and TPE.

The Rx Data output is inhibited in a logic-high level when FCar is in the inactive high state. The delay from the positive edge of FCar to the inhibiting of data is 2 μs.

RECEIVE CLOCK (Rx Clk), Pin 20 — The receive clock output provides the 2400 Hz ±0.005% timing signal to the business machine for sampling the demodulated received

data marks and spaces (Rx Data). Receive clock is present at the demodulator chip output at all times; is not clamped to an inactive state when the carrier detected is not presented on FCar; nor is Rx Clk clamped by any other combination of inputs to the demodulator.

Timing corrections to the receive clock, that are generated internally, are made following FCar going active. As described in FCar, if CarS is held active the receive clock is continuously updated from dibit Sync.

The positive transition of the Receive Clock, which occurs in the middle of the data bit, should be used to strobe data from the demodulator, under normal operating conditions. When TPE scrambler/descrambler is being incorporated, then the negative edge of the Rx Clk will occur in the center of the data bit.

Receive Clock will be 2400 bps or 1200 bps depending on the logic input at the DRS input. The Rx Clk edges described above apply to either 2400 bps or 1200 bps data rates.

Under TPE active, the Dibit relation to Rx Clk does not change. See Figure 9 for relative timing of Rx Clk, DBC and Rx Data.

Figure 10 depicts the requirements at the demodulator if the data scrambler is being incorporated. The exclusive Nor gating of TPE and Rx Clk would then maintain proper phasing of Rx Clk as it goes to the RS-232 driver. This circuit would be required since the positive edge of Receive Clock is a Data Communications Standard.

FIGURE 8 — ANALOG-TO-DIGITAL TIMING DIAGRAM
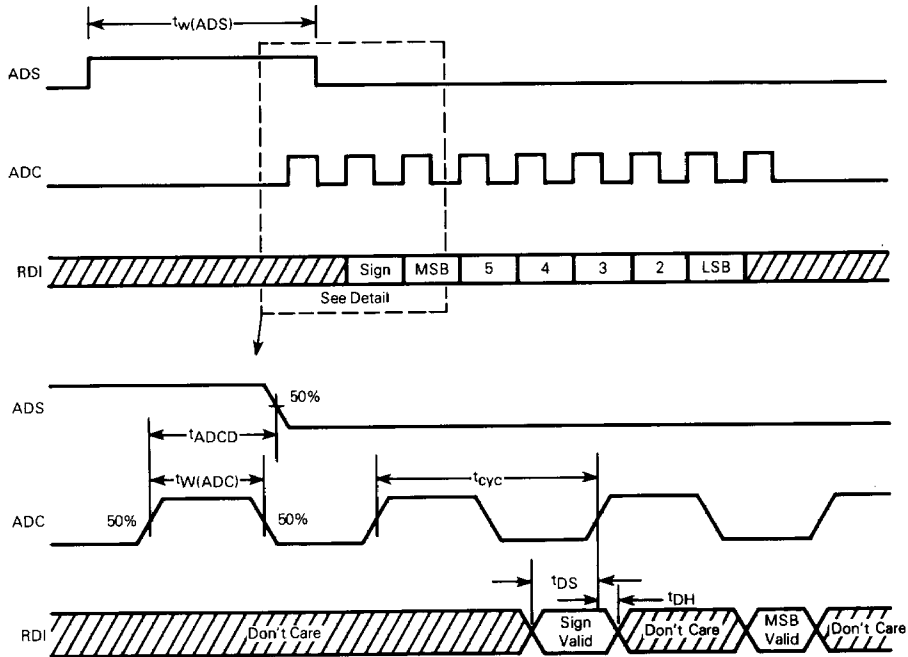
DATA RATE SELECT (DRS), Pin 24 — The following levels are valid for either phase-shift select:
 Logic high equals 2400 bps,
 Logic low equals 1200 bps.

PHASE-SHIFT SELECT (PSS), Pin 17 — Option A (CCITT) or option B (U.S.) phase shift can be selected for 2400 bps operation. The input data format and phase shift relationship for these two options are as follows:

Data	PSS = 0 Option A (Degrees)	PSS = 1 Option B (Degrees)
00	0	+ 45
01	+ 90	+ 135
11	+ 180	+ 225
10	+ 270	+ 315

For 1200 bps operation, option A (CCITT) or option B (U.S.) phase shift can be selected as follows:

Data	PSS = 0 Option A (Degrees)	PSS = 1 Option B (Degrees)
0	+ 90	+ 45
1	+ 270	+ 225

The phase shifts shown are the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next dibit.

If the logic level inputs to PSS are EXORed with DBC (dibit clock) or $\overline{DBC}$, then the test-pattern enable option may be selected and produce the compliment of normal data at Rx Data as explained in the $\overline{TPE}$ description. (See Figure 11.)

TEST-PATTERN ENABLE ($\overline{TPE}$), Pin 18 — Incorporated in the demodulator is the 511-bit test pattern shift register that is in accord with CCITT specification V52. This is the pattern that is generated by feedback from the 5th and 9th stages of a 9-bit shift register.

When the $\overline{TPE}$ input is allowed to be pulled up internally, there is normal data flow through the receiver. When the $\overline{TPE}$ input is pulled low, the incoming data is passed through this self-synchronous decoder which will produce the inverse of the 511-bit CCITT V52 pattern.

$\overline{TPE}$ works in coordination with PSS. If PSS is directly pulled high or low to represent option A or option B, then the presence of the 511-test pattern at the (RDI) input and $\overline{TPE}$ active will result in logic "1" condition at Rx Data output. If the DBC option is being utilized at the PSS input and $\overline{TPE}$ is active while the 511-bit test pattern is being received, the receiver data output will equal a logic "0". These options (Figure 11) are summarized in Table 2.

This assumes the modulator is sending the 511-bit test pattern with Rx Data being either a constant mark (logic "1") or space (logic "0"). If a logic "0" is received in options 1 or 2 or a logic "1" is received in options 3 or 4, then a transmission error has occurred. The number of errors-per-unit time is a measure of the transmission line quality.

A feature of the above type of pattern detector is that it will be self-synchronizing. It should be pointed out that there will be at least two error counts each time an error is detected.

If the $\overline{TPE}$ input is in the active state, it is important to note that the Rx Clk phase changes. The necessary circuit to regain proper phase is shown in Figure 10.

A scheme for programming the phase-shift select is illustrated in Figure 11. The PSS input may either be a constant high or low level which will produce options 1 and 2. If the input "A" is exclusive ORed with the dibit clock, options 3 and 4 are produced at the same input pin.

FIGURE 9 — CLOCK TIMING DIAGRAM

SETUP AND HOLD TIME
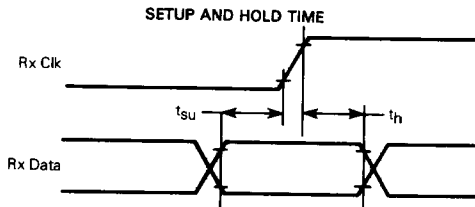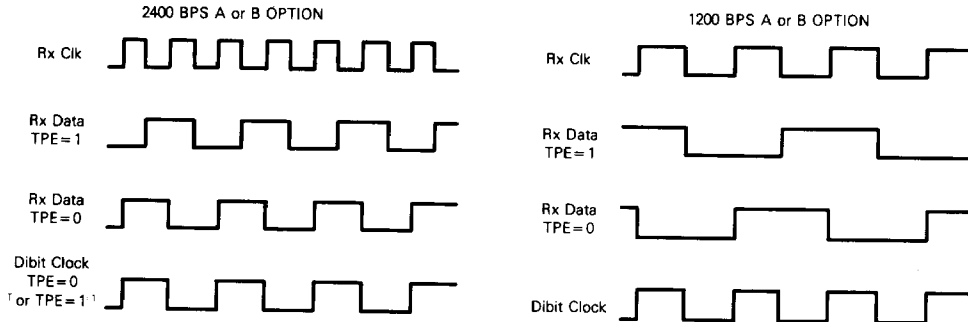
Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 10 — DEMODULATOR DATA SCRAMBLER RECEIVE CLOCK PHASE CORRECTION REQUIREMENTS
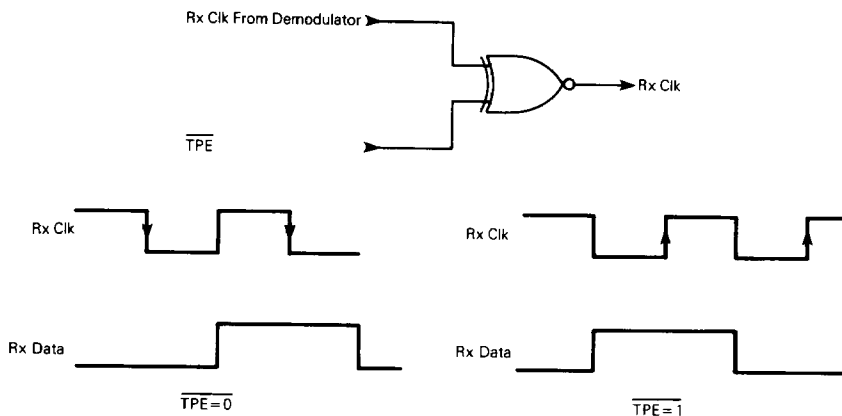
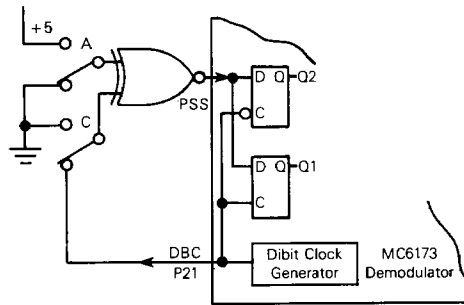FIGURE 11 — PHASE-SHIFT SELECT DEMULTIPLEXER
FOR TEST PATTERN ENABLE

TABLE 2 — TEST PATTERN ENABLE OPTIONS

Option	TPE	A	C	Phase Option	PSS	Output State
1	0	1	0	A	0	Rx Data Output = 1
2	0	0	0	B	1	Rx Data Output = 1
3	0	1	DBC	A	DBC	Rx Data Output = 0
4	0	0	DBC	B	$\overline{DBC}$	Rx Data Output = 0

CLOCK (Clk), Pin 14 — A 1.8432 MHz signal input ± 0.005% is required at this port. The clock requirements are the same as the modulator clock specifications. See Figure 12 for a suggested clock circuit.

The receive clock is generated by dividing down the 1.8432 MHz. Since receive clock accuracy must be at least ± 0.005%, the clock source must be of the same accuracy.

TEST-CLOCK (TClk), Pin 13 — This input is used for production testing of the demodulator device. In normal operation this pin should be left open which will enable the internal pullup resistor.

Pin 5	0 Degree Eye
Pin 4	90 Degree Eye
Pin 7	0 Degree Carrier
Pin 19	Carrier Correction

These test outputs are explained in the test enable ($\overline{TEN}$) description below.

TEST ENABLE ($\overline{TEn}$), Pin 16; 0° Eye, Pin 5; 90° Eye, Pin 4; 0° Car, Pin 7; CCor, Pin 19 — These pins allow the monitoring of ten internal points within the demodulator. A low level on $\overline{TEn}$ is normally associated with testing of the demodulator such as in a production test environment or incoming testing. Activation of $\overline{TEn}$ affects internal timing.

TABLE 3 — INTERNAL MONITORS

Output	$\overline{TEn}$	Function
ADS (Pin 8)	H	See Description Under ADS (Pin 8)
	L	Monitors Zero Crossings
ADC (Pin 6)	H	See Description Under ADC (Pin 6)
	L	Monitors Check Accumulator Output
0 Degree Eye (Pin 5)	H	Monitors 0 Degree Eye 2s Complement Information from 6 Tap Filter
	L	Monitors 0 Degree Eye 2s Complement Information from 12 Tap Filter
90 Degree Eye (Pin 4)	H	Monitors 90 Degree Eye 2s Complement Information from 12 Tap Filter
0°Car (Pin 7)	H	Monitors 0 Degree Carrier
	L	Monitors Check Accumulator Compare Errors
CCor (Pin 19)	H	Monitors Carrier Correction Enable
	L	Monitors Carrier Correction Direction

DIBIT CLOCK (DBC), Pin 21 — This output is a 1200 Hz clock which is derived from incoming data envelope and provides a dibit reference. This signal is representative of "data derived timing." When studying the quality of the demodulated signal, through the use of eye patterns, this output is necessary for proper synchronization of the oscilloscope.

TEST STROBE ($\overline{TStr}$), Pin 22 — This input is used to facilitate testing of the demodulator during the manufacturing process. It should be left unconnected which will result in

FIGURE 12 — OSCILLATOR CONFIGURATION

U1 = MC14069
Y1 = 1.8432 ± .005%
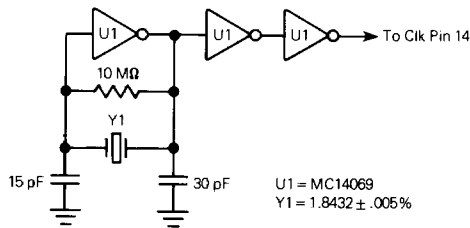
the internal pullup resistor causing the high level on this pin.

V_{SS} Pin 1 = The most negative supply, typically ground.
V_{CC} Pin 12 = The most positive supply, typically 5 volts.

DATA SCRAMBLER

The scrambling of data in the data communication environment is not done in an attempt to encrypt information in the normal sense of the word. Rather, the purpose of the scrambling of data is to guarantee that, with respect to the modem carrier, there is always random data on the line with little chance for a long string of "1s" or "0s" to exist. This is particularly important if an adaptive equalizer is being incorporated in the modem as the adaptive equalizer will require reasonably evenly distributed data to optimize its statistical response to the incoming signal. The normally used code is the CCITT 511 sequence which is EXORed with data.

The Motorola 2400 bps modulator contains a CCITT 511-bit test-pattern generator. It does not, however, incorporate the 511 data randomizer or scrambler. To scramble data using the MC6172 modulator, the circuit in Figure 10 must precede the Tx Data input of the modulator. Tx Data is added to the scrambler output pattern; then, the data is delayed by a full data bit before being transmitted by the modem. This assures a proper transmit-data/transmit-clock phase relationship. If the data scrambler is to be an optional feature, then the transmit-data multiplexer would also have to be built. This is selected by the test-pattern enable signal or any other signal that is found suitable.

The demodulator does contain a built-in data descrambler which is enabled by the $\overline{TPE}$ input going active. The receive phasing, with respect to data, changes when $\overline{TPE}$ goes active. The exclusive NOR gating of $\overline{TPE}$ and Rx Clk, as shown in Figure 10 will maintain proper phase of Rx Clk. This circuit is required since the clocking of data on a positive edge is a data communications standard.

EYE PATTERN

When performing an evaluation of an 2400 bps modem, one common point of comparison is the quality of the eye patterns produced by the demodulator. The eye pattern may also be used as an indicator of the incoming signal with respect to level and line perturbations. Eye patterns are for test and evaluation only and are not used in the demodulation of the incoming signal.

Timing information in the Motorola 2400 bps demodulator is derived directly from the demodulated data signal. This is referred to as data derived timing. The advantage of data

FIGURE 13 — MODULATOR CCITT 511 DATA SCRAMBLER

U1 MC14006
U2 MC14070
U3 MC14069
U4 MC14011
U5 MC14013
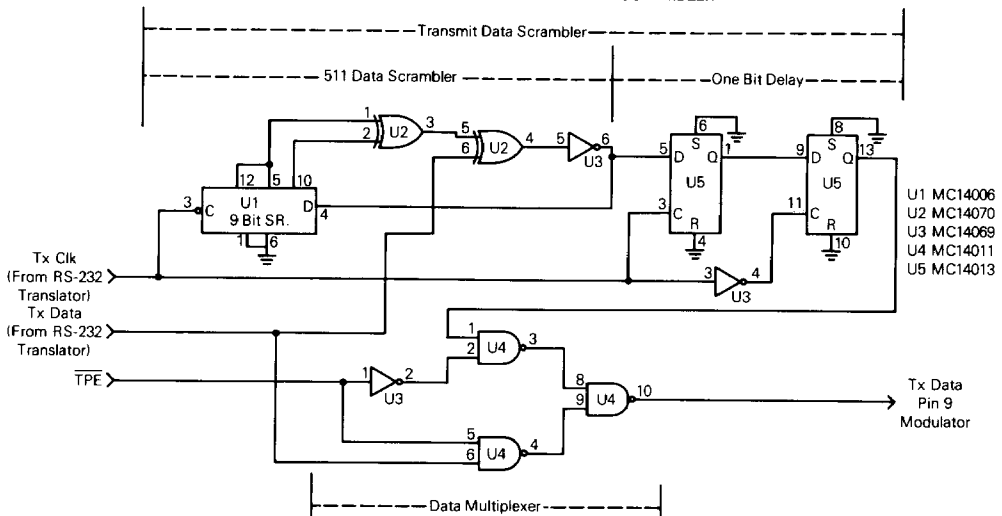
derived time is that it allows data to be sampled at optimum times. The demodulated signals, in differential phase-shift keying, take the form of "eye patterns" as shown in Figure 14. The demodulator, in optimizing its performance for minimum error rates, strobes data at the point of maximum eye opening. The demodulator constantly examines the eye opening to assure that the data sample is being taken at exactly the optimum point. As a result of constantly adjusting timing control, correct sampling is maintained. This technique provides improvements in reception that are significant, especially in a poor communications media environment.

The circuit in Figure 16 is required to observe the eye patterns. This circuit was built using Motorola CMOS devices. The 0 and 90 degree eye data is strobed from pins 4 and 5, respectively, into the shift register by the A/D clock. The A/D strobe then latches the data sample into the "D" type storage devices. The output of the storage devices taken across the scaled resistors will then represent the appropriate value of the sample taken. To properly observe the actual eye patterns, it is necessary to Sync on dibit clock while observing the 0 to 90 degree eye data. Overlaying the two patterns produces a two-level digital-eye pattern from which the quality of the incoming signal may be judged.

Figures 15 thru 17 show a typical receive/demodulator and transmit/modulator circuit, respectively. The transmit filter illustrated in Figure 17 limits the bandwidth of the signal to those frequencies allowed on a telephone line. The receive filter and equalizer in Figure 15 clean up and normalize the incoming signal for the A/D network, 1200 Hz envelope detector, and 1800 Hz carrier detector.

FIGURE 14 — EYE PATTERN

FIGURE 15 — 2400 BPS DPSK DEMODULATOR SYSTEM
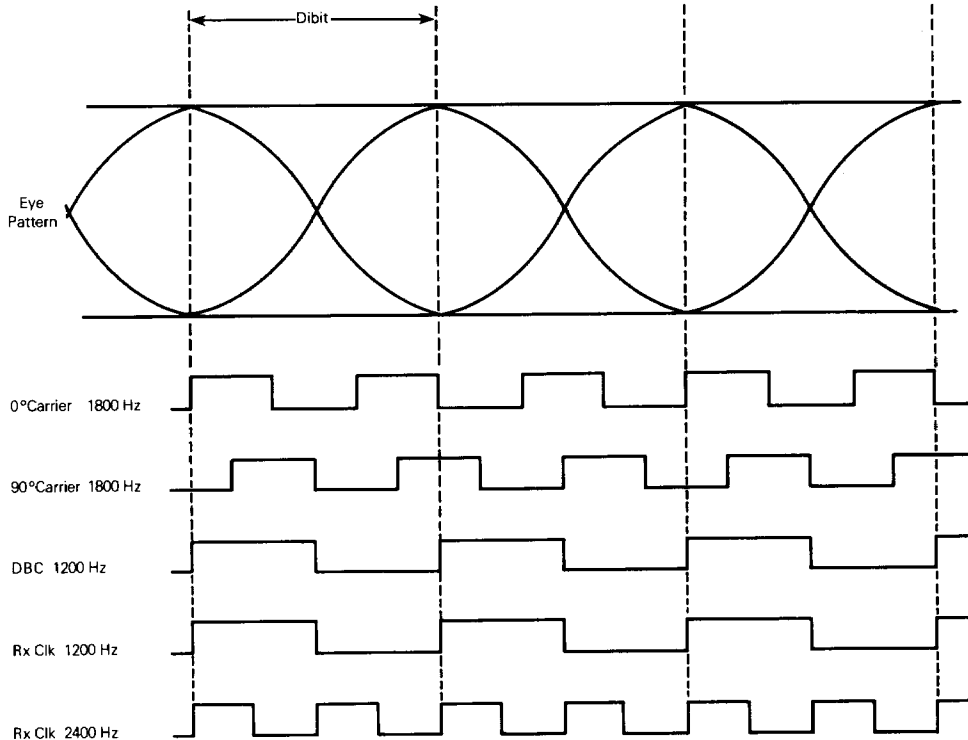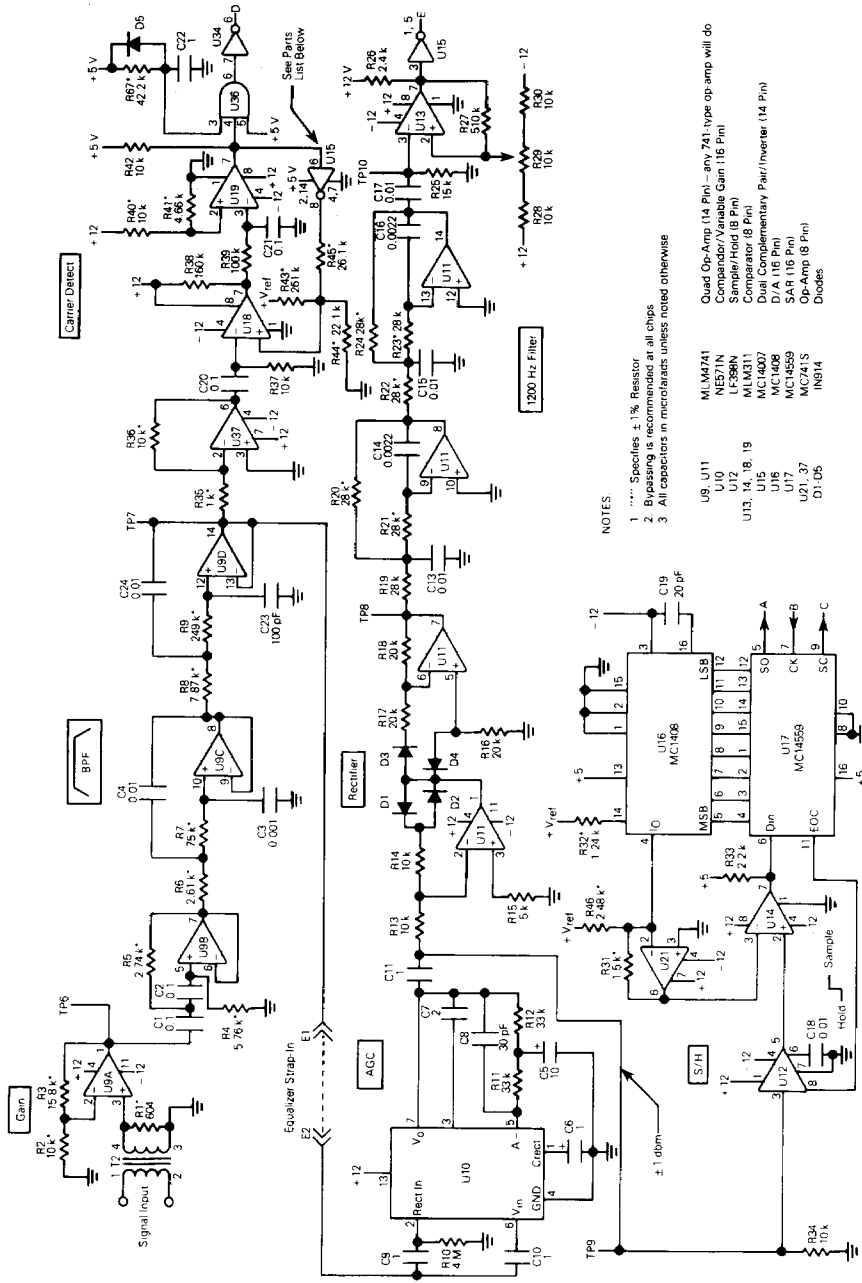
NOTES:
1. ***** Specifies ± 1% Resistor
2. Bypassing is recommended at all chips.
3. All capacitors in microfarads unless noted otherwise

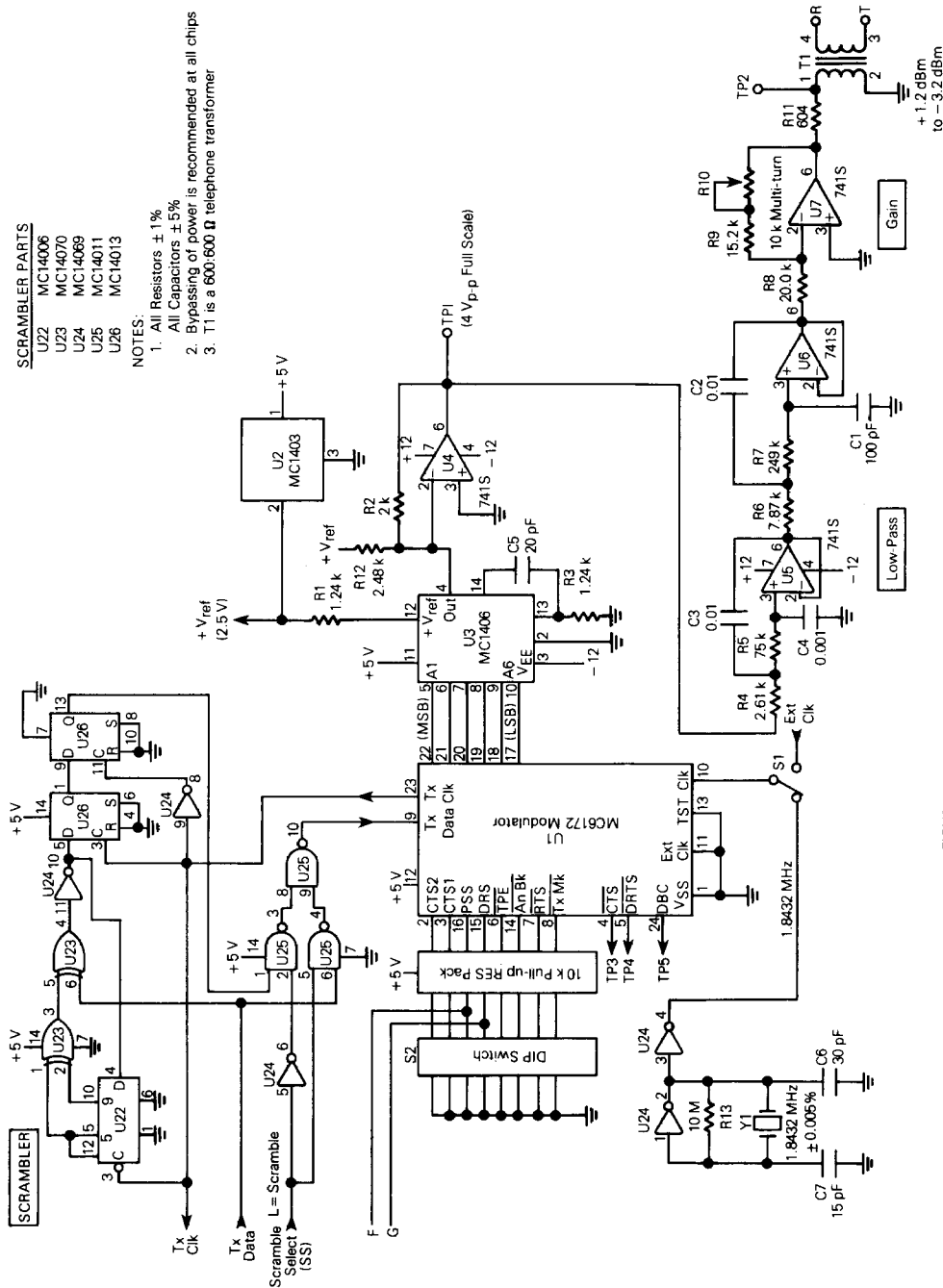| U9, U11 | MLM4741 | Quad Op-Amp (14 Pin) — any 741-type op-amp will do |
U10	NE571N	Compandor/Variable Gain (16 Pin)
U12	LF398N	Sample/Hold (8 Pin)
U13, 14, 18, 19	MLM311	Comparator (8 Pin)
U15	MC14007	Dual Complementary Pair/Inverter (14 Pin)
U16	MC1408	D/A (16 Pin)
U17	MC14559	SAR (16 Pin)
U21, 37	MC741S	Op-Amp (8 Pin)
D1-D5	1N914	Diodes

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FIGURE 16 — 2400 BPS DPSK DEMODULATOR SYSTEM

FIGURE 17 — 2400 BPS DPSK MODULATOR SYSTEM

SCRAMBLER PARTS

U22	MC14006
U23	MC14070
U24	MC14069
U25	MC14011
U26	MC14013

NOTES:
1. All Resistors ± 1%
   All Capacitors ± 5%
2. Bypassing of power is recommended at all chips
3. T1 is a 600:600 Ω telephone transformer