GiGa

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Preliminary

General Description

The GD16521 is a high performance low power 2.5 Gbit/s Laser Driver with optional on chip re-timing of data.

The GD16521 is designed to meet and exceed ITU-T STM-16 and SONET OC-48 fiberoptic communication systems requirements.

The GD16521 is designed to sink a Modulation Current into the IM pin and a Pre-Bias Current into the IB pin. The Modulation Current is adjustable up to 50 mA and the Pre-Bias Current is adjustable up to 100 mA. The device features two control loops for stabilizing the laser diode operating conditions. An automatic optical power control loop maintains a constant average optical power out of the laser diode, independent of changes in the threshold current of the laser diode. A modulation current control loop maintains a constant modulation current for the laser diode, or alternatively maintains a constant extinction ratio of the laser diode.

Re-timing of the data signal connected to the pins SDIP/SDIN is made by means of a DFF-clocked by an external clock signal at the data rate fed to the pins SCIP/SCIN.

The GD16521 requires a single +3.3 V supply.

The circuit is available as:
◆ 48 lead 7 × 7 mm TQFP power enhanced plastic package
◆ die.

Features

● Differential CML data and clock inputs with internal 50 Ω load termination.

● Selectable on chip retiming-FF.

● Output modulation current pulse duty width adjustable (Compensates for LD emission delay)

● Modulation/Bias current monitor output.

● Modulation/Bias current shutdown input.

● Single supply operation: +3.3 V.

● Power dissipation: 410 mW (typ.).

● Available as:
  – 48 lead 7 × 7 mm TQFP power enhanced plastic package
  – die
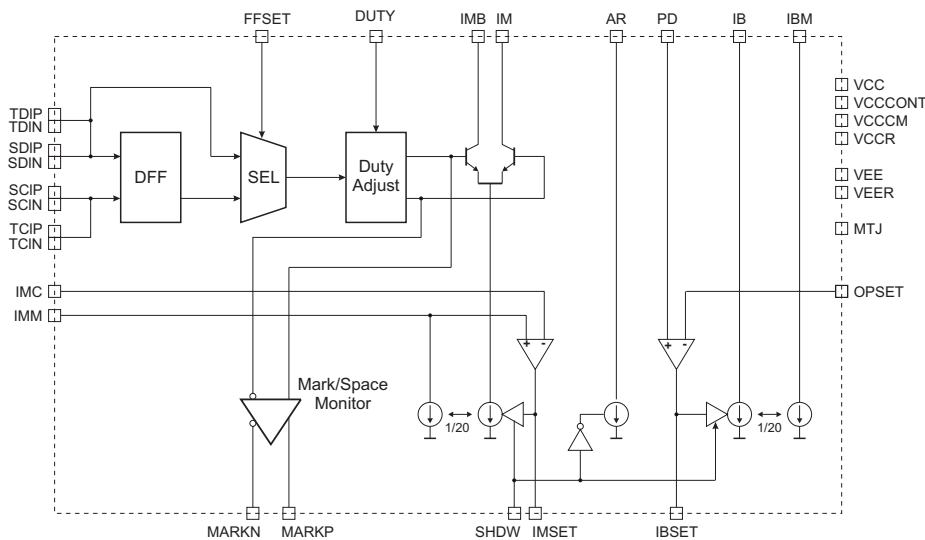
Applications

● Tele Communication:
  – SDH STM-16 modules
  – SONET OC-48 modules

● Data Communication.

● Electro Absorption laser driver.

● Direct Modulation laser driver.

Functional Details

GD16521 is a 2.5 Gbit/s laser driver with an optional re-timing of the data signal. It is capable of driving laser diodes, at a maximum modulation current of 50 mA and a maximum pre-bias current of 100 mA.

The Inputs

Data (SDIP/SDIN) is input to GD16521 and re-timed within a DFF clocked by an external clock (SCIP/SCIN). Optionally the re-timing may be bypassed controlled by a select pin (FFSET).
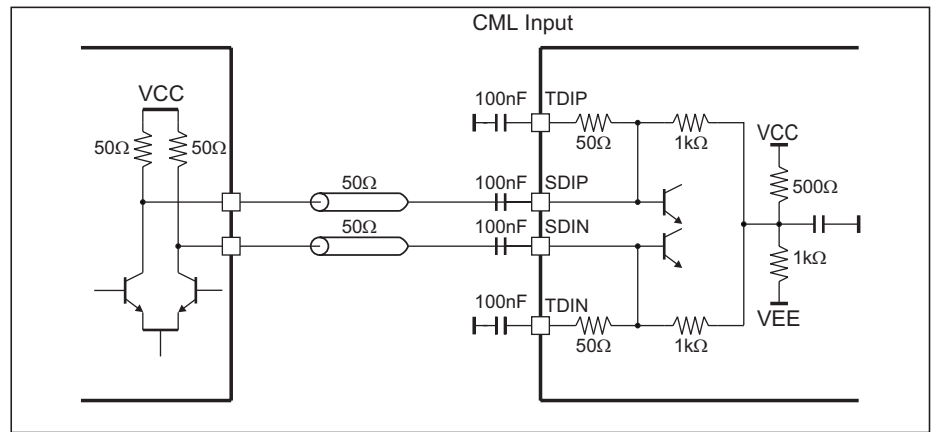
Input Termination

The data inputs (SDIP/SDIN) and clock inputs (SCIP/SCIN)are internally terminated to 50 Ω through the pins TDIP/TDIN and TCIP/TCIN respectively, see Figure 1 below. Using this scheme a VSWR better than 1.5 up to 1.75 GHz and better than 2 up to 2.5 GHz can be achieved. The inputs are internally biased to $2\times(V_{CC} - V_{EE})/3$ with a resistive divider.

The Modulation Current

The output pins (IM/IMB) are open collector outputs designed for driving an external load with a controlled current, typically a laser diode.

The output modulation current can be controlled in the range from 0 mA to 70 mA. The AC specifications are however valid only in the range from 9 mA to 50 mA. The output voltage swing across the external load may be varied accordingly. The external load however must be designed so that the voltage on the output will never be lower than VCC -2 V.

In AC coupling the circuit can be operated at modulation currents above 50 mA. At modulation currents between 50 and 70 mA together with a high operating temperature, there is, however, a small penalty in AC performance. The output jitter can exceed the specification, fall times can exceed the specified values by 10% while rise time are within specifications.

Figure 1. *CML input termination scheme with loop through connection. This example shows an AC coupled differential input configuration.*

Modulation Current Control Loop

A modulation current control loop (MCCL) maintaining a constant modulation current has been incorporated into GD16521. The MCCL OP-amp controls the modulation current so that the voltage across an external resistor caused by the current sink into the IMM pin which is 1/20 of the modulation current equals an external reference voltage applied to the IMC pin. The voltage applied to the IMC pin sets the modulation current. Because the sink current into the IMM pin is 1/20 of the modulation current sink into pin IM the MCCL maintains a constant modulation current. Loop stability is obtained by adding an external capacitor across the OP-amp, see Figure 2 below.

The Pre-bias Current

The pre-bias current can be controlled from 0 mA to 100 mA.

A control loop that maintains a constant average optical power, independent of changes over temperature and lifetime in the laser diode threshold current is incorporated in GD16521. The optical power control loop (OPCL) OP-amp adjusts the laser diode pre-bias current so that the voltage drop across the resistor connected to the back facet monitor diode photo detector, applied to the PD pin, equals the voltage applied to the OPSET pin, see Figure 2 below.

The voltage applied to the OPSET pin determines the average optical power. Loop stability is obtained by adding an external capacitor across the OP-amp.

In addition to the modulation current control and the pre-bias control loops described above, GD16521 features a current mirror of the bias current on the

pin IBM. The mirrored current is 1/20 of the pre-bias current.

Shutdown

Also added is an anti-rush circuitry, which is used to avoid over loading the laser diode during turn on. Typically AR or PD are connected, see Figure 2. In this case, the bias and modulation current are turned off, there will not be any voltage across the resistor connected to the back facet monitor diode photo detector. Therefore, without the anti-rush circuitry, the OPCL will adjust to increase the bias current, effectively setting the bias control voltage to its maximum, regardless of the setting of the voltage on the OPSET pin. Once the bias and modulation current is turned on again, the laser diode will be subject to the full bias current, and this may harm the laser diode. Therefore, an anti-rush circuitry has been provided, which sinks a current into the AR/PD pins when the bias and modulation current is turned off, SHDW = "1". This causes the AR/PD pins to become more negative than the reference voltage on the OPSET pin, and therefore causes the OPCL to turn down the control for the bias current. This ensures a smooth turn on of the laser diode.
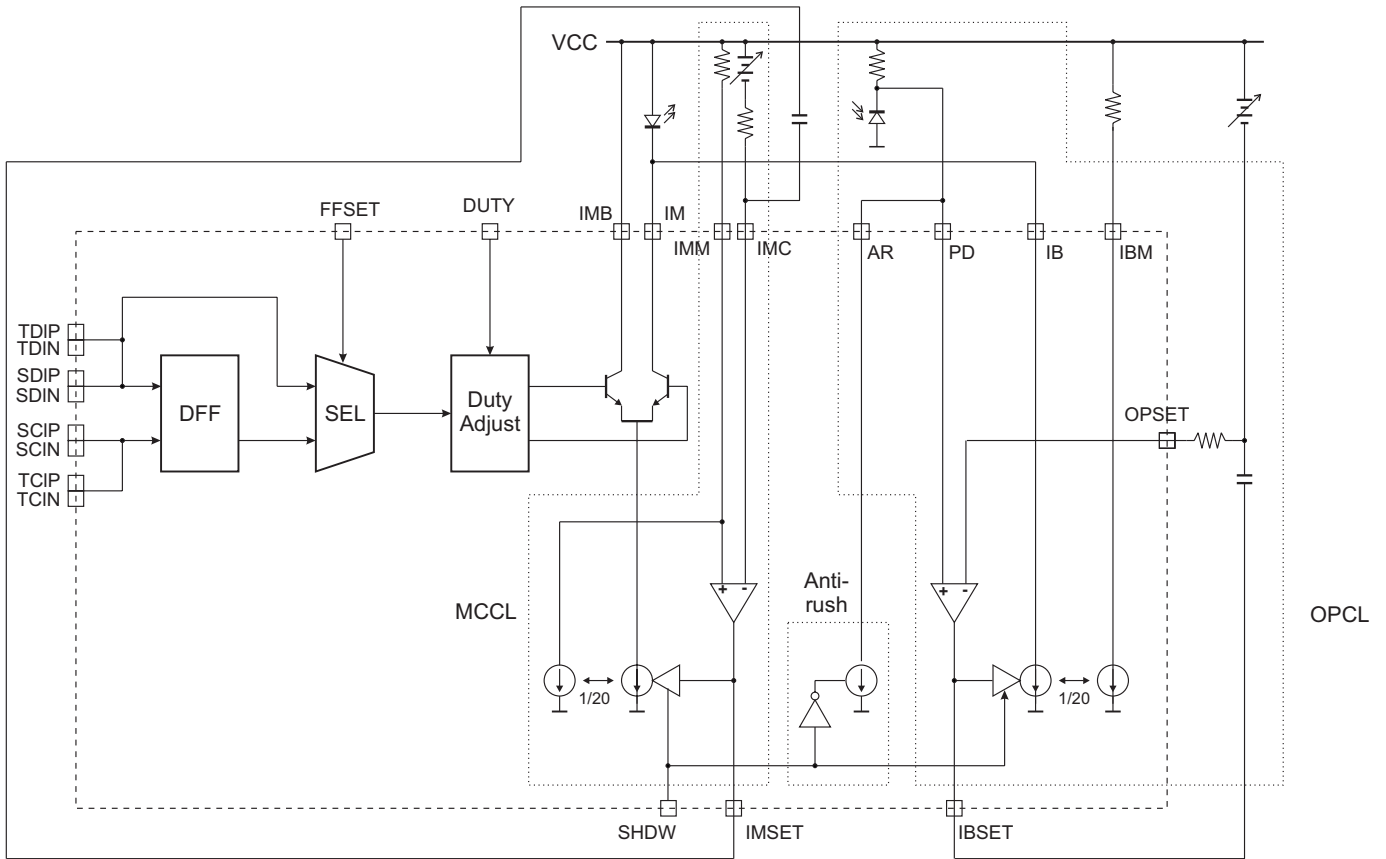
Figure 2. *Modulation current control loop and optical power control loop.*
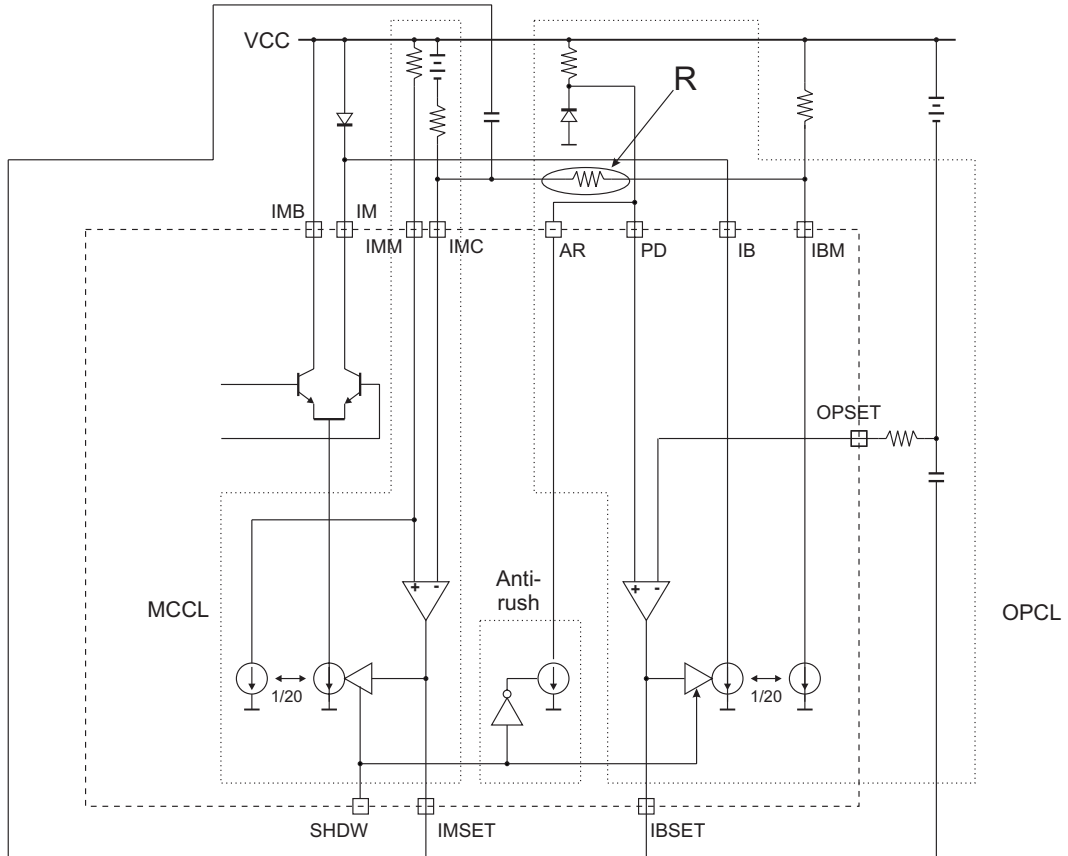
Figure 3. *Modulation current control loop with enhanced extinction ratio control.*

Applications

Temperature Monitor

An on-chip, diode connected transistor is used to monitor the junction temperature in the proximity of the output stage. The voltage at pin MTJ decreases with increasing temperature, see Figure 4.
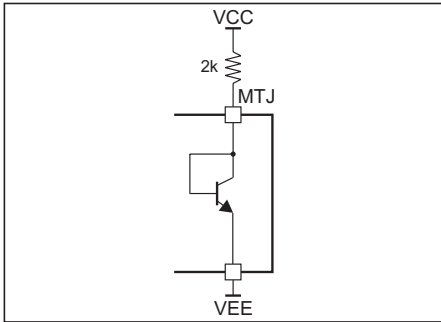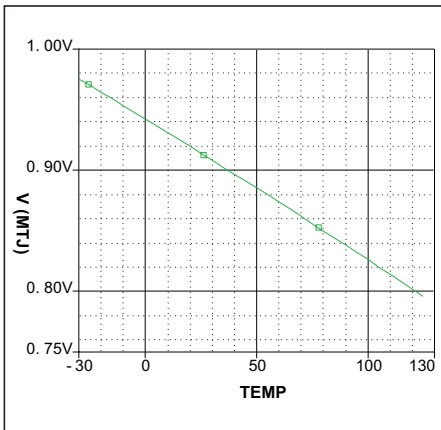

Figure 4. *Temperature Monitor.*

Figure 5. *Voltage at pin MTJ versus Temperature.*

DC Coupling

For a compact design, pre-bias and modulation current can be DC coupled. DC coupling is appropriate when connections between laser driver and laser diode are kept short (with low inductance) as achieved, e.g. by flip-chip mounting of the two dice in close proximity, see Figure 10 on page 5. The GD16521 is optimized for this configuration.

AC Coupling

AC coupling is recommended for the packaged version, in particular when the output is connected to the laser diode through a transmission line, see Figure 6.
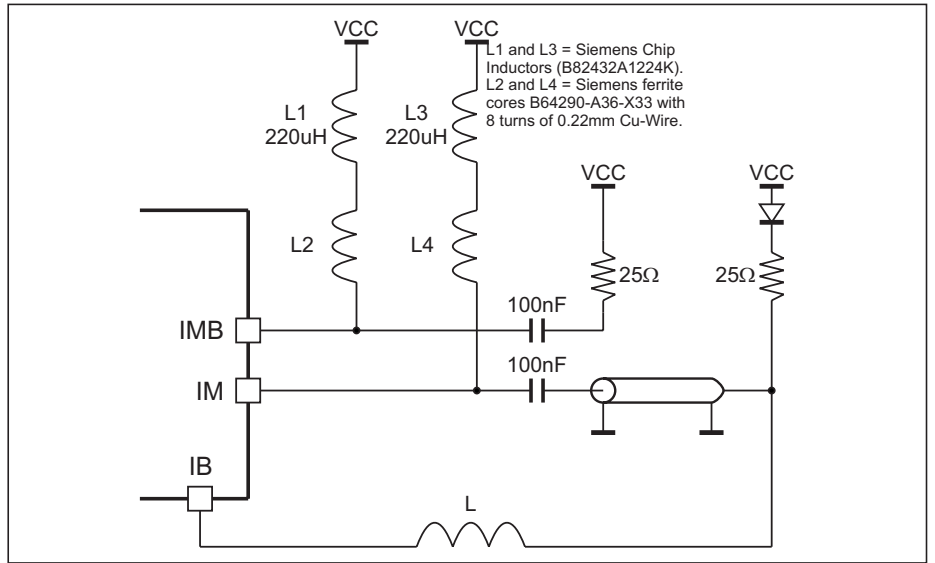
Figure 6. *AC coupled output.*

Duty Cycle Adjustment

The "on-time" of the laser current (IM-pin) can be increased up to 20% by controlling the voltage at the Duty input. In the configuration in Figure 7, a smaller R results in a longer on-time. The duty cycle adjustment can be monitored using the Mark/Space monitor outputs (MARKP/MARKN), see Figure 8.
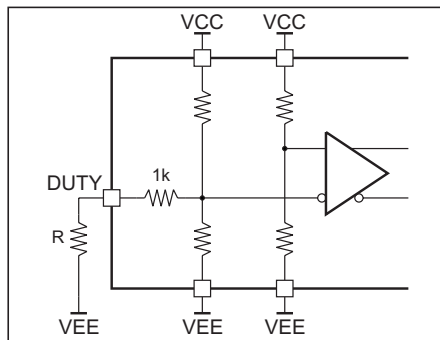

Figure 7. *Duty cycle adjustment with an external resistor.*
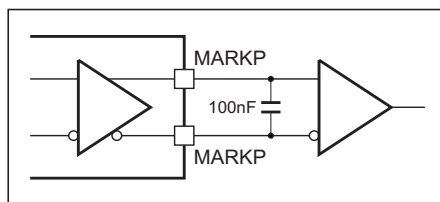

Figure 8. *MARKP/MARKN outputs.*

Laser Diode Slope Efficiency Compensation

The pre-bias control loop may be used to make a simple compensation for changes in the slope efficiency of a laser diode, in order to maintain a constant extinction ratio. Typically the slope efficiency of the laser diode is inversely proportional to the threshold current, as shown in Figure 9 below. Therefore the pre-bias monitor current will compensate changes in the threshold current of the laser diode if it is added to the reference voltage on pin IMC at a ratio. This ratio may be chosen individually for the specific laser diode and is set by an external R as shown in Figure 3 on page 3. Thereby the extinction ratio may be maintained at a constant ratio. The variation of the pre-bias monitor current compared to the pre-bias current is only +/-1% over temperature and supply, ensuring that the performance is not sacrificed by changes in this ratio.
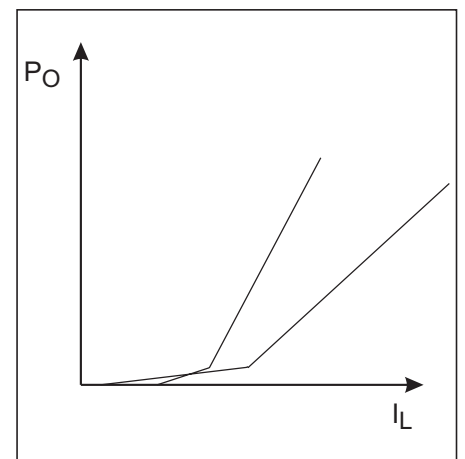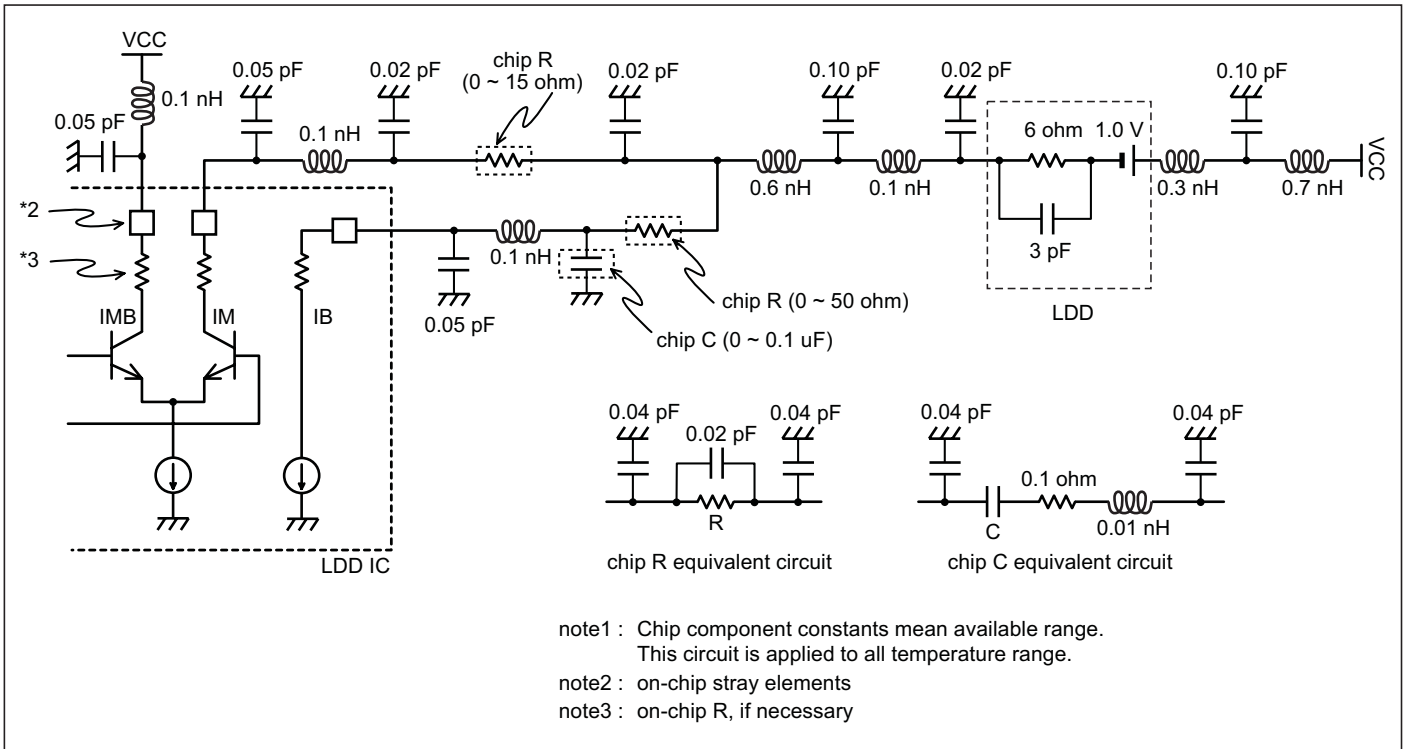

Figure 9. *Laser diode characteristics*

Figure 10. LD Equivalent circuit for simulating of DC coupled flip chip mounted laser driver and laser diode. The capacitors and inductors represent paratisiv elements of the connections. Best performance is achieved with chip R = 10 Ω in bias.

Pin List

Mnemonic:	Pad and Pin No.:	Pin Type:	Description:
SDIP SDIN	4 5	CML IN	Data inputs. Internally terminated with 50 Ω to TDIP/TDIN.
TDIP TDIN	3 6	CML IN	Loop through termination pins for SDIP and SDIN respectively.
SCIP SCIN	9 10	CML IN	Clock inputs. Internally terminated with 50 Ω to TCIP/TCIN.
TCIP TCIN	8 11	CML IN	Loop through termination pins for SDIP and SDIN respectively.
IM	29, 30	OPEN COLLECTOR	Laser Driver Output (2.5 Gbit/s). IM sinks a modulation current, which is controlled by the pin IMSET. A logic HI on SDIP corresponds to IM sinking current.
IMB	31, 32	OPEN COLLECTOR	Laser Driver inverted Output (2.5 Gbit/s). IMB sinks a modulation current, which is controlled by the pin IMSET. Connect to VCC through 20 to 25 Ω.
IB	27	OPEN COLLECTOR	Pre-bias current output. IB sinks a current, which is controlled by the pin IMC.
IMSET	40	ANL OUT	Modulation current control monitor output. This pin is the output of the modulation current control loop OP-amp. For stability a capacitor may be added between this pin and the IMC pin.
IBSET	22	ANL OUT	Pre-bias current control monitor output. This pin is the output of the optical power control loop OP-amp. For stability a capacitor may be added between this pin and the OPSET pin.
IBM	23	ANL OUT	Pre-bias current mirror output. The sink current into the IBM pin is 1/20 of the pre-bias current.
IMM	39	ANL OUT	Modulation current mirror output. The sink current into the IMM pin is 1/20 of the modulation current. Internally IMM is connected to the positive input of the modulation current control loop OP-amp.
AR	25	ANL OUT	Anti-rush current sink. AR sinks a 1 mA current when SHDW is high. Typically connected together with PD to the monitor diode.
MARKP MARKN	35 36	ANL OUT	Mark-space monitor outputs. High impedance CML outputs.
MTJ	38	ANL OUT	Temperature monitor.
IMC	41	ANL IN	Modulation current setting. The modulation current will automatically be adjusted to this value if the internal modulation control loop is used. The IMC pin is the negative input of the modulation current control loop OP-amp.
PD	26	ANL IN	Positive input of the automatic optical power control loop OP-amp, used to control the pre-bias current. Typically connected to the monitor diode photo detector of the laser diode.
OPSET	19	ANL IN	Negative input of the automatic optical power control loop OP-amp, used to control the pre-bias current. Typically connected to an external reference voltage.
FFSET	15	LVTTL IN	When FFSET is low data is re-timed. When high data re-timing is bypassed.
SHDW	16	LVTTL IN	Modulation and pre-bias current shutdown input. Set high for shutdown, low for normal operation.
DUTY	48	ANL IN	Input for control of the mark-space ratio of the output. Decreasing the voltage of the DUTY pin increases the pulse width of a current high into the IM pin. Typically connected to VEE through resistor.
VCC	14, 18, 20, 28, 33, 42, 46	PWR	Positive supply pins for laser driver part.
VCCCONT	44	PWR	Positive supply pin for modulation current control system.

Mnemonic:	Pad and Pin No.:	Pin Type:	Description:
VCCCM	45	PWR	Positive supply pin for output stage operating point control system. Connect to VCCCONT.
VCCR	7, 12	PWR	Positive supply pin for re-timing part.
VEE	13, 17, 24, 34, 37, 43, 47	PWR	Negative supply pins for laser driver and control circuit part.
VEER	1, 2	PWR	Negative supply pin for re-timing part.
NC	21		Not connected.
Heat sink	Package backside		Connected to VEE.

Package Pinout
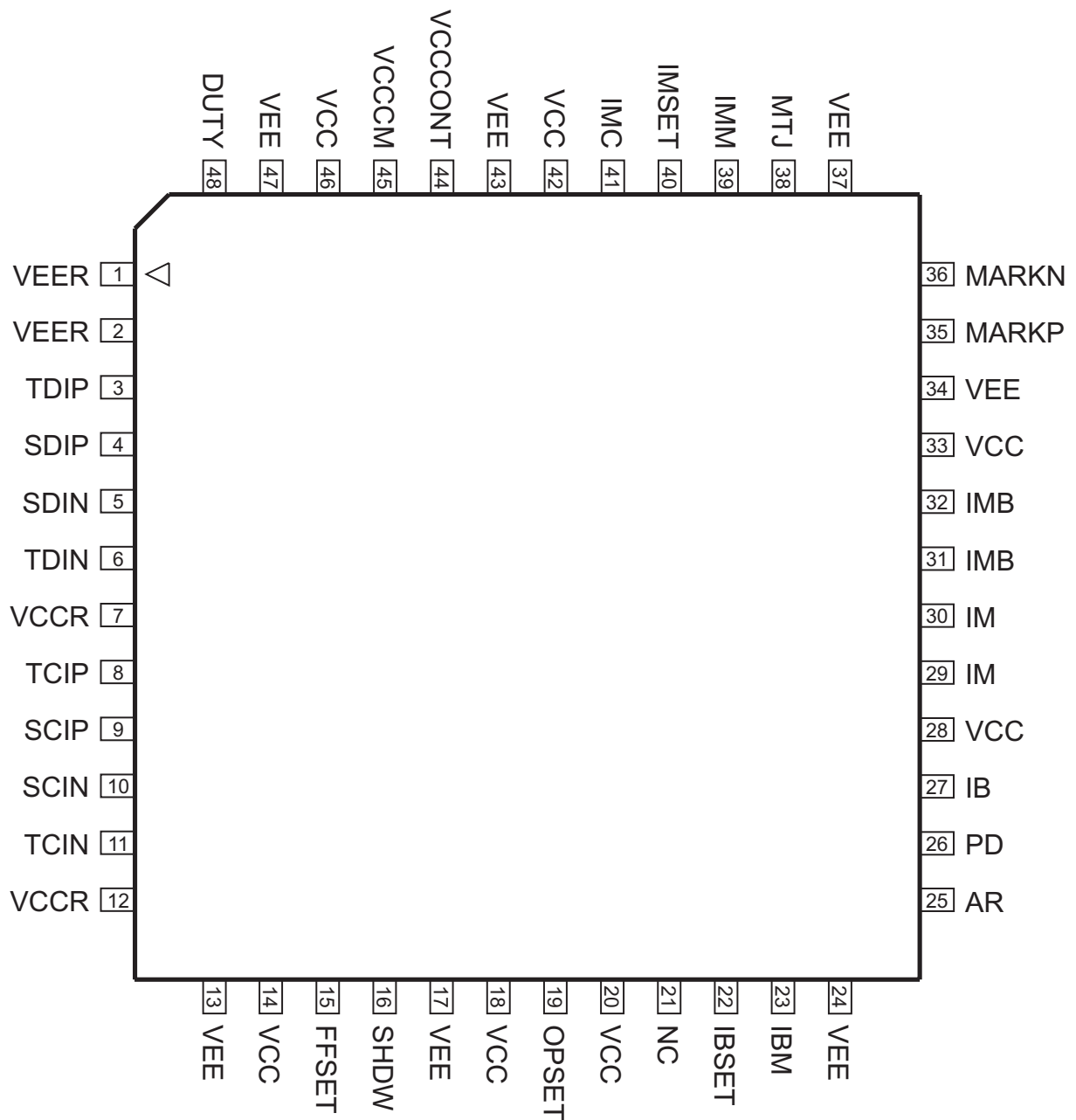
Figure 11. *Package Pinout, Top View.*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VEE.
All currents in table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{cc}	Power Supply		-0.5		6	V
V_O	Applied Voltage (All Outputs)		-0.5		6	V
V_I	Applied Voltage (All Inputs)		-0.5		V_{CC} + 0.5	V
$I_{I\ CML\ IN}$	Input Current		-15		15	mA
T_O	Operating Temperature	Junction	-40		+125	°C
T_S	Storage Temperature		-65		+150	°C
$V_{I/O}\ ESD$	Static Discharge (CML, LVTTL, ANL and PWR)	Note 1, 2	500			V

Note 1: Human body model (100 pF, 1500 Ω) MIL883 std.
Note 2: The pins IM and IMB have no ESD protection.

DC Characteristics

T$_{CASE}$ = -40 °C to +95 °C, appropriate heat sinking may be required, for package parts. Device is DC-tested in the temperature range 0 °C to 85 °C, specifications from -40 °C to 95 °C are guaranteed by design.

T$_{DIE BACK}$ = -30 °C to +100 °C, appropriate heat sinking may be required, for dies. Die is DC-tested at the temperature 85 °C, specifications from -30 °C to +100 °C are guaranteed by design.

All voltages in table are referred to VEE. All input signal and power currents in table are defined positive into of the pin. All output signal currents in table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{CC}	Power Supply		+2.97	+3.3	+3.6	V
I_{CC}	Supply Current	$I_{IM/IMB}$ = 0 A, I_{IB} = 0 A	-170	-125	-110	mA
P_{DISS}	Power Dissipation	V_{CC} = 3.3 V, $I_{IM/IMB}$ = 0 A, I_{IB} = 0 A		410		mW
$V_{Diff\ CML\ IN}$	CML input voltage swing.	Note 4	300		800	mV
$V_{CM\ CML\ IN}$	Common mode voltage for CML input.	Note 4	1.8		V_{CC} - 0.5	V
$Z_{IN\ CML}$	CML input impendance		35	50	65	Ω
$I_{HI\ CML\ IN}$	CML input HI current	Note 3			10	mA
$I_{LO\ CML\ IN}$	CML input LO current	Note 3	-10			mA
V_{IMSET}	Voltage Range for IMSET		0		V_{CC}	V
$V_{IMM/IMC}$	Voltage Range IMM and IMC		2.5		V_{CC}	V
$V_{PD/OPSET}$	Voltage Rang PD and OPSET		2.5		V_{CC}	V
$I_{SINK\ IMM}$	Sink Current into pin IMM		-4			mA
$I_{SINK\ IMB}$	Sink Current into pin IMB		-8			mA
$\Delta_{ABSIM/IMM}$	Absolute Modulation current monitor deviation from I_{IM} /20		-5		5	%
$\Delta_{RELIB/IBM}$	Relative Modulation current monitor error over temperature, supply voltage, and modulation current	T$_{CASE}$ = -10 °C to +95 °C	-2		2	%
		T$_{CASE}$ = -40 °C to +95 °C	-3		3	%
$\Delta_{ABSIB/IBM}$	Absolute Pre-bias current monitor deviation from I_{IB} /20		-4		4	%
$\Delta_{RELIB/IBM}$	Relative Pre-bias current monitor error over temperature, supply voltage, and bias current	I_{IBM} / I_{IM}	-2		2	%
$V_{IN\ IBSET}$	Input Voltage Range for IBSET		0		V_{CC}	V
$V_{IN\ DUTY}$	Input Voltage Range for DUTY		0		V_{CC} /2	V
$R_{IN\ DUTY}$	Input impedance for DUTY		1	TBD		kΩ
$V_{HI\ LVTTL}$	Input High Voltage for FFSET and SHDW		2		V_{CC}	V
$V_{LO\ LVTTL}$	Input Low Voltage for FFSET and SHDW		0		0.8	V
$I_{HI\ LVTTL}$	Input High Current for FFSET and SHDW				50	μA
$I_{LO\ LVTTL}$	Input Low Current for FFSET and SHDW		-500			μA
$V_{O\ IB}$	IB Output Voltage		V_{EE} +1		V_{EE} +5	V
I_{IB}	IB Current		−100		0	mA
$I_{SD\ IB}$	IB Current shutdown mode	SHDW = "1"	−25			μA
$V_{O\ IM}$	IM Output Voltage		V_{EE} +1		V_{EE} +5	V
$I_{Mod,HI\ IM}$	IM High Modulation Current	Note 2	−70		0	mA
$I_{Mod,LO\ IM}$	IM Low Modulation Current	Note 1	−3		1	mA
$I_{SD\ IM}$	IM Current shutdown mode	SHDW = "1"	−25			μA

Note 1: Conditions TBD.
Note 2: The AC parameters are only specified in the range from - 50 mA to - 9 mA.
Note 3: The current is terminated with the external loop through termination.

Note 4: $V_{CM} = \dfrac{V_P + V_N}{2}, V_{Diff} = \left| V_P - V_N \right|$

AC Characteristics

T_{CASE} = -40 °C to +95 °C, appropriate heat sinking may be required, for package parts. Device is AC-tested in the temperature range 0 °C to 85 °C, specifications from -40 °C to +95 °C are guaranteed by design.

$T_{DIE\ BACK}$ = -30 °C to +100 °C, appropriate heat sinking may be required, for dies. Die is not AC-tested. Specifications are guaranteed by design.

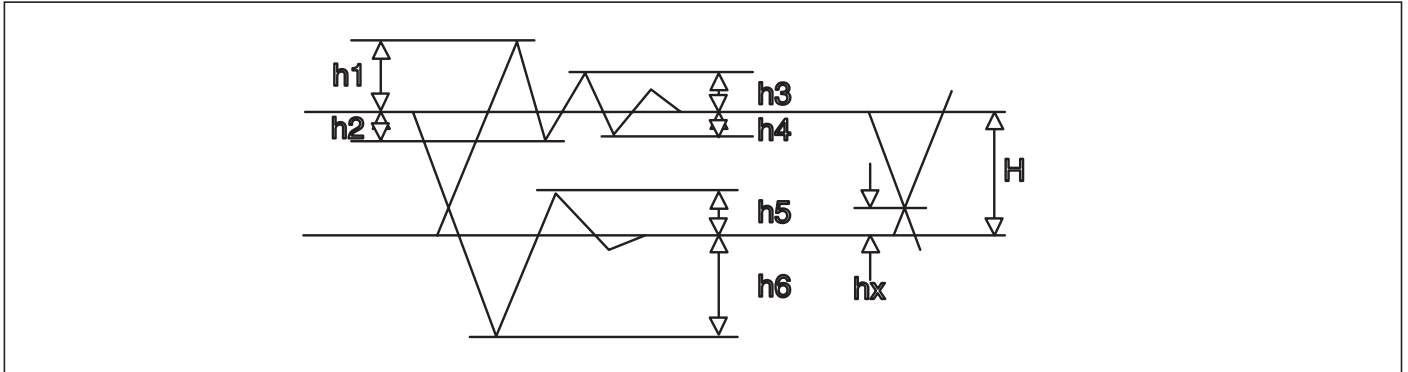**Figure 12.** *LDD Output Definition.*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$f_{MAX\ OUT}$	Data Output Frequency		2500			Mbit/s
$J_{pp}\ IM$	IM Output Pattern Jitter	Note 1, 2			0.06	UI_{PP}
$t_{RISE}\ IM$	IM Output Rise Time (20 - 80 %)	Note 1			100	ps
$t_{FALL}\ IM$	IM Output Fall Time (80 - 20 %)	Note 1			100	ps
D_{range}	Duty Adjustable Range		0		+20	%
t_S	Data Set-up Time		60			ps
t_H	Data Hold Time		60			ps

Target Specifications for Optical Output

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$J_{pp}\ IM$	IM Output Pattern Jitter	Note 3, 2			0.06	UI_{PP}
$t_{RISE}\ IM$	IM Output Rise Time (20 - 80 %)	Note 3			100	ps
$t_{FALL}\ IM$	IM Output Fall Time (80 - 20 %)	Note 3			100	ps
h1/H	Ringing, See figure	Note 3			-	%
h2/H	Ringing, See figure	Note 3			12	%
h3/H	Ringing, See figure	Note 3			7	%
h4/H	Ringing, See figure	Note 3			7	%
h5/H	Ringing, See figure	Note 3			15	%
h6/H	Ringing, See figure	Note 3			-	%
hx/H	Crosspoint, See figure	Note 3	45		55	%

Note 1: R_{LOAD} = 25 Ω to VCC connected to pin IM. I_{LD} = 50 mA. Rise/Fall times at 20 – 80 % of HI/LO voltage levels. IMB connected to VCC.

Note 2: Added jitter. Measured as a peak-peak jitter value on a sampling oscilloscope in 60 s period. Measured with the data re-timing enabled, and using the retiming clock signal as trigger for the oscilloscope.

Note 3: Load is equivalent circuit of LD module, see Figure 10 on page 5 . Input signal is PN23 (2^{23} -1 PRBS). Measured on the optical output of LD module. These specs are target specs.
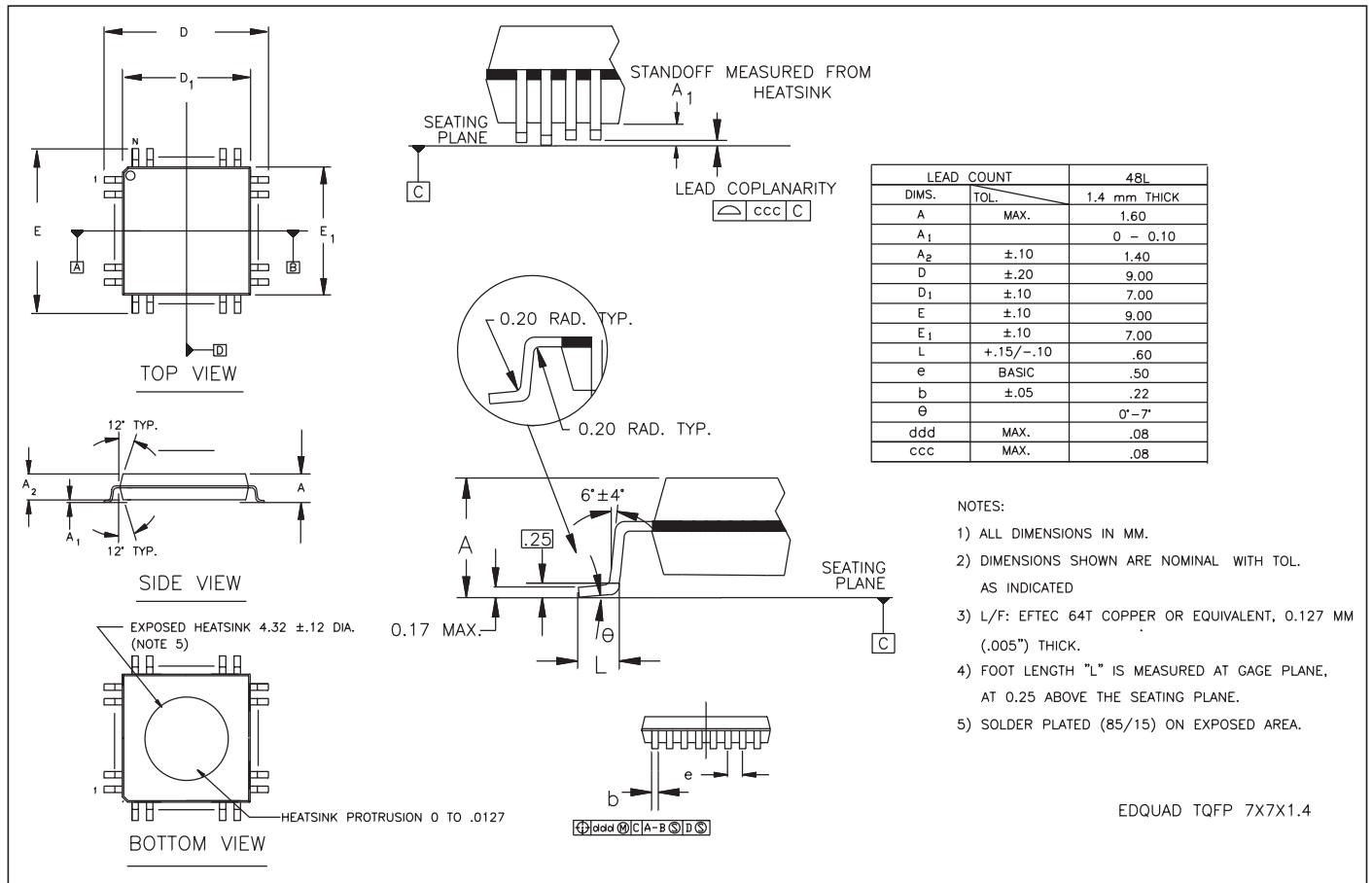
Package Outline

Figure 13. Package 48 pin TQFP. All dimension are in mm.

Side/top/bottom view callouts:

- STANDOFF MEASURED FROM HEATSINK, A₁
- SEATING PLANE
- LEAD COPLANARITY, ccc C
- TOP VIEW
- SIDE VIEW
- 12° TYP.
- EXPOSED HEATSINK 4.32 ±.12 DIA. (NOTE 5)
- HEATSINK PROTRUSION 0 TO .0127
- BOTTOM VIEW
- 0.20 RAD. TYP.
- 6° ±4°
- 0.17 MAX.
- SEATING PLANE

LEAD COUNT		48L
DIMS.	TOL.	1.4 mm THICK
A	MAX.	1.60
A₁		0 – 0.10
A₂	±.10	1.40
D	±.20	9.00
D₁	±.10	7.00
E	±.10	9.00
E₁	±.10	7.00
L	+.15/–.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ddd	MAX.	.08
ccc	MAX.	.08

NOTES:

1) ALL DIMENSIONS IN MM.

2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED

3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") THICK.

4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.

5) SOLDER PLATED (85/15) ON EXPOSED AREA.

EDQUAD TQFP 7X7X1.4

Device Marking

Figure 14. *Device Marking, Top View.*

Die Delivery Conditions

Contact GIGA

Ordering Information

To order, please specify as shown below:

Product Name:	Package Type:	Temperature Range:	Option:
GD16521-D	Die	-30..+100 °C (die back)	
GD16521-48BA	48 pin TQFP EDQUAD	-40..+95 °C (case)	

GD16521, Data Sheet Rev.: 11 - Date: 1 February 2001

an Intel company
Mileparken 22, DK-2740 Skovlunde
Denmark
Phone   : +45 7010 1062
Fax   : +45 7010 1063
E-mail   : sales@giga.dk
Web site : http://www.giga.dk

*Please check our Internet web site
for latest version of this data sheet.*

Distributor: