

Description

The CXP82000 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP82052/82060.

Features

- Wide-range instruction system (213 instructions) to cover various types of data
 - 16-bit operation/multiplication and division/
Boolean bit operation instructions

- Minimum instruction cycle 250ns at 16MHz operation
 122 μ s at 32kHz operation
- Applicable EPROM LCC type 27C512 (Maximum 60K bytes are available.)

- Incorporated RAM capacity 3984 bytes (Including fluorescent display data area)

- Peripheral functions

- A/D converter

8-bit, 8-channel, successive approximation method
(Conversion time of 1.6 μ s/16MHz)

- Serial interface

Incorporated buffer RAM

(Auto transfer for 1 to 32 bytes), 1 channel

8-bit clock sync type (MSB/LSB first selectable), 1 channel

Start-stop sync type(UART), 1 channel

- Timers

8-bit timer

8-bit timer/counter

19-bit time base timer

16-bit capture timer/counter

32kHz timer/counter

- Fluorescent display panel controller/driver

Supports the universal grid fluorescent display panel.

High voltage drive output port of 56 pins (40V)

Maximum of 640 segments display possible

Display timing number of 1 to 20

Dimmer function

Incorporated pull-down resistor (Mask option)

Hardware key scan function

(Maximum 16 \times 8 key matrix compatible)

- Remote control receiving circuit

8-bit pulse measurement counter with on-chip 6-stage FIFO

- PWM output

14 bits, 1 channel

- Interruption

16 factors, 15 vectors, multi-interruption possible

- Standby mode

SLEEP/STOP

- Package

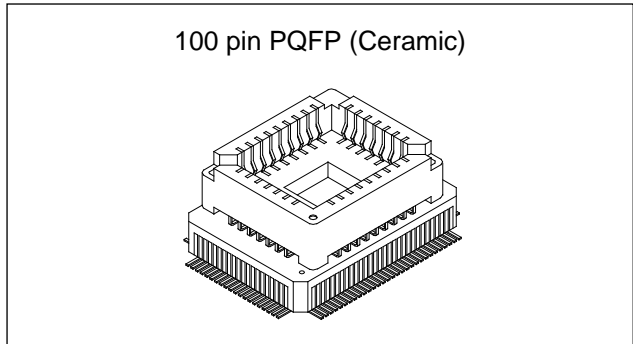
100-pin ceramic PQFP

Note) Mask option depends on the type of the CXP82000. Refer to the Products List for details.

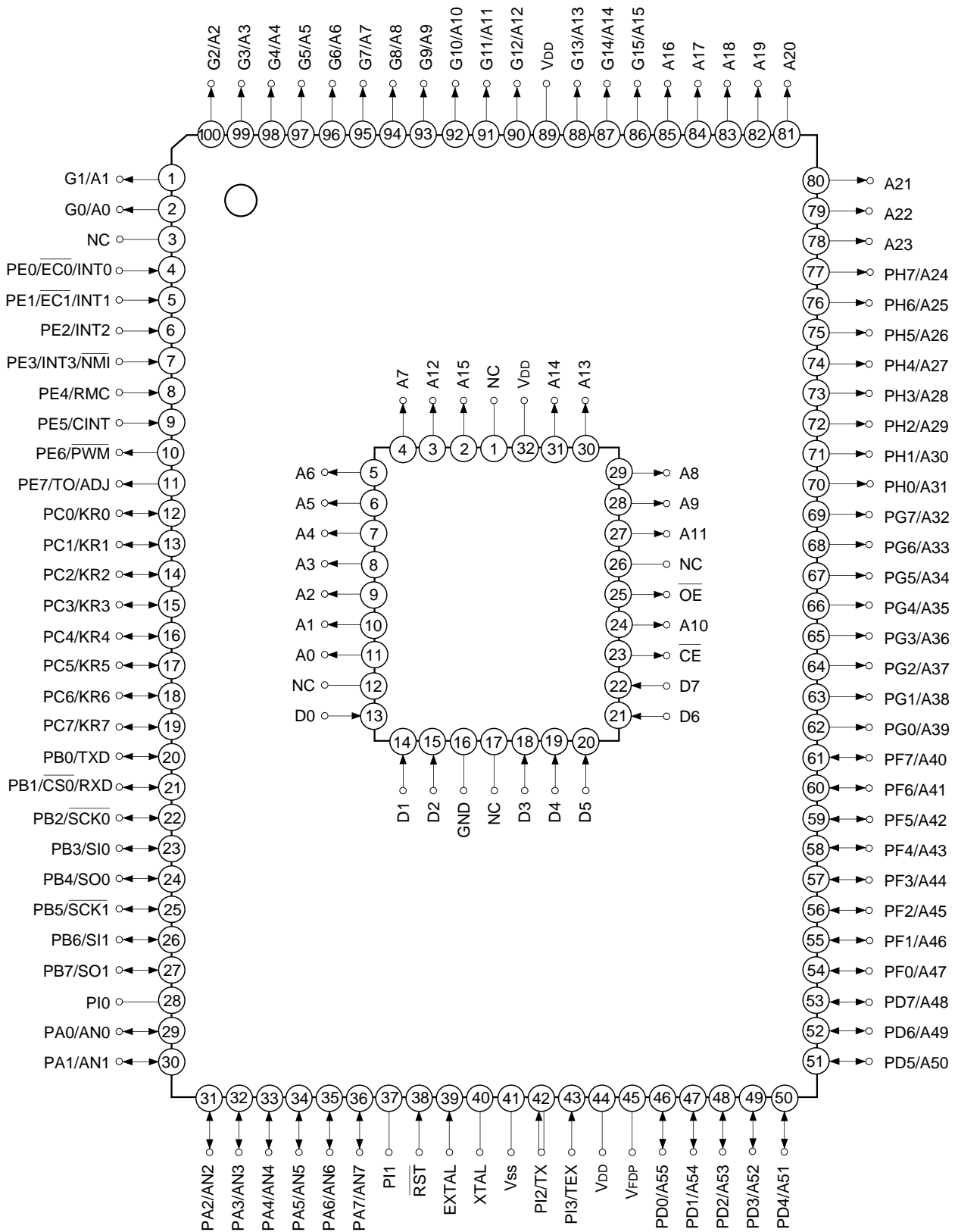
Structure

Silicon gate CMOS IC

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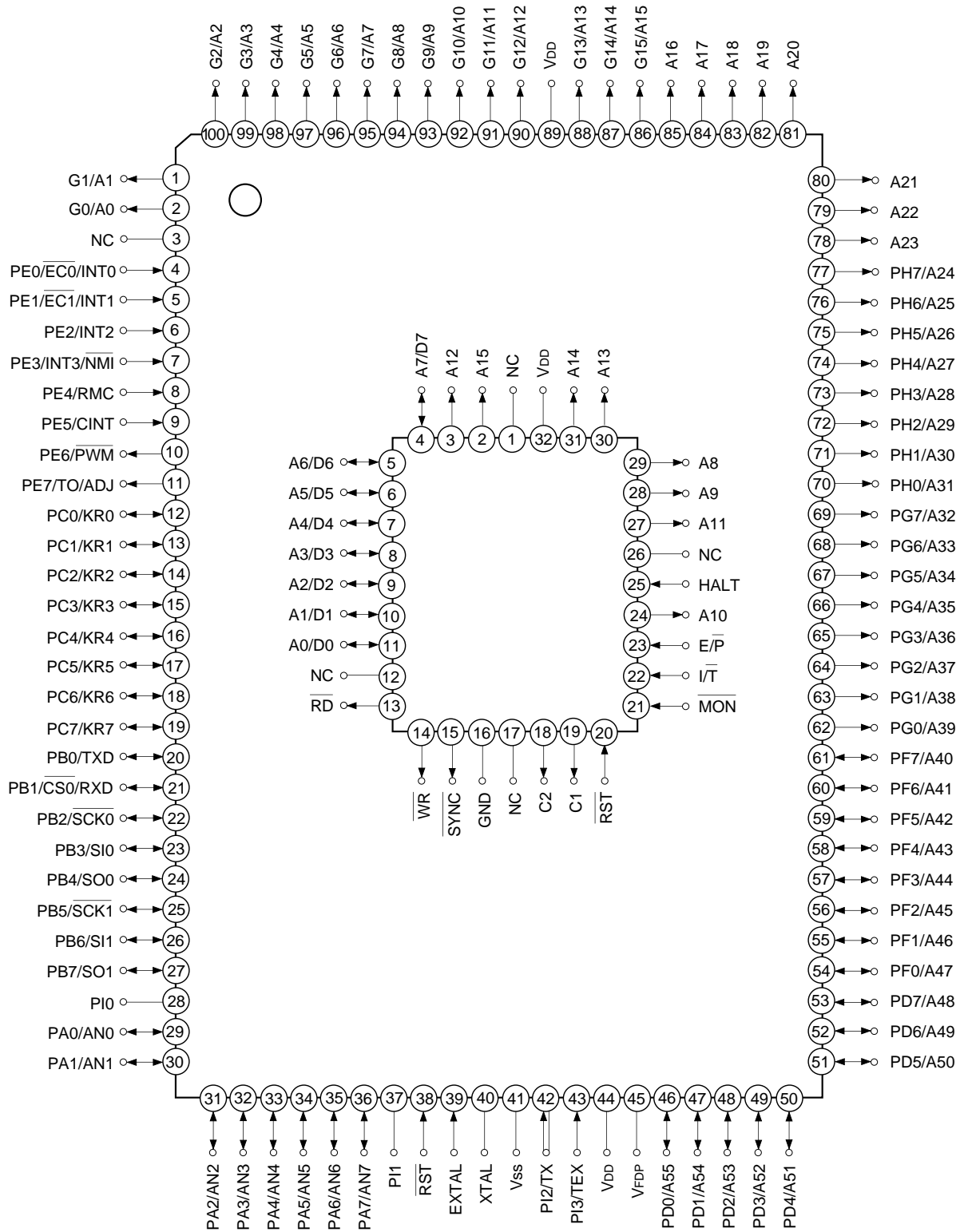


Pin Configuration in Piggyback Mode



- Note)**
1. Do not any connetions toNC (Pin 3).
 2. V_{DD} (Pins 44 and 89) are both connected to V_{DD}.

Pin Configuration in Evaluator Mode

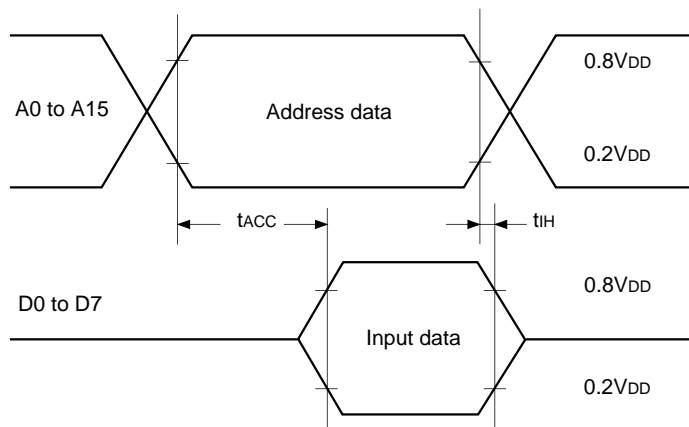


- Note)**
1. Do not any connetions to NC (Pin 3).
 2. VDD (Pins 44 and 89) are both connected to VDD.

EPROM Read Timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{cc} = 4.5$ to 5.5V , $V_{ss} = 0\text{V}$ reference)

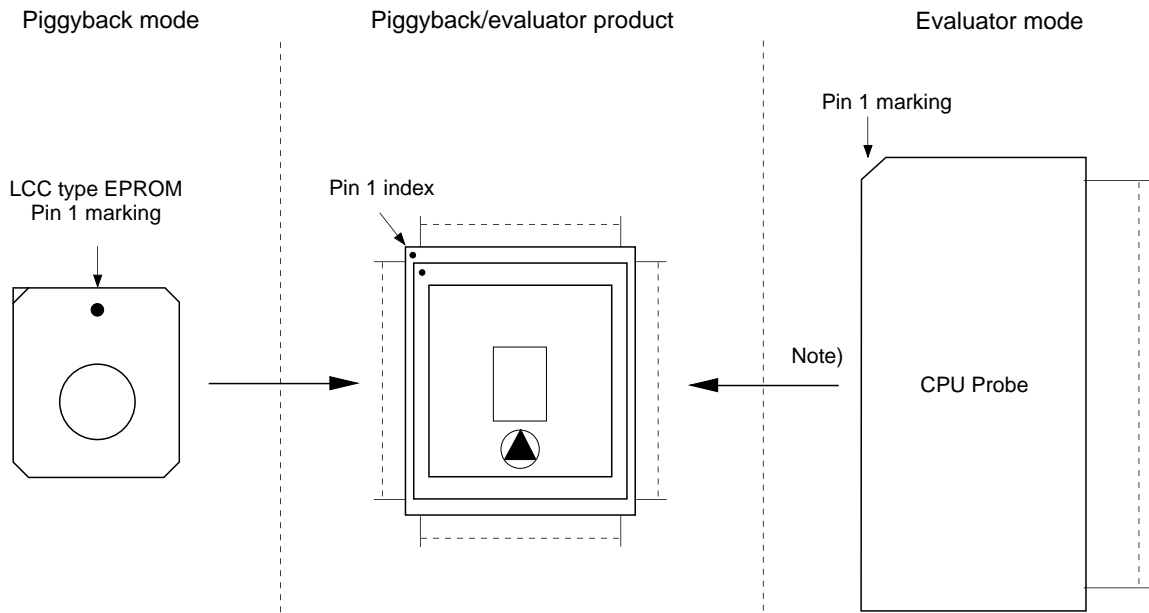
Item	Symbol	Pins	Min.	Max.	Unit
Address → Data input delay time	t_{ACC}	A0 to A15 D0 to D7		120	ns
Address → Data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns



Products List

Option item	Products		
	Mask		Piggyback/evaluator
	CXP82052	CXP82060	CXP82000-U01Q
Package	100-pin plastic QFP		100-pin ceramic PQFP
ROM capacitance	52K bytes	60K bytes	EPROM 60K bytes
Pull-up resistance for reset pin	Existent/Non-existent		Existent
Pull-down resistance for high voltage drive pin	Existent/Non-existent		Existent: G0/A0 to A23 Non-existent: PD0/A55 to PH7/A24

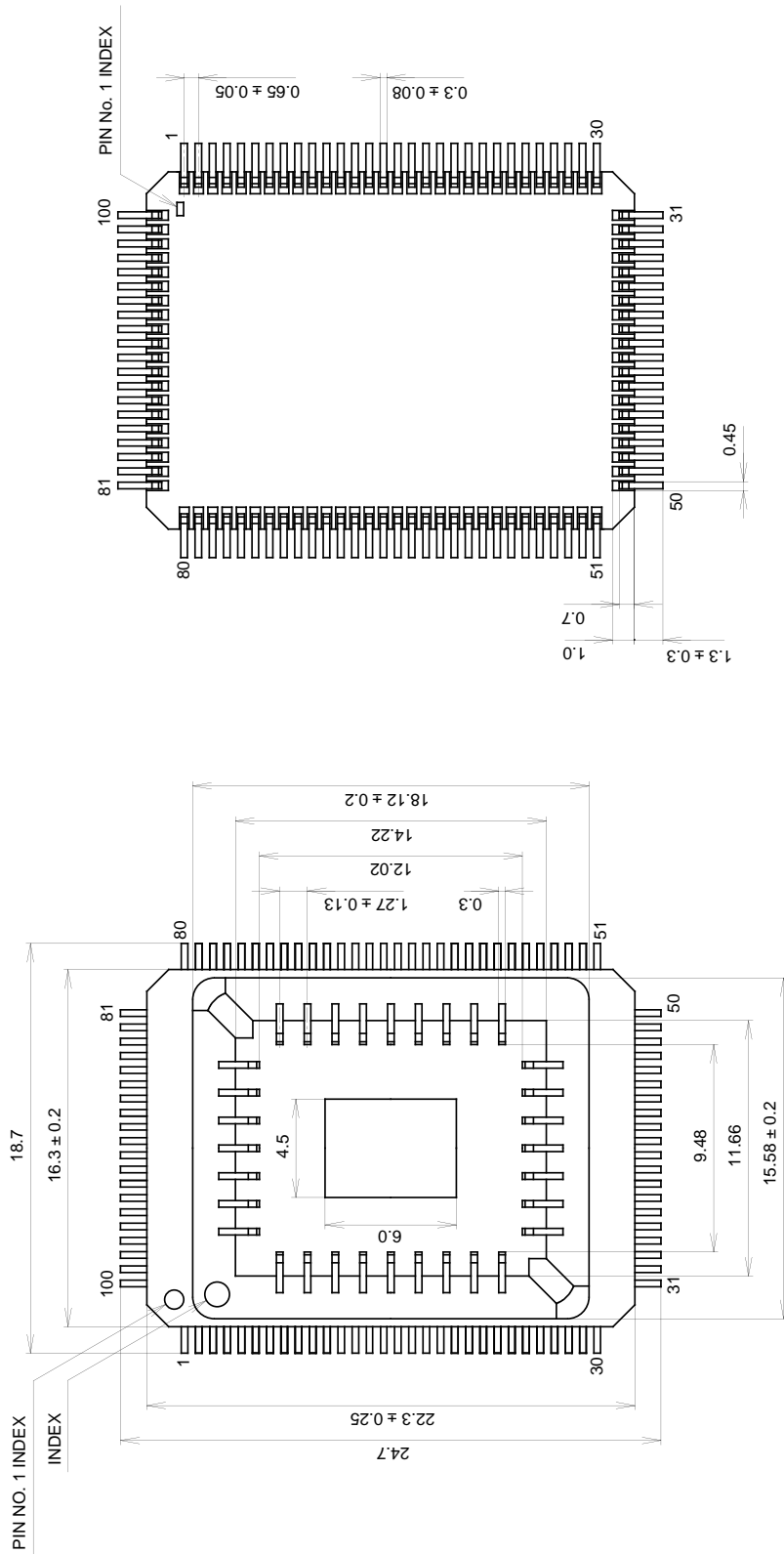
Piggyback mode/evaluator mode can be switched as shown below.



Note) Evaluation cap should be connected to CPU probe.

Package Outline Unit: mm

100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

SONY CODE	PQFP-100C-L01
EIA/J CODE	AQFP100-C-0000-A
JEDEC CODE	

