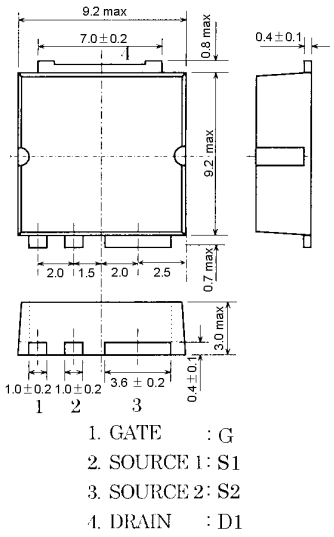
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (L^2-π-MOSV)

2SK3387

Switching Regulator, DC-DC Converter and Motor Drive Applications

Unit: mm



JEDEC	—
JEITA	SC-97
TOSHIBA	2-9F1B

Weight: 0.74 g (typ.)

- 4 V gate drive
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 0.08 Ω(typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 17 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (V_{DS} = 150 V)
- Enhancement-mode: V_{th} = 0.8~2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	150	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	150	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	18	A
	Pulse (Note 1)	I_{DP}	54	
Drain power dissipation (Tc = 25°C)		P_D	100	W
Single pulse avalanche energy (Note 2)		E_{AS}	176	mJ
Avalanche current		I_{AR}	18	A
Repetitive avalanche energy (Note 3)		E_{AR}	10	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	1.25	°C/W

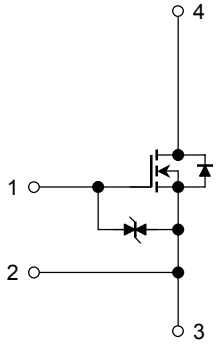
Notice:
Please use the S1 pin for gate input signal return. Make sure that the main current flows into S2 pin.

Note 1: Please use devices on condition that the channel temperature is below 150°C.

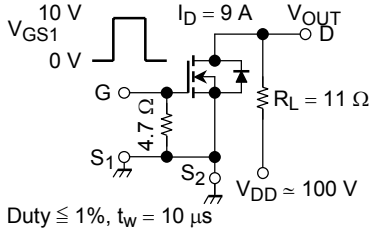
Note 2: V_{DD} = 50 V, T_{ch} = 25°C (initial), L = 800 μH, R_G = 25 Ω, I_{AR} = 18 A

Note 3: Repetitive rating: pulse width limited by max junction temperature

This transistor is an electrostatic sensitive device.
Please handle with caution.



Electrical Characteristics (Note 4) (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = 150 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	150	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 9 A	—	0.09	0.18	Ω
			V_{GS} = 10 V, I_D = 9 A	—	0.08	0.12	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 9 A	10	17	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1380	—	pF
Reverse transfer capacitance		C_{rss}		—	200	—	
Output capacitance		C_{oss}		—	610	—	
Switching time	Rise time	t_r		—	12	—	ns
	Turn-on time	t_{on}		—	20	—	
	Fall time	t_f		—	12	—	
	Turn-off time	t_{off}		—	68	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 120 V, V_{GS} = 10 V, I_D = 18 A	—	57	—	nC
Gate-source charge		Q_{gs}		—	43	—	nC
Gate-drain (“miller”) charge		Q_{gd}		—	14	—	nC

Note 4: Please connect the S1 pin and S2 pin, and then ground the connected pin.
(However, while switching times are measured, please don’t connect and ground it.)

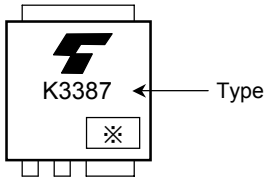
Source-Drain Diode Ratings and Characteristics (Note 5) (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current	(Note 1, 5)	$I_{DR}1$	—	—	—	18	A
Pulse drain reverse current	(Note 1, 5)	$I_{DRP}1$	—	—	—	54	A
Continuous drain reverse current	(Note 1, 5)	$I_{DR}2$	—	—	—	1	A
Pulse drain reverse current	(Note 1, 5)	$I_{DRP}2$	—	—	—	4	A
Diode forward voltage		V_{DS2F}	I_{DR1} = 18 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time		t_{rr}	I_{DR} = 18 A, V_{GS} = 0 V,	—	185	—	ns
Reverse recovery charge		Q_{rr}	dI_{DR}/dt = 100 A/μs	—	1.3	—	μC

Note 5: drain, flowing current value between the S2 pin, open the S1 pin
drain, flowing current value between the S1 pin, open the S2 pin

Unless otherwise specified, please connect the S1 and S2 pins, and then ground the connected pin.

Marking

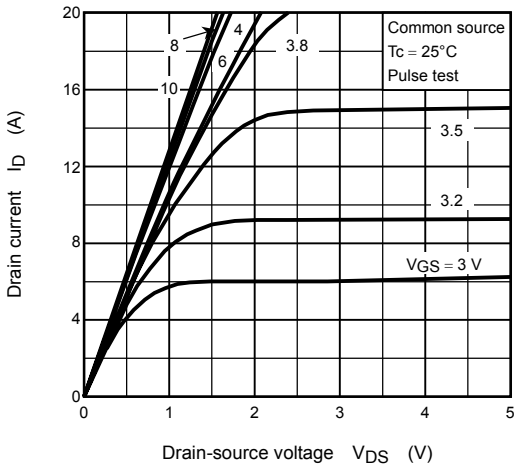


※ Lot Number

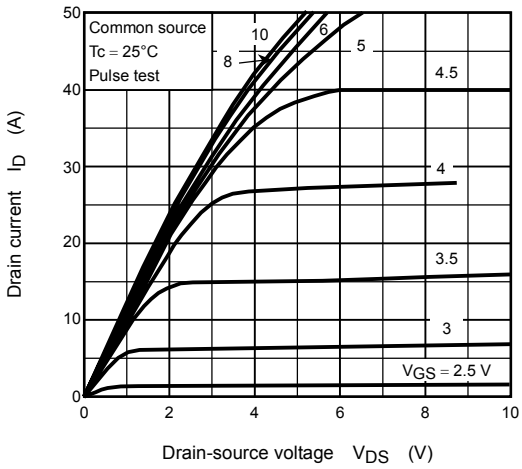
Month (starting from alphabet A)

Year (last number of the christian era)

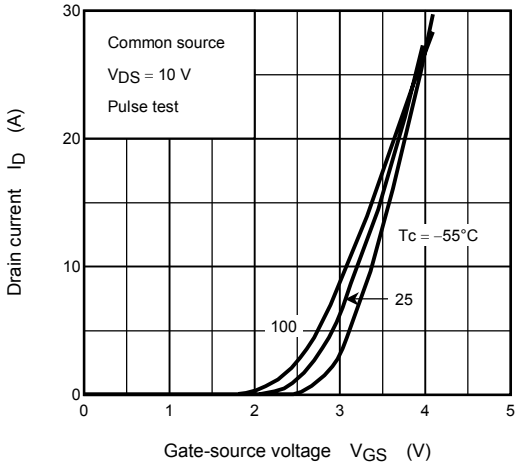
$I_D - V_{DS}$



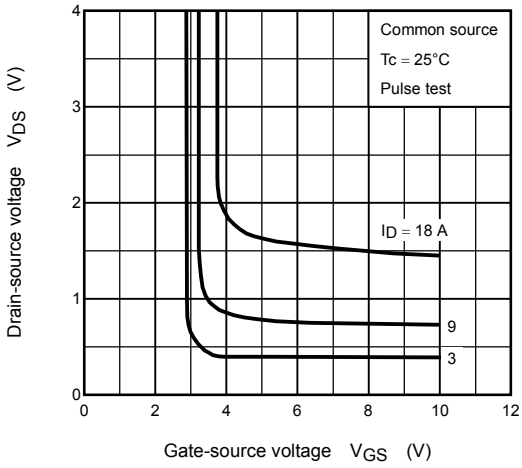
$I_D - V_{DS}$



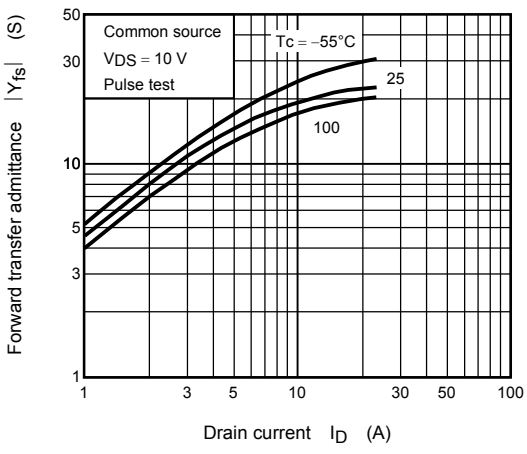
$I_D - V_{GS}$



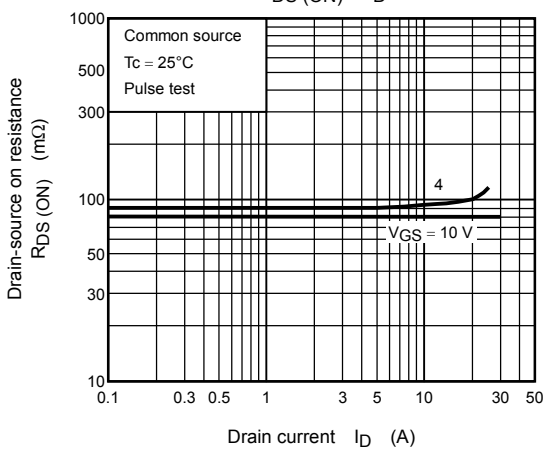
$V_{DS} - V_{GS}$



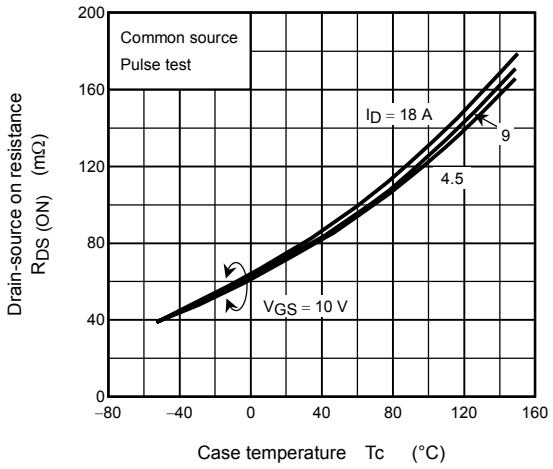
$|Y_{fs}| - I_D$



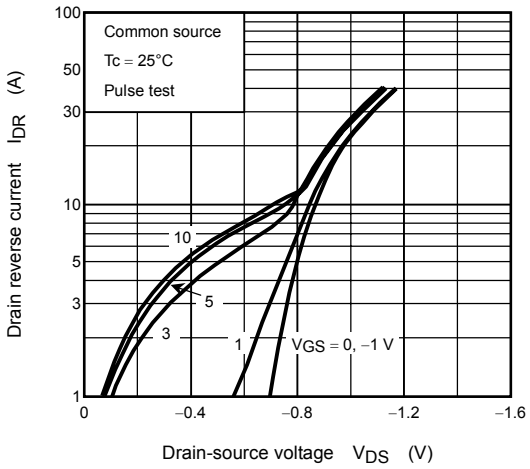
$R_{DS\ (ON)} - I_D$



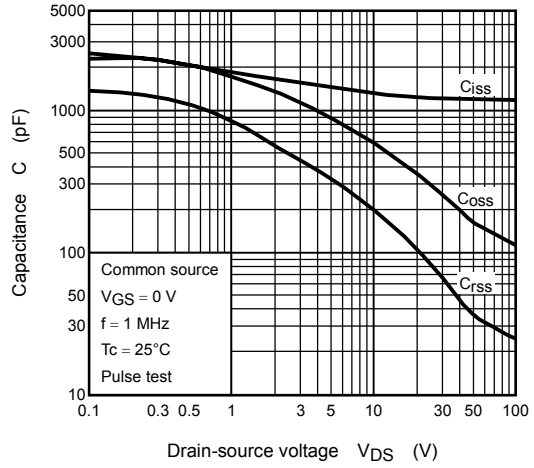
$R_{DS\ (ON)}$ – Tc



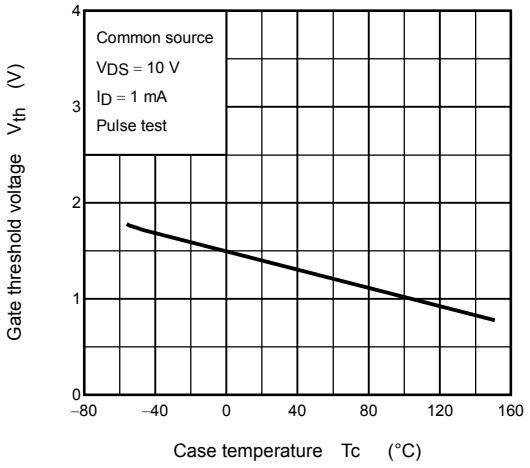
I_{DR} – V_{DS}



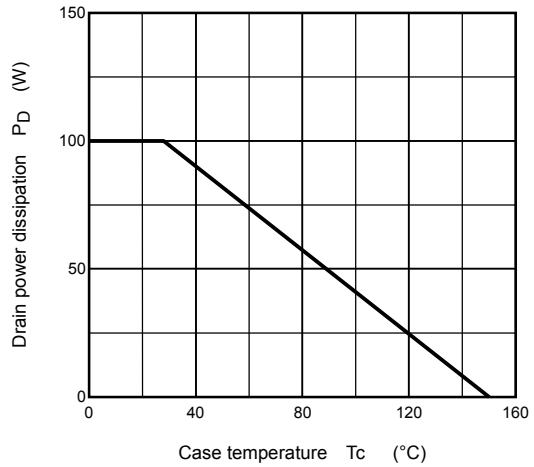
Capacitance – V_{DS}



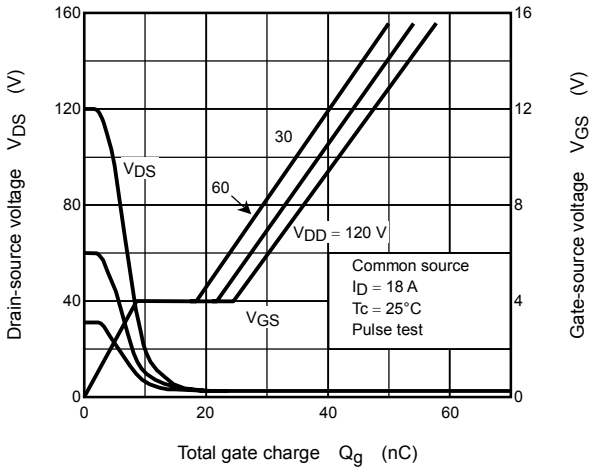
V_{th} – Tc



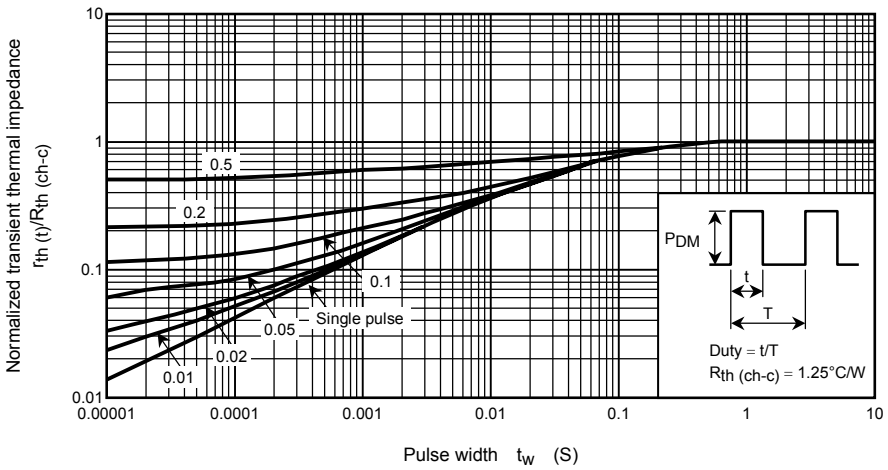
P_D – Tc



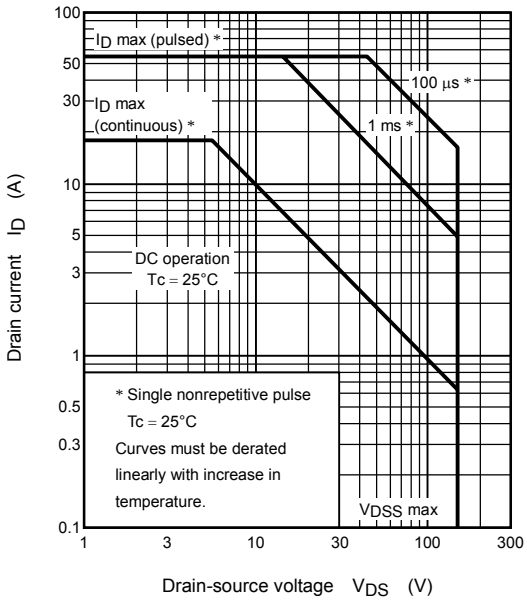
Dynamic input/output characteristics



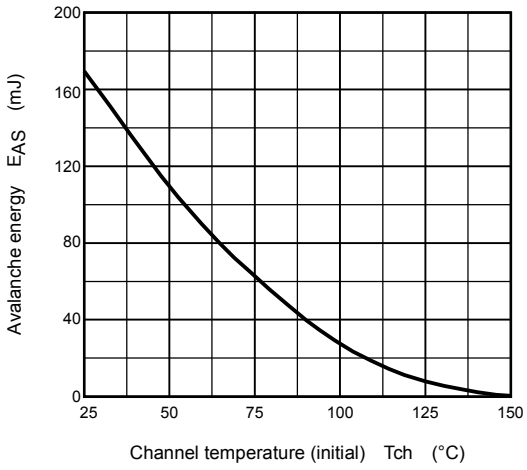
$r_{th} - t_w$

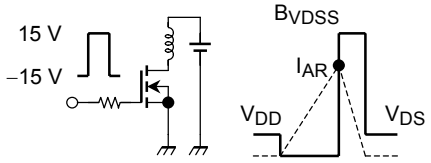


Safe operating area



$E_{AS} - T_{ch}$





Test circuit Wave form

$R_G = 25\ \Omega$
$V_{DD} = 50$ V, L = 0.8 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

RESTRICTIONS ON PRODUCT USE

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