TDA 2140

LINEAR INTEGRATED CIRCUIT

PAL SUBCARRIER REFERENCE OSCILLATOR FOR COLOUR TV

The TDA 2140 is a monolithic integrated circuit for regenerating and processing the subcarrier reference signals in the decoder circuit of PAL colour TV receivers. It is encapsulated in a 16-lead dual in-line plastic package and its main features are:

- High stability of the subcarrier oscillator with supply voltage and temperature variations.
- High noise immunity in ACC and APC circuits obtained by means of detectors activated only during key pulse
- High noise immunity in identification circuit
- Integrated 90° phase shifter
- No adjustments of ACC (Automatic Color Control) needed
- Hysteresis in coulor killer circuit
- Internal circuit, driven by flyback pulse, generated a composite blanking and burst key pulse
- When the antenna signal decreases, the saturation of the chroma signal is automatically reduced before colour killer action.
- Colour killer activated if the antenna signal is too low, if the oscillator is not locked, if the burst is absent or if PAL identification is wrong.

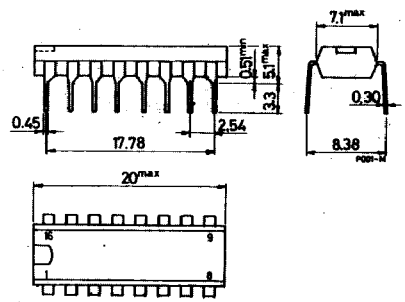
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 2)	15	V
V_{15}	Voltage at pin 15	$\begin{cases} +12 \\ -50 \end{cases}$	V
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

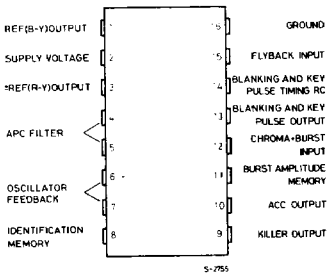
ORDERING NUMBER: TDA 2140

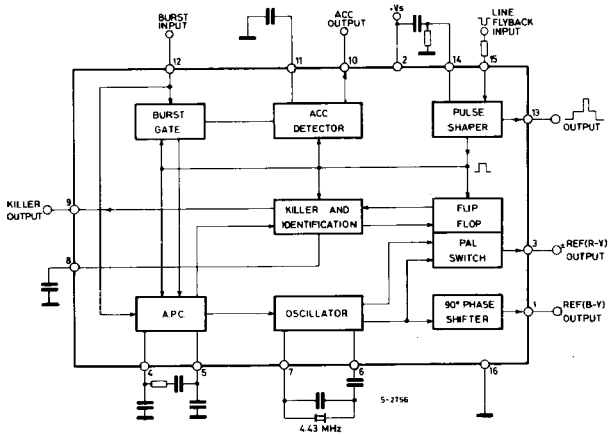
MECHANICAL DATA

Dimensions in mm

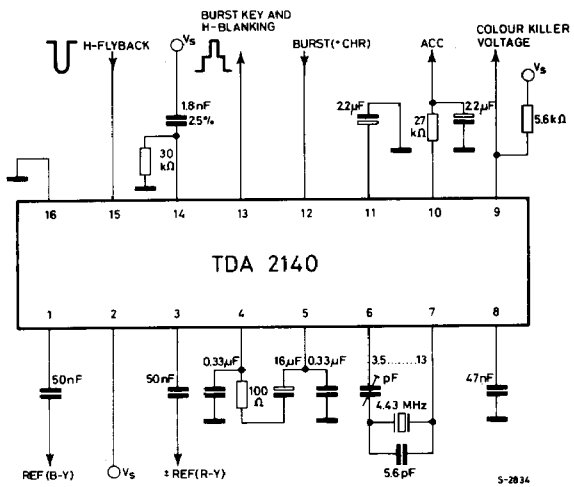


CONNECTION AND BLOCK DIAGRAMS
(top view)





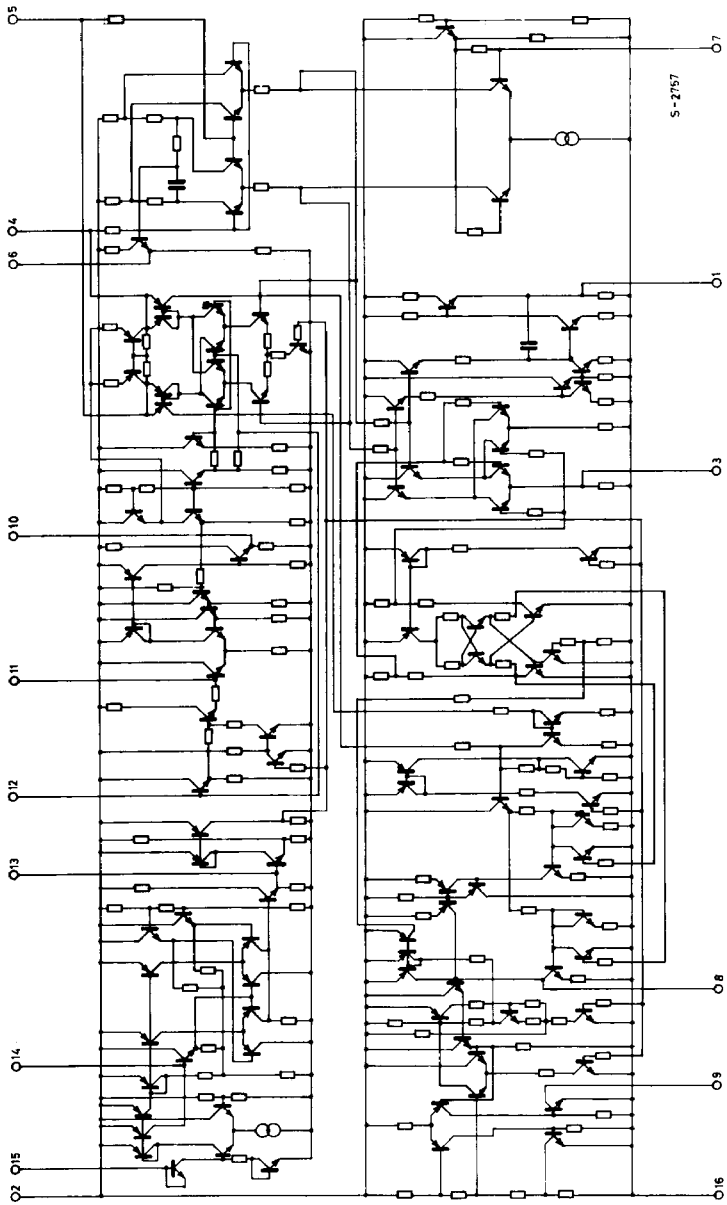
TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

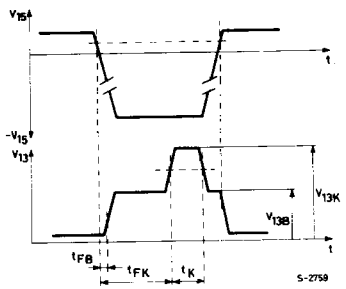
(Refer to the test circuit; V_s = 12V, f_o = 4.43 MHz, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 2)		10.8		13.2	V
I_s	Supply current (pin 2)			45	64	mA
V_1	Ref. (B-Y) peak to peak output voltage			0.9		V
R_1	Ref. (B-Y) output resistance			100		Ω
V_3	± Ref. (R-Y) peak to peak output voltage			0.9		V
R_3	± Ref. (R-Y) output resistance			100		Ω
V_9	Colour killer output	Correct phase of PAL flip-flop	11.4			V
		Incorrect phase of PAL flip-flop			0.5	V
V_{10}	ACC output voltage (note 1)	V_{12} = 0.9 Vpp		1		V
V_{12}	Burst peak to peak input voltage (note 1)			0.9		V
V_{13K}	Key pulse peak output voltage (note 2)			5		V
V_{13B}	Blanking pulse peak output voltage (note 2)		2.1	2.5		V
R_{13}	Output resistance			100		Ω
t_K	Key pulse duration (note 2)	V_{13} = 3V		3.5		µs
t_{FK}	Phase relation between leading edges of flyback and key pulses (note 2)	V_{13} = 3V V_{15} = 1V	6.5	6.8		µs
t_{FB}	Delay between flyback and blanking pulses (note 2)	V_{13} = 1V V_{15} = 1V		0.4		µs
V_{15}	Input voltage of composite blanking and key pulse generator (flyback pulse) (note 2)	$V_{13} \leq 0.2V$	2.5		7.5	V
		$V_{13} \geq 1V$	-50		+ 1	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
R_{15}	Line flyback pulse input resistance	V_{15} = 2.5V		1		kΩ
φ	Phase angle between Ref (B-Y) and Ref (R-Y) output signals		85	90	95	°
Δf	Pull-in range	V_{12} = 0.9 Vpp		+300 -400		Hz
$\frac{\Delta\varphi}{\Delta f}$	Static phase shift	Δf = ± 400 Hz		10		°/kHz
$\frac{\Delta f}{\Delta T_{amb}}$	Oscillator frequency thermal drift	T_{amb} = 20 to 60°C		1		Hz/°C
$\frac{\Delta f}{\Delta V_s}$	Oscillator frequency voltage drift	V_s = 10.8 to 13.2V		10		Hz/V

Notes: 1 - Measured in closed loop configuration with TDA 2151 chroma amplifier.
2 - Composite blanking and key pulse waveform.



APPLICATION INFORMATION

Pin 1 - Ref. (B-Y) output
The Ref. (B-Y) signal is obtained from the oscillator waveform by means of an operational amplifier with capacitive feedback, which guarantees a 90° phase shift with ± 5° accuracy. Pin 1 has low output impedance and shows a triangular waveform.

Pin 2 - Positive supply
The operating supply voltage of the device ranges from 10.8V to 13.2V.

Pin 3 - ± Ref. (R-Y) output
The phase of this signal is changed line by line from 0° to 180° by means of the PAL flip-flop, which is driven by the key pulses and is reset by the identification circuit. Pin 3 has low output impedance and shows a square waveform.

APPLICATION INFORMATION (continued)

Pin 4 - Automatic phase control circuit
The APC circuit, which generates the voltage to control the oscillator by comparing the burst and oscillator waveforms, is activated only during the key pulse time. Therefore high noise immunity of the oscillator phase control is achieved. The filter network connected to pins 4 and 5 determines the bandwidth of the APC loop.

Pin 5 - (see pin 4)

Pin 6 - Oscillator
The tuning network of the oscillator is connected to pins 6 and 7. The free running frequency of the oscillator is calibrated by means of the variable capacitor connected in series to the quartz. The pull-in range is typically +300 Hz -400 Hz; its slight asymmetry is due to the characteristics of the circuit which controls the oscillator. The pull-in range can be enlarged by reducing the value of the capacitor connected in parallel to the quartz, but it should never fall below 3.3 pF.

Pin 7 - (see pin 6)

Pin 8 - Identification circuit
The capacitor connected between pin 8 and ground memorizes the identification circuit status. The identification circuit performance is influenced by the value of this capacitor and suitable ground layout must be provided. To reduce the identification sensitivity, a 6.8 MΩ resistor can be connected in parallel to the capacitor.

Pin 9 - Colour killer
Pin 9 is the output of the colour killer which is controlled by the identification circuit. Colour killing occurs if the antenna signal is too low, if the oscillator is not locked, if the burst is absent or if PAL identification is wrong. Colour killer activation and deactivation occur with different delays and with a hysteresis which eliminates the possibility of system oscillation.

Pin 10 - ACC detector
Pin 10 is the output of the ACC voltage to control the gain of the TDA 2150 chroma amplifier. At pin 11 the capacitor of the burst peak detector is connected to avoid annoying effects on the picture due to colours being affected by a very noisy signal. The ACC detector gradually desaturates the picture before the killer switches off the colours, in the event of low antenna signal levels.

Pin 11 - (see pin 10)

Pin 12 - Burst input circuit
Pin 12 is the input of the burst signal which is picked up together with the chrominance signal and has to be separated from the remainder of the line. This is done by the burst gate controlled by the key pulse. If the burst is coupled to the TDA 2140 via a band pass filter, the relative phase between sub-carriers and chrominance signal can be calibrated so that correct picture colours are obtained even with broadcasts which do not correspond perfectly to the PAL standard.

Pin 13 - Composite blanking and key pulse generator (sandcastle pulse)
The low impedance sandcastle pulse available at pin 13 of the IC is obtained from the flyback pulse applied at pin 15. The flyback pulse must be negative and have a maximum amplitude of 55 Vpp.
The precision of the sandcastle timing is determined by the tolerances of the RC network connected to pin 14 of the IC; to avoid calibration, the maximum tolerances allowed are ± 2% for the resistance and ± 2.5% for the capacitance. When the composite blanking and key pulse are available from any other circuit, e.g. from jungle IC, the sandcastle generator of the TDA 2140 can not be used. In this case, the sandcastle pulse is sent to pin 13 of the TDA 2140, pin 14 is brought directly to V_s and pin 15 is brought to V_s via a 5.6 kΩ resistor. The internal circuit picks up the key pulse required to operate the IC.

Pin 14 - (see pin 13); Pin 15--(see pin 13); Pin 16 - Ground