3.3V, PRECISION, 33MHz to 500MHz PROGRAMMABLE LVPECL AND LVDS BUS CLOCK SYNTHESIZER

Precision Edge®
SY89534L
SY89535L

FEATURES

- **Integrated synthesizer plus fanout buffers, clock dividers, and translator in a single 64-pin package**
- **Accepts any reference input between 14MHz to 160MHz (single-ended or differential)**
- **33MHz to 500MHz output frequency range**
- **LVPECL outputs (SY89534L)**
  LVPECL and LVDS outputs (SY89535L)
- **3.3V ±10% power supply**
- **Low jitter: <50ps cycle-to-cycle**
- **Low pin-to-pin skew: <50ps**
- **TTL/CMOS compatible control logic**
- **3 independently programmable output frequency banks:**
  - **9 differential output pairs @BankB (LVPECL/LVDS)**
  - **2 differential output pairs @BankA (LVPECL)**
  - **2 differential output pairs @BankC (LVPECL)**
- **Available in 64-pin EPAD-TQFP**

Precision Edge®

DESCRIPTION

The SY89534L and SY89535L programmable clock synthesizers are a 3.3V, high-frequency, precision PLL-based family optimized for multi-frequency, large clock-tree applications that require the highest precision. These devices integrate the following blocks into a single monolithic IC:

- PLL (Phase-Lock-Loop)-based synthesizer
- Fanout buffer
- Clock generator (divider)
- Logic translation (LVPECL, LVDS)

The SY89534L and SY89535L includes a flexible input design that accepts any reference input; single-ended LVTTL/CMOS, SSTL and differential LVPECL, LVDS, HSTL and CML.

This level of integration minimizes the additive jitter and part-to-part skew associated with the discrete alternative, resulting in superior system-level timing as well as reduced board space and power. For applications that must interface to a crystal oscillator, see the SY89532/33.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

APPLICATIONS

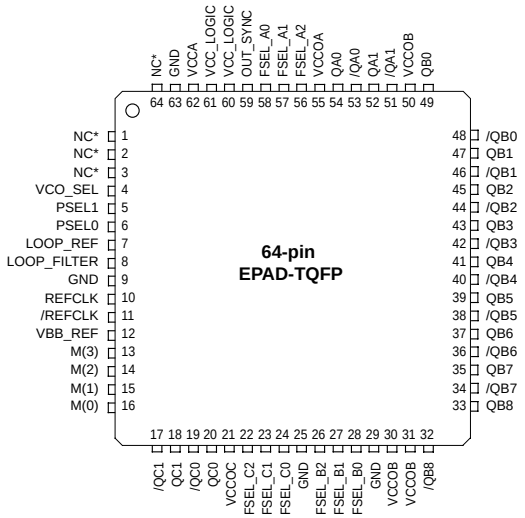
- **Servers**
- **Workstations**
- **Parallel processor-based systems**
- **Other high-performance computing**
- **Communications**

PRODUCT SELECTION GUIDE

	Input		Output		
Device	Crystal	Reference	BankA	BankB	BankC
SY89532L*	X		LVPECL	LVPECL	LVPECL
SY89533L*	X		LVPECL	LVDS	LVPECL
SY89534L		X	LVPECL	LVPECL	LVPECL
SY89535L		X	LVPECL	LVDS	LVPECL

*Refer to SY89532/33L data sheet for details.

PACKAGE/ORDERING INFORMATION



64-Pin EPAD-TQFP (H64-1)

*NC: Do not connect, leave floating.

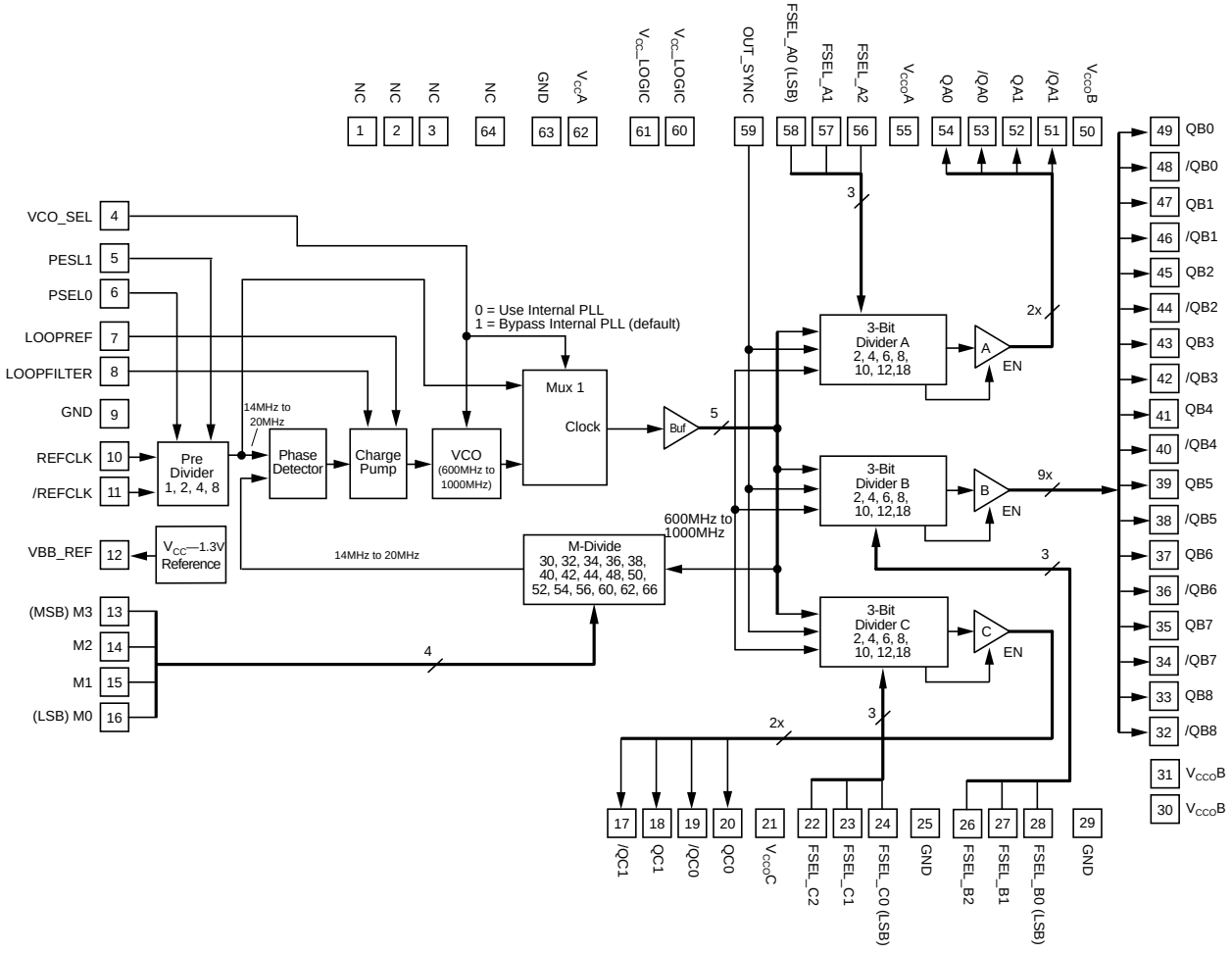
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89534LHC	H64-1	Commercial	SY89534LHC	Sn-Pb
SY89534LHCTR[2]	H64-1	Commercial	SY89534LHC	Sn-Pb
SY89535LHC	H64-1	Commercial	SY89535LHC	Sn-Pb
SY89535LHCTR[2]	H64-1	Commercial	SY89535LHC	Sn-Pb
SY89534LHH[3]	H64-1	Commercial	SY89534LHC with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89534LHHTR[2, 3]	H64-1	Commercial	SY89534LHC with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89535LHH[3]	H64-1	Commercial	SY89535LHC with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89535LHHTR[2, 3]	H64-1	Commercial	SY89535LHC with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Power

Pin Number	Pin Name	Functional Description
60, 61	V_{CC_Logic}	Power for Core Logic: Connect to 3.3V supply. 3.3V power pins are not internally connected on the die, and must be connected together on the PCB.
62	V_{CCA}	Power for PLL: Connect to "quiet" 3.3V supply. 3.3V power pins are not internally connected on the die, and must be connected together on the PCB.
55 30, 31, 50 21	V_{CCO}A V_{CCO}B V_{CCO}C	Power for Output Drivers: Connect all V_{CCO} pins to 3.3V supply. V_{CCO} pins are not connected internally on the die.
4, 9, 25, 63, 29 (exposed pad)	GND	Ground. All GND pins must be tied together on the PCB. Exposed pad must be soldered to a ground plane.

Configuration

Pin Number	Pin Name	Functional Description
4	VCO_SEL	LVTTL/CMOS Compatible Input: Selects between internal or external VCO. When tied LOW (GND) internal VCO is selected. For external VCO, leave floating (default condition is logic HIGH). Internal 25kΩ pull-up.
5, 6	PSEL(1:0)	LVTTL/CMOS Compatible Input: Controls input frequency pre divider. Internal 25kΩ pull-up. Default is logic HIGH. See *"Pre-Divide Frequency Select"* table.
7	LOOP REF	Analog Input/Output: Provides the reference voltage for PLL loop filter.
8	LOOP FILTER	Analog Input/Output: Provides the loop filter for PLL. See *"External Loop Filter Considerations"* for loop filter values.
13,14,15,16	M (3:0)	LVTTL/CMOS Compatible Input: Used to change the PLL (Phase-Lock Loop) feedback divider. Internal 25kΩ pull-up. (M0 = LSB). Default is logic HIGH. See *"Feedback Divide Select"* table.
22, 23, 24	FSEL_C (2:0)	LVTTL/CMOS Compatible Input: Bank C post divide select. Internal 25kΩ pull-up. Default is logic HIGH. See *"Post-Divide Frequency Select"* table.
26, 27, 28	FSEL_B (2:0)	LVTTL/CMOS Compatible Input: Bank B post divide select. Internal 25kΩ pull-up. Default is logic HIGH. See *"Post-Divide Frequency Select"* table.
56, 57, 58	FSEL_A (2:0)	LVTTL/CMOS Compatible Input: Bank A post divide select. Internal 25kΩ pull-up. Default is logic HIGH. See *"Post-Divide Frequency Select."* FSEL_A0 = LSB.
59	OUT_SYNC	Banks A,B,C output synchronous control: (LVTTL/CMOS compatible). Internal 25kΩ pull-up. After any bank has been programmed, toggle with a HIGH-LOW-HIGH pulse to resynchronize all output banks.

Input/Output

Pin Number	Pin Name	Functional Description
1, 2, 3	NC	No Connect: Leave floating.
10, 11	REFCLK, /REFCLK	Reference Input: This flexible input accepts any input TTL/CMOS, LVPECL, LVDS, HSTL, SSTL. See *"Input Interface"* section.
12	VBB_REF	Reference Output Voltage. Used for single-ended input. Maximum sink/source current = 0.5mA.
51, 52, 53, 54	QA1 to QA0	Bank A 100k LVPECL Output Drivers: Output frequency is controlled by FSEL_A (0:2). Terminate outputs with 50Ω to V_{CC} –2V. See *"Output Termination Recommendations"* section for termination detail.
32–49	QB8 to QB0	Bank B Output Drivers: SY89534: 100k LVPECL output drivers. SY89535: Differential LVDS outputs. See *"Output Termination Recommendations"* section for termination detail. Output frequency is controlled by FSEL_B (0:2).
17, 18, 19, 20	QC1 to QC0	Bank C 100k LVPECL Output Drivers: Output frequency is controlled by FSEL_C (0:2). Terminate outputs with 50Ω to V_{CC}–2V. See *"Output Termination Recommendations"* section.
64	NC	No Connect: Leave floating.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
All V_{CC}	V_{CC} Pin Potential to Ground Pin	–0.5 to +4.0	V
V_{IN}	Input Voltage	–0.5 to V_{CCI}	V
I_{OUT}	DC Output Current –LVPECL outputs –LVDS outputs	–50 ±10	mA mA
T_{LEAD}	Lead Temperature (soldering, 20sec.)	260	°C
T_{store}	Storage Temperature	–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient) With Die attach soldered to GND: –Still-Air (TQFP) –200lfpm (TQFP) –500lfpm (TQFP)	 23 18 15	 °C/W °C/W °C/W
	With Die attach NOT soldered to GND:[2] –Still-Air (TQFP) –200lfpm (TQFP) –500lfpm (TQFP)	44 36 30	°C/W °C/W °C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)	4.4	°C/W

DC ELECTRICAL CHARACTERISTICS

Power Supply

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CCA}[3] V_{CC_LOGIC}	PLL and Logic Supply Voltage	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{CCO}A/C	Bank A and C V_{CC} Output	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{CCO}B	Bank B V_{CC} Output LVPECL/LVDS	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
I_{CC}	Total Supply Current[4] SY89534L PECL SY89535L LVDS	 — —	 — 275	 260 330	 — —	 — 285	 260 330	 — —	 — 300	 260 330	 mA mA

LVCMOS/LVTTL Input Control Logic (All V_{CC} pins = +3.3V ±10%)

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V
I_{IH}	Input HIGH Current	—	—	—	—	—	150	—	—	—	µA
I_{IL}	Input LOW Current	—	—	—	–300	—	—	—	—	—	µA

NOTES:

1. permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. It is recommended that the user always solder the exposed die pad to a ground plane for enhanced heat dissipation.
3. V_{CCA}, V_{CC_LOGIC}, V_{CCO}A/C. V_{CCO}B are *not* internally connected together inside the device. They must be connected together on the PCB.
4. No load. Outputs floating, Banks A, B, and C enabled.

DC ELECTRICAL CHARACTERISTICS

REFCLK (pins 10, 11) INPUT (All V_{CC} pins = +3.3V ±10%)

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{ID}	Differential Input Voltage	100[5] 200[6]	— —	— —	100[5] 200[6]	— —	— —	100[5] 200[6]	— —	— —	mV mV
V_{IH}	Input HIGH Voltage	—	—	V_{CC} +0.3	—	—	V_{CC} +0.3	—	—	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage	–0.3	—	—	–0.3	—	—	–0.3	—	—	V

100K LVPECL Outputs (All V_{CC} pins = +3.3V ±10%)

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage[7]	V_{CC}–1.075	—	V_{CC}–0.830	V_{CC}–1.075	—	V_{CC}–0.830	V_{CC}–1.075	—	V_{CC}–0.830	V
V_{OL}	Output LOW Voltage[7]	V_{CC}–1.860	—	V_{CC}–1.570	V_{CC}–1.860	—	V_{CC}–1.570	V_{CC}–1.860	—	V_{CC} –1.570	V
V_{ID}	Differential Input Voltage[8]	100[3] 200[4]	— —	— —	100[3] 200[4]	— —	— —	100[3] 200[4]	— —	— —	mV mV
V_{IH}	Input HIGH Voltage[8]	—	—	V_{CC} +0.3	—	—	V_{CC} +0.3	—	—	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage[8]	–0.3	—	—	–0.3	—	—	–0.3	—	—	V
I_{IH}	Input HIGH Current	–600	—	–300	–600	—	–300	–600	—	–300	µA
I_{IL}	Input LOW Current	–1200	—	–700	–1200	—	–700	–1200	—	–700	µA
V_{BB}	Output Reference Voltage	V_{CC}–1.26	V_{CC}–1.32	V_{CC}–1.38	V_{CC}–1.26	V_{CC}–1.32	V_{CC}–1.38	V_{CC}–1.26	V_{CC}–1.32	V_{CC}–1.38	V

LVDS Outputs (SY89535L) Bank B QB0:8[9] (All V_{CC} pins = +3.3V ±10%)

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OD}	Output Voltage Swing[9, 10]	250	—	450	250	—	450	250	—	450	mV
V_{OH}	Output HIGH Voltage	—	—	1.475	—	—	1.475	—	—	1.475	V
V_{OL}	Output LOW Voltage	0.925	—	—	0.925	—	—	0.925	—	—	V
V_{OCM}	Output Common Mode Voltage[9]	1.125	—	1.375	1.125	—	1.375	1.125	—	1.375	V
ΔV_{OCM}	Change in Common Mode Voltage[9]	–50	—	50	–50	—	50	–50	—	50	mV

NOTES:

5. V_{IN} < 2.4V
6. V_{IN} < V_{CC} +0.3V
7. 50Ω to V_{CC} –2V. Banks A, B, and C enabled.
8. V_{CC} = 3.0V to 3.6V.
9. 100Ω termination across differential pair.
10. 

AC ELECTRICAL CHARACTERISTICS

All V_{CC} pins = +3.3V ±10%

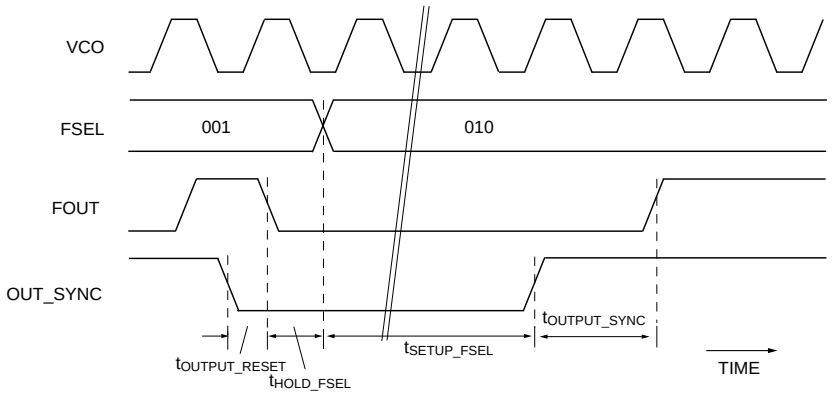
Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{IN}	Reference Input Frequency	—	—	—	14	—	160	—	—	—	MHz
f_{OUT}	Output Frequency Range	—	—	—	33.33	—	500	—	—	—	MHz
t_{VCO}	Internal VCO Frequency Range	600	—	1000	600	—	1000	600	—	1000	MHz
t_{skew}	Within Device(11) Within Bank	—	25	50	—	0	50	—	0	50	ps
	Bank-to-Bank	—	60	150	—	60	150	—	60	150	ps
	Part-to-Part Skew(12)	—	—	—	—	—	200	—	—	200	ps
t_{LOCK}	Maximum PLL Lock Time	—	—	—	—	—	10	—	—	10	ms
t_{JITTER}	Cycle-to-Cycle Jitter(13) (Pk-to-Pk)	—	—	—	—	—	50	—	—	—	ps
	Period Jitter(14) (rms)	—	—	50	—	—	50	—	—	50	ps
t_{pw} (min)	Minimum Pulse Width	—	—	—	50	—	—	50	—	—	ns
	Target PLL Loop Bandwidth										
	Feedback Divider Ratio: 66(15)	—	1.0	—	—	1.0	—	—	1.0	—	MHz
	Feedback Divider Ratio: 30(15)	—	2.0	—	—	2.0	—	—	2.0	—	MHz
t_{DC}	f_{OUT} Duty Cycle	—	—	—	45	50	55	45	50	55	%
t_r, t_f	Output Rise/Fall Time										ps
	(20% to 80%) LVPECL_Out	—	—	400	—	250	400	—	—	400	
	(SY89535L) LVDS_Out	—	—	450	—	300	450	—	—	450	
t_{OUTPUT_RESET}(16)		—	—	—	—	—	10	—	—	—	ns
t_{HOLD_FSEL}(16)		—	—	—	5	—	—	—	—	—	ns
t_{SETUP_FSEL}(16)		—	—	—	5	—	—	—	—	—	ns
t_{OUTPUT_SYNC}(16)		—	—	—	1	—	—	—	—	—	VCO clock cycle
FSEL-to-Valid Output Transition Time		—	—	—	—	50	—	—	—	—	ns

NOTES:

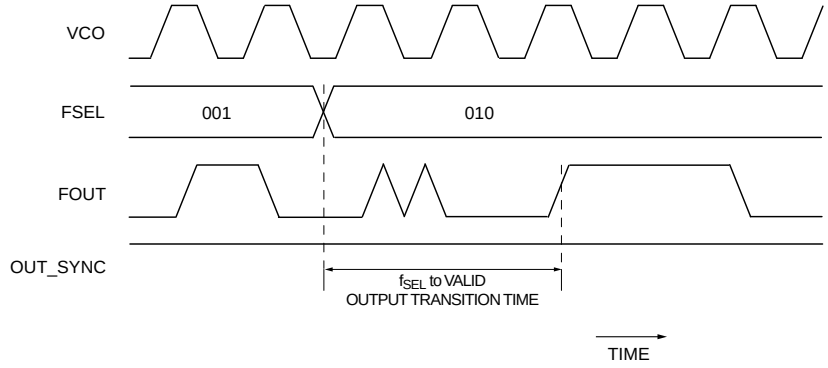
11. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
12. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.
13. Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n - T_{n+1}$ where T is the time between rising edges of the output signal.
14. Period Jitter definition: For a specified amount of time (i.e., 1ms), there are N periods of a signal, and T_n is defined as the average period of that signal. Period jitter is defined as the variation in the period of the output signal for corresponding edges relative to T_n. Parameter guaranteed by design and characterization.
15. Using recommended loop filter components.
16. See *"Timing Diagrams."*

TIMING DIAGRAMS

(Conditions: Internal VCO, unless otherwise stated.)



Frequency Programming



Output Frequency Updates to Valid Output

FUNCTIONAL DESCRIPTION

At the core of the SY89534/35L clock synthesizer is a precision PLL driven by a differential or single-ended reference input. For users who wish to supply a crystal input, please use the SY89532L or SY89533L. The PLL output is sent to three banks of outputs. Each bank has its own programmable frequency divider, and the design is optimized to provide very low skew between banks, and very low jitter.

PLL Programming and Operation

The internal VCO range is 600MHz to 1000MHz, and the feedback ratio is selectable via the MSEL divider control (M3:0 pins). The feedback ratio can be changed without powering the chip down. The PLL output is fed to three banks of outputs: Bank A, Bank B, and Bank C. Banks A and C each have two differential LVPECL output pairs. Bank B has nine differential output pairs. On the SY89534L, Bank B is LVPECL. On the SY89535L, Bank B is LVDS.

Each bank has a separate frequency divider circuit that can be reprogrammed on the fly. The FSEL_x0:2 (where x is A, B, or C) pins control the divider value. The FSEL divider can be programmed in ratios from 2 to 18, and the outputs of Banks A, B, and C can be synchronized after programming by pulsing the OUT_SYNC pin HIGH-LOW-HIGH.

To determine the correct settings for SY89534/35L follow these steps:

1. Refer to the *"Suggested Selections for Specific Customer Applications"* section for common applications, as well as the formula used to compute the output frequency.

2. Determine the desired output frequency, such as 66MHz.

3. Choose a reference input frequency between 14MHz and 20MHz. The user can also choose a higher input frequency, and use the PSEL pre-divider to divide it down to the 14MHz to 20MHz range. In this example, we choose 18MHz for the reference input frequency. This results in an input/output ratio of 66/18.

4. Refer to the *"Feedback Divide Select Table"* and the *"Post-Divide Frequency Select Table"* to find values for MSEL and FSEL such that MSEL/FSEL equals the same 66/18 ratio. In this example, values of MSEL=44 and FSEL=12 work.

5. Make sure that REFCLK ÷ PSEL × MSEL is between 600MHz and 1000MHz.

The user may need to experiment with different REFCLK input frequencies to satisfy these requirements.

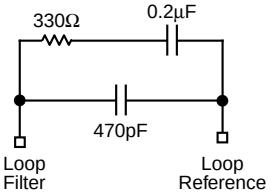


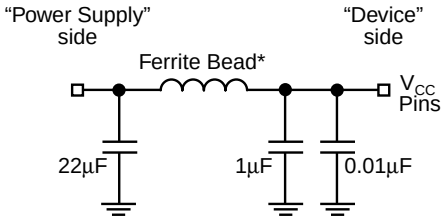
Figure 1. External Loop Filter Connection

External Loop Filter Considerations

The SY89534/35L features an external PLL loop filter that allows the user to tailor the PLL's behavior to their application and operating environment. We recommend using ceramic capacitors with NPO or X7R dielectric, as they have very low effective series resistance. For applications that require ultra-low cycle-to-cycle jitter, use the components shown in Figure 1. The PLL loop bandwidth is a function of feedback divider ratio, and the external loop filter allows the user to compensate. For instance, the PLL's loop bandwidth can be decreased by using a smaller resistor in the loop filter. This results in less noise from the PLL input, but potentially more noise from the VCO. Refer to *"AC Electrical Characteristics"* for target PLL loop bandwidth. The designer should take care to keep the loop filter components on the same side of the board and as close as possible to the SY89534/35L's LOOP_REF and LOOP_FILTER pins. To insure minimal noise pick-up on the loop filter, it is desirable to cut away the ground plane directly underneath the loop filter component pads and traces. However, the benefit may not be significant in all applications and one must be careful to not alter the characteristic impedance of nearby traces.

Power Supply Filtering Techniques

As with any high-speed integrated circuit, power supply filtering is very important. At a minimum, V_{CC}A, V_{CC}_Logic, and all V_{CCO} pins should be individually connected using a via to the power supply plane, and separate bypass capacitors should be used for each pin. To achieve optimal jitter performance, each power supply pin should use separate instances of the circuit shown in Figure 2.



*For V_{CC}_Analog, V_{CC_TTL}, V_{CC1}, use ferrite bead = 200mA, 0.45Ω DC, Murata P/N BLM21A1025

*For V_{CC_OUT} use ferrite bead = 3A, 0.025Ω DC, Murata, P/N BLM31P005

*Component size: 0805

Figure 2. Power Supply Filtering

Output Logic Characteristics

See *"Output Termination Recommendations"* for illustrations. In cases where single-ended output is desired, the designer should terminate the unused complimentary output in the same manner as the normal output that is being used. Unused LVPECL output pairs can be left floating. Unused LVDS output pairs should be terminated w/100Ω across the pair.

LVPECL operation:

- Typical voltage swing is $700mV_{PP}$ to $800mV_{PP}$ into 50Ω.
- Common mode voltage is V_{CC}–1.3V, typical.
- 100Ω termination across the output pair is NOT recommended for LVPECL. See *"Output Termination"* section, Figures 3 to 5.

LVDS operation (SY89535L, Bank B)

- Typical voltage swing is $250mV_{PP}$ to $450mV_{PP}$ into effective 50Ω.
- Common mode voltage is 1.25V, typical.
- 100Ω termination across differential output pair is fine.

Thermal Considerations

This part has an exposed die pad for enhanced heat dissipation. We strongly recommend soldering the exposed die pad to a ground plane. Where this is not possible, we recommend maintaining at least 500lfpm air flow around the part.

REFCLK Input Interface

The flexible REFCLK inputs are designed to accept any differential to single-ended input signal within 300mV above V_{CC} and 300mV below ground.

Do not leave unused REFCLK inputs floating. Tie either the true or complement inputs to ground, but not both. A logic zero is achieved by connecting the complement input to ground with the true input floating. For a TTL input, tie a 2.5kΩ resistor between the complement input and ground. See "Input Interface" section, Figures 4a through 4j.

Input Levels

LVDS, CML and HSTL differential signals may be connected directly to the REFCLK inputs. Depending on the actual worst case voltage seen, the minimum input voltage swing varies as illustrated in the following table:

Input Voltage Range	Minimum Voltage Swing
0 to 2.4V	100mV
0 to V_{CC} +0.3	200mV

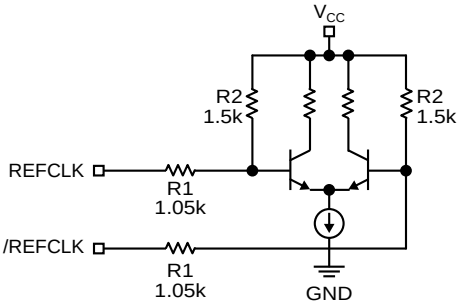


Figure 3. Simplified Input Structure

PRE-DIVIDE FREQUENCY SELECT TABLE (PSEL)

PSEL1 (MSB)	PSEL0	Reference Input Frequency
0	0	REFCLK ÷ 8
0	1	REFCLK ÷ 4
1	0	REFCLK ÷ 2
1	1	REFCLK ÷ 1

POST-DIVIDE FREQUENCY SELECT TABLE (FSEL)

FSEL_A2[1] (MSB)	FSEL_A1[1]	FSEL_A0[1] (LSB)	Output Divider
0	0	0	TDB
0	0	1	VCO ÷ 2
0	1	0	VCO ÷ 4
0	1	1	VCO ÷ 6
1	0	0	VCO ÷ 8
1	0	1	VCO ÷ 10
1	1	0	VCO ÷ 12
1	1	1	VCO ÷ 18

NOTES:

1. Same dividers apply to FSEL_B (0:2) and FSEL_C (0:2).

FEEDBACK DIVIDE SELECT TABLE (MSEL)

M3	M2	M1	M0	VCO Frequency(1)
0	0	0	0	REFCLK ÷ PSEL × 34
0	0	0	1	REFCLK ÷ PSEL × 36
0	0	1	0	REFCLK ÷ PSEL × 38
0	0	1	1	REFCLK ÷ PSEL × 40
0	1	0	0	REFCLK ÷ PSEL × 42
0	1	0	1	REFCLK ÷ PSEL × 44
0	1	1	0	REFCLK ÷ PSEL × 48
0	1	1	1	REFCLK ÷ PSEL × 50
1	0	0	0	REFCLK ÷ PSEL × 52
1	0	0	1	REFCLK ÷ PSEL × 54
1	0	1	0	REFCLK ÷ PSEL × 56
1	0	1	1	REFCLK ÷ PSEL × 60
1	1	0	0	REFCLK ÷ PSEL × 62
1	1	0	1	REFCLK ÷ PSEL × 66
1	1	1	0	REFCLK ÷ PSEL × 30
1	1	1	1	REFCLK ÷ PSEL × 32

SUGGESTED SELECTIONS FOR SPECIFIC CUSTOMER APPLICATIONS

Protocol	Rate (MHz)	FSEL (Post Divider)	MSEL (Feedback Div.)	REFCLK (MHz)	PSEL	FOUT
PCI	33	18	36	16.67	1	33
Fast Ethernet	100	6	40	15	1	100
1/8 FC	133	6	52	15.36	1	133
ESCON	200	4	50	16	1	200

$$FOUT = \frac{(REFCLK \div PSEL \times MSEL)}{FSEL}$$

NOTES:

1. 600MHz < (REFCLK ÷ PSEL × MSEL) < 1000MHz.
2. 14MHz ≤ (REFCLK ÷ PSEL) ≤ 20MHz.
3. Where two settings provide the user with the identical desired frequency, the setting with the higher PLL input reference frequency (and lower feedback divider) will usually have lower output jitter. However, the reference input frequency, as well as the VCO frequency, must be kept within their respective ranges.

INPUT INTERFACE

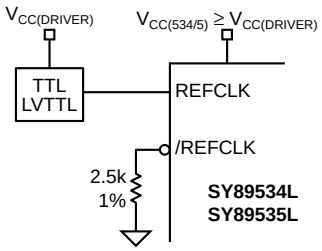


Figure 4a. 5V, 3.3V "TTL"

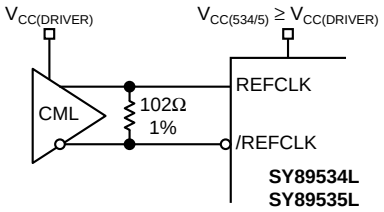


Figure 4b. CML-DC Coupled

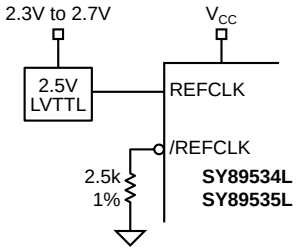


Figure 4c. 2.5V "LVTTL"

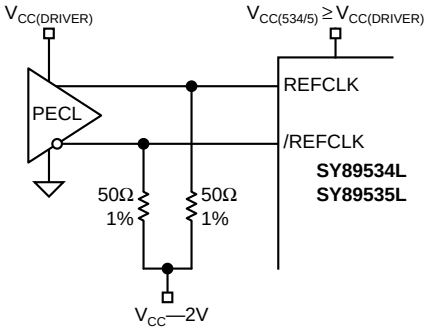


Figure 4d. 3.3V LVPECL-DC Coupled

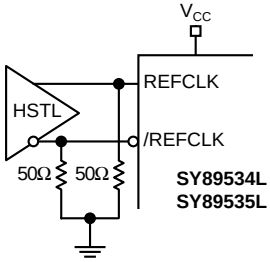


Figure 4e. HSTL

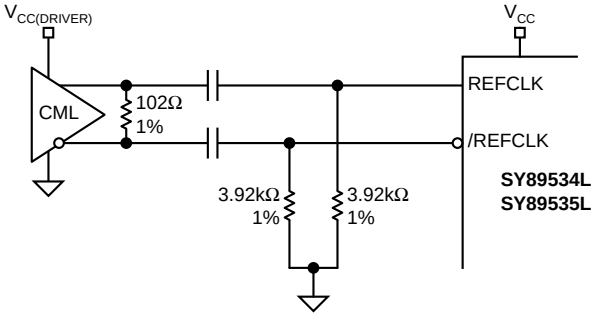


Figure 4f. CML-AC Coupled–Short Trace Lengths

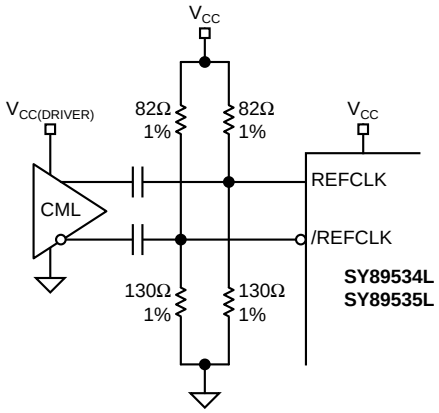


Figure 4g. CML-AC Coupled–Long Trace Lengths

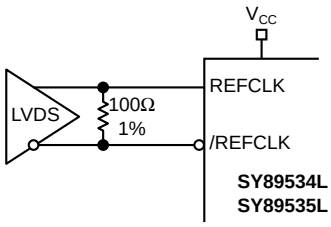


Figure 4h. LVDS

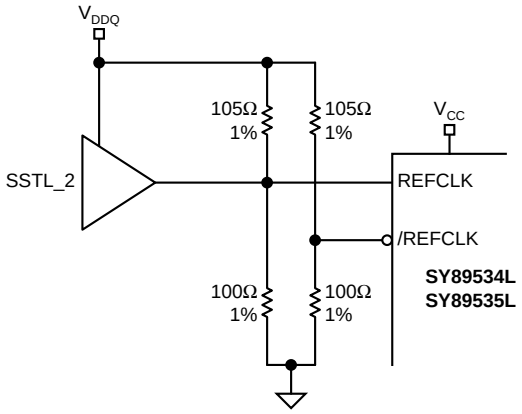


Figure 4i. SSTL_2

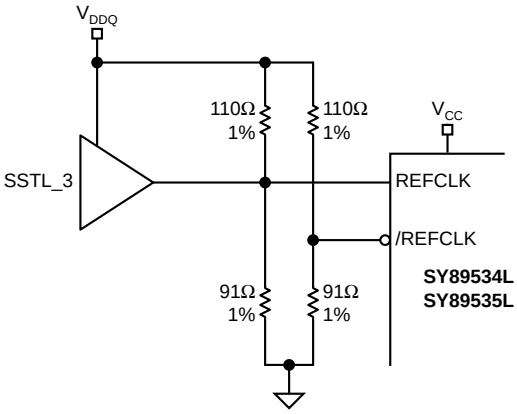


Figure 4j. SSTL_3

OUTPUT TERMINATION RECOMMENDATIONS

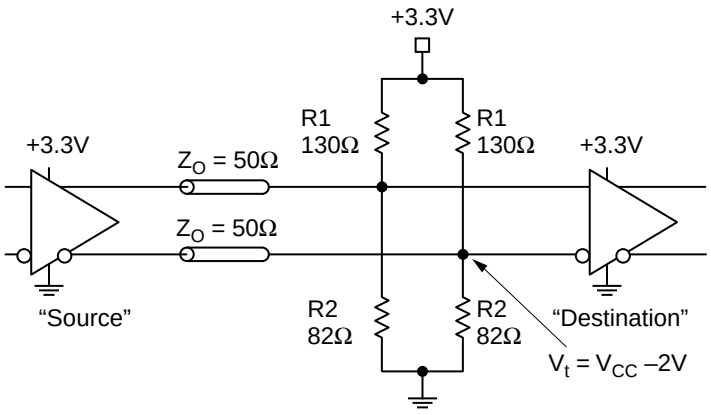


Figure 5. PECL Parallel Termination–Thevenin Equivalent

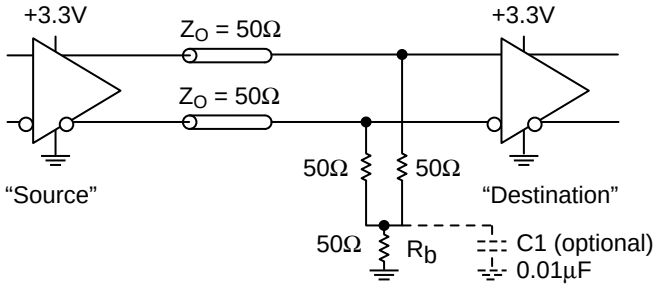


Figure 6. PECL Three-Resistor "Y–Termination"

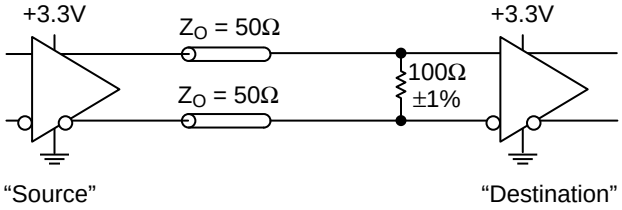
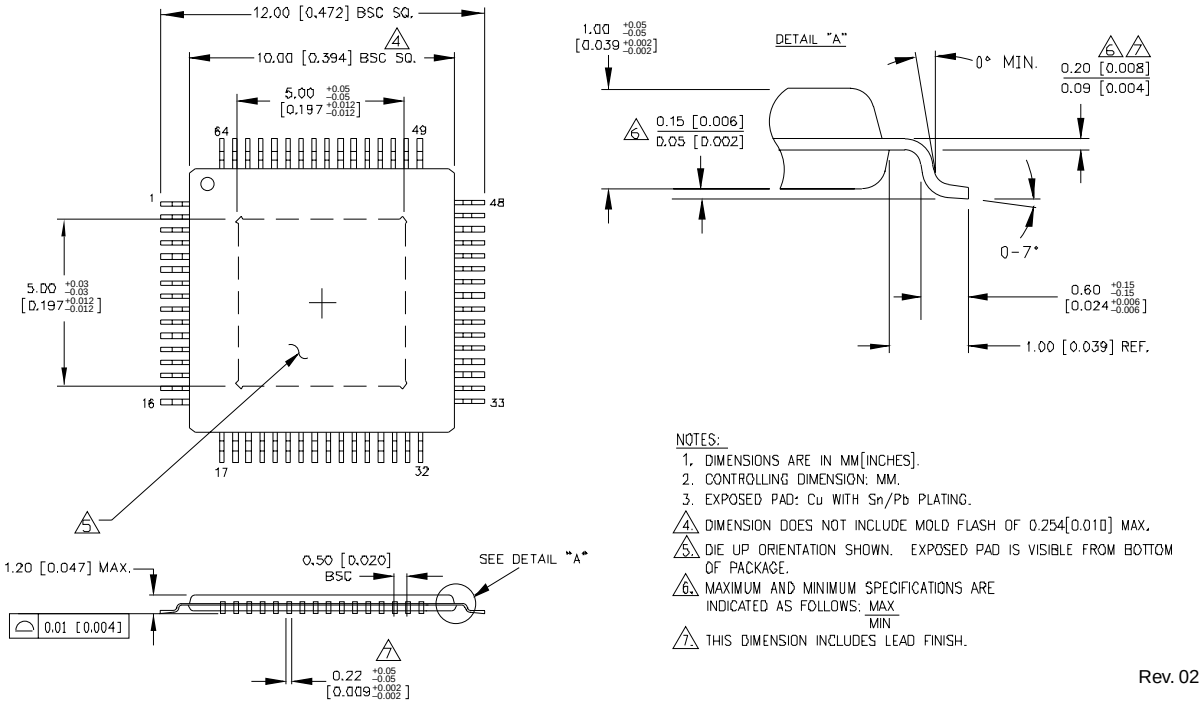


Figure 7. LVDS Differential Termination

NOTES:

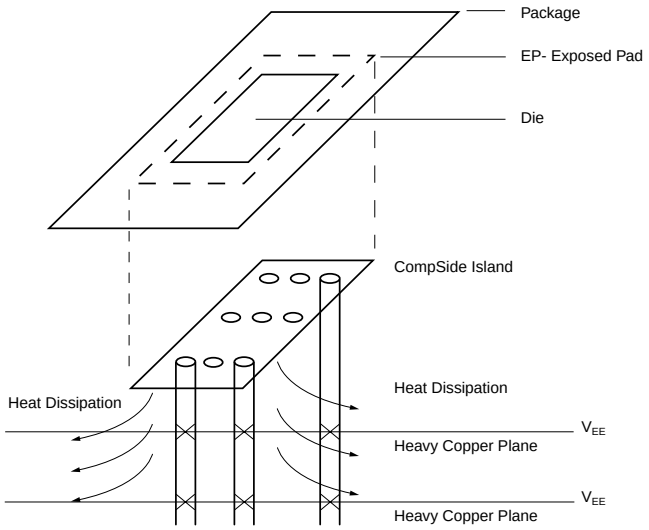
1. PECL Y-termination is a power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω.

64-PIN EPAD-TQFP (DIE UP) (H64-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 02



PCB Thermal Consideration for 64-Pin EPAD-TQFP Package

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