STS8C5H30L

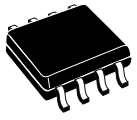
N-CHANNEL 30V - 0.018Ω - 8A SO-8
P-CHANNEL 30V - 0.045Ω - 5A SO-8
LOW GATE CHARGE StripFET™ III MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS8C5H30L (N-Channel)	30 V	< 0.022 Ω	8 A
STS8C5H30L (P-Channel)	30 V	< 0.055 Ω	5 A

- TYPICAL $R_{DS(on)}$ (N-Channel) = 0.018 Ω
- TYPICAL $R_{DS(on)}$ (P-Channel) = 0.045 Ω
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DRIVE
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY

Figure 1: Package

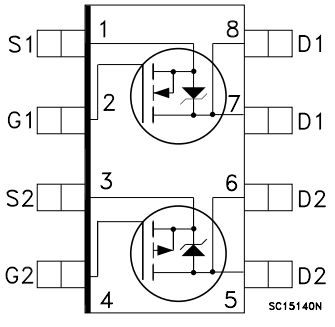


SO-8

DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Figure 2: Internal Schematic Diagram



APPLICATIONS

- DC/DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES
- DC MOTOR DRIVE

Table 2: Order Codes

PART NUMBER	MARKING	PACKAGE	PACKAGING
STS8C5H30L	S8C5H30L	SO-8	TAPE & REEL

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		N-CHANNEL	P-CHANNEL	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30		V
V_{GS}	Gate- source Voltage	± 16	± 16	V
I_D	Drain Current (continuous) at T_C = 25°C Single Operating	8	4.2	A
I_D	Drain Current (continuous) at T_C = 100°C Single Operating	6.4	3.1	A
I_{DM} (•)	Drain Current (pulsed)	32	16.8	A
P_{TOT}	Total Dissipation at T_C = 25°C Dual Operating Total Dissipation at T_C = 25°C Single Operating	1.6 2		W W
T_j T_{stg}	Operating Junction Temperature Storage Temperature	150 -55 to 150		°C °C

(•) Pulse width limited by safe operating area
Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Single Operating Dual Operating	62.5 78	°C/W °C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 5: On/Off

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	n-ch p-ch	30 30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS}= Max Rating V_{DS}= Max Rating, T_C= 125°C	n-ch p-ch			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS}= ± 16V V_{GS}= ± 16V	n-ch p-ch			±100 ±100	nA nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D= 250 µA	n-ch p-ch	1 1	 1.6	 2.5	V V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS}= 10 V, I_D= 4 A V_{GS}= 10 V, I_D= 2.5 A V_{GS}= 4.5 V, I_D= 4 A V_{GS}= 4.5 V, I_D= 2.5 A	n-ch p-ch n-ch p-ch		0.018 0.045 0.020 0.070	0.022 0.055 0.025 0.075	Ω Ω Ω Ω

Table 6: Dynamic

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D= 4 A V_{DS} = 15 V, I_D= 2.5 A	n-ch p-ch		8.5 10		S S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0	n-ch p-ch		857 1350		pF pF
C_{oss}	Output Capacitance		n-ch p-ch		147 490		pF pF
C_{rss}	Reverse Transfer Capacitance		n-ch p-ch		20 130		pF pF

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

ELECTRICAL CHARACTERISTICS(CONTINUED)

Table 7: Switching On

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 15 V, I_D = 4 A,	n-ch		12		ns
t_r	Rise Time	R_G= 4.7 Ω, V_{GS} = 4.5 V	p-ch		25		ns
		P-CHANNEL					
		V_{DD} = 15 V, I_D = 2 A,	n-ch		14.5		ns
		R_G= 4.7 Ω, V_{GS} = 4.5 V	p-ch		35		ns
		(Resistive Load see, Figure 28)					
Q_g	Total Gate Charge	V_{DD}= 24 V, I_D= 8 A,	n-ch		7	10	nC
		V_{GS}= 5 V	p-ch		12.5	16	nC
Q_{gs}	Gate-Source Charge	**P-CHANNEL**	n-ch		2.5		nC
		V_{DD} = 24 V, I_D = 4 A,	p-ch		5		nC
Q_{gd}	Gate-Drain Charge	V_{GS} = 5 V	n-ch		2.3		nC
		(see, Figure 31)	p-ch		3		nC

Table 8: Switching Off

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	V_{DD} = 15 V, I_D = 4 A,	n-ch		23		ns
t_f	Fall Time	R_G= 4.7 Ω, V_{GS} = 4.5 V	p-ch		125		ns
		P-CHANNEL					
		V_{DD} = 15 V, I_D = 2.5 A,	n-ch		8		ns
		R_G= 4.7 Ω, V_{GS} = 4.5 V	p-ch		35		ns
		(Resistive Load see, Figure 28)					

Table 9: Source-Drain Diodef

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current		n-ch			8	A
			p-ch			5	A
I_{SDM} (2)	Source-drain Current (pulsed)		n-ch			32	A
			p-ch			20	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 8 A, V_{GS} = 0	n-ch			1.5	V
		I_{SD} = 5 A, V_{GS} = 0	p-ch			1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 8 A, di/dt = 100 A/µs	n-ch		15		ns
		V_{DD} = 15V, T_j = 150°C	p-ch		45		ns
Q_{rr}	Reverse Recovery Charge		n-ch		5.7		nC
		P-CHANNEL	p-ch		36		nC
I_{RRM}	Reverse Recovery Current	I_{SD} = 5 A, di/dt = 100 A/µs	n-ch		0.76		A
		V_{DD} = 15V, T_j = 150°C	p-ch		1.6		A
		(see test circuit, Figure 29)					

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.
(3) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS

Figure 3: .Safe Operating n-channel

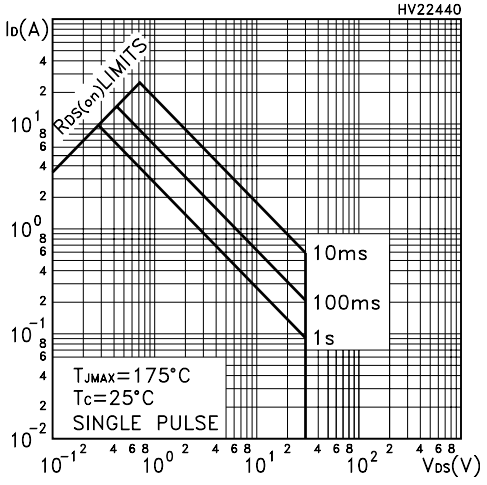


Figure 4: Output Characteristics n-channel

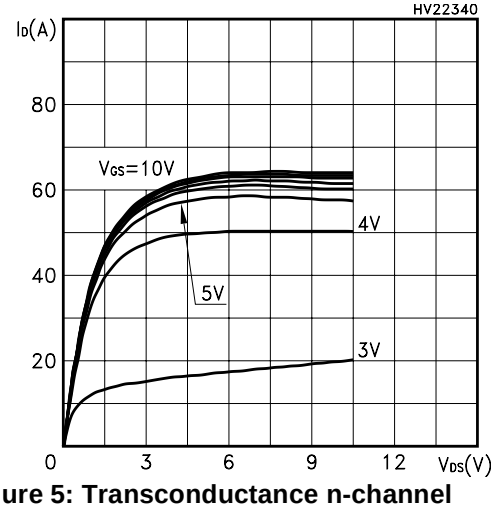


Figure 5: Transconductance n-channel

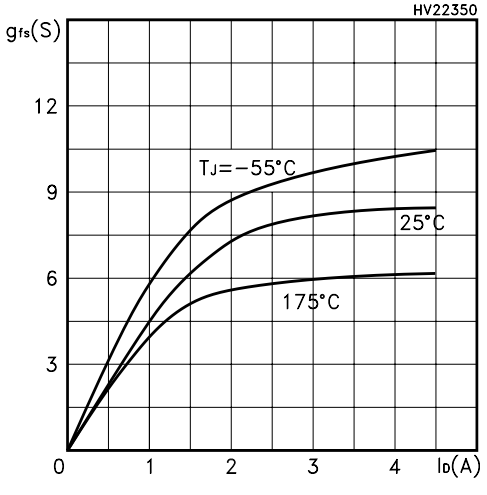


Figure 6: Thermal Impedance For Complementary Pair

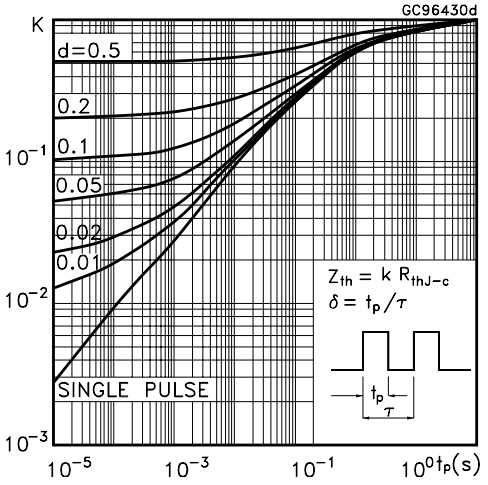


Figure 7: Transfer Characteristics n-channel

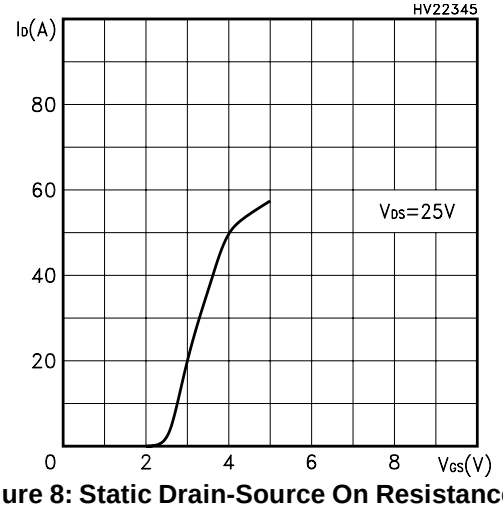


Figure 8: Static Drain-Source On Resistance n-channel

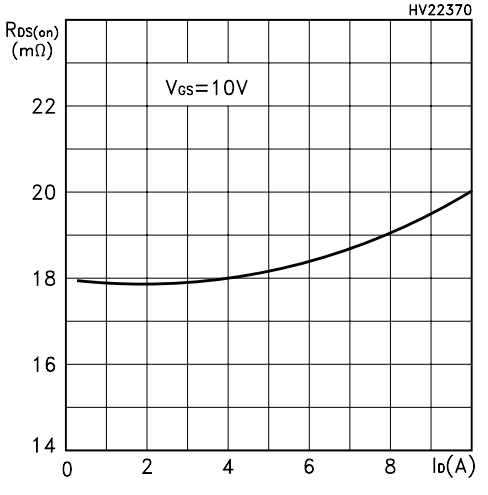


Figure 9: Gate Charge vs Gate-Source Voltage n-channel

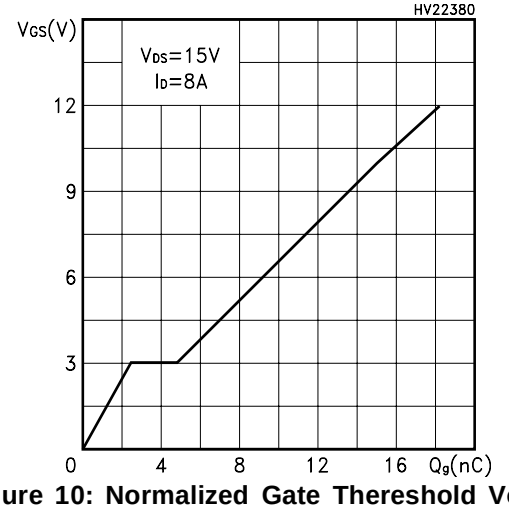


Figure 10: Normalized Gate Thereshold Voltage vs Temperature n-channel

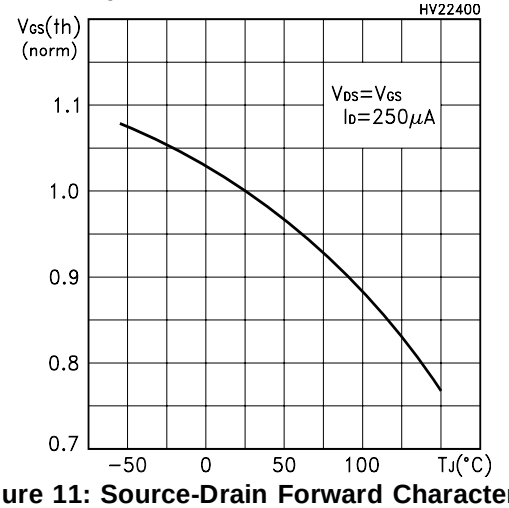


Figure 11: Source-Drain Forward Characteristics n-channel

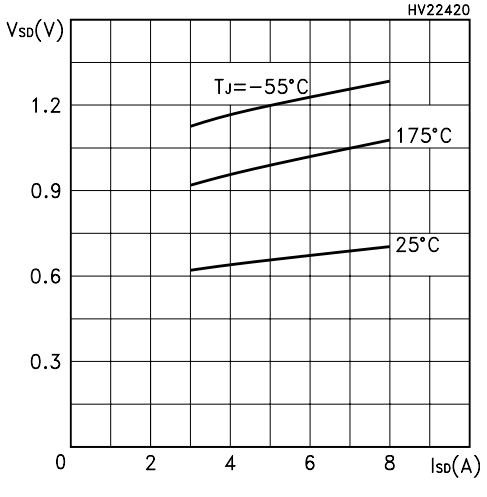


Figure 12: Capacitance Variations n-channel

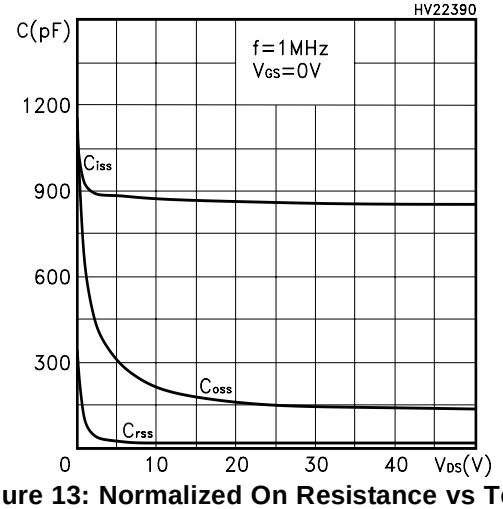


Figure 13: Normalized On Resistance vs Temperature n-channel

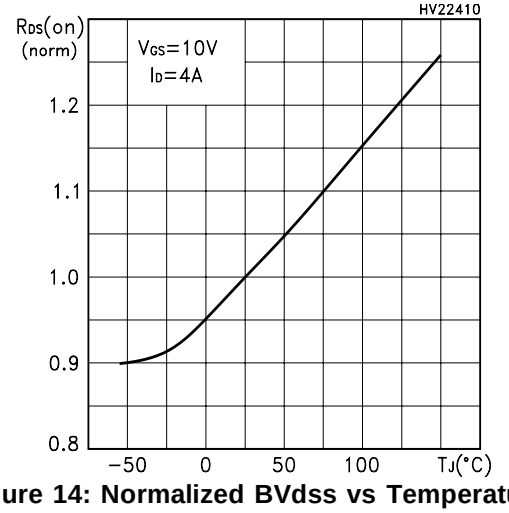


Figure 14: Normalized BVdss vs Temperature n-channel

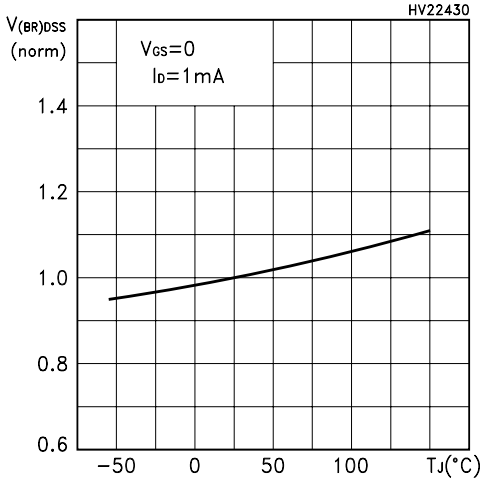


Figure 15: Safe Operating p-channel

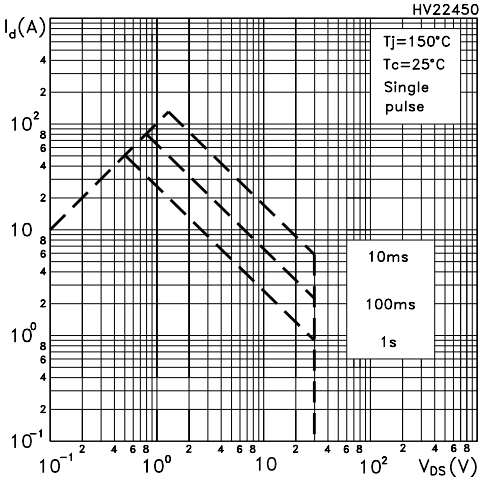


Figure 16: Output Characteristics p-channel

Figure 18: Thermal Impedance for Complementary Pair

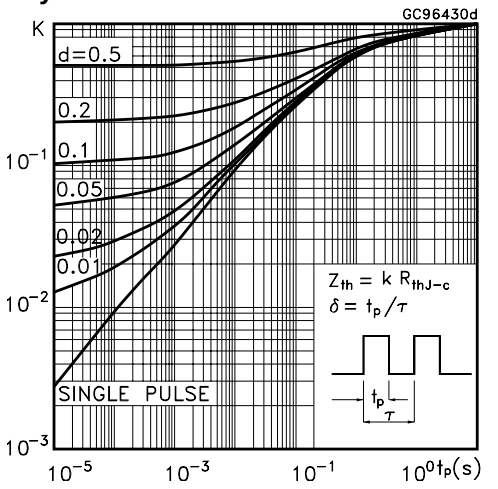


Figure 19: Transfer Characteristics p-channel

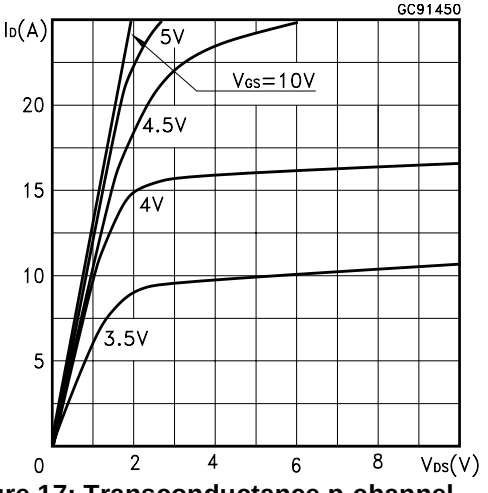


Figure 17: Transconductance p-channel

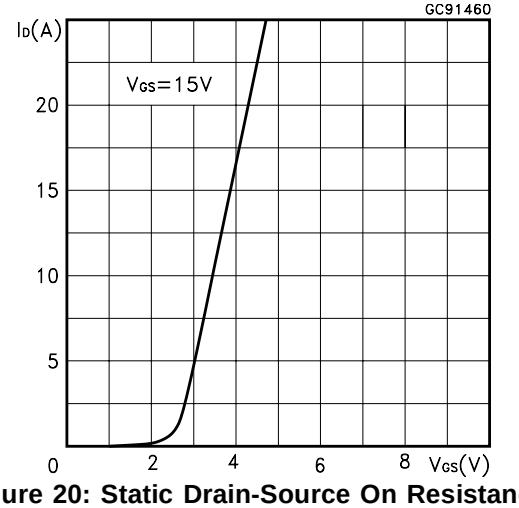
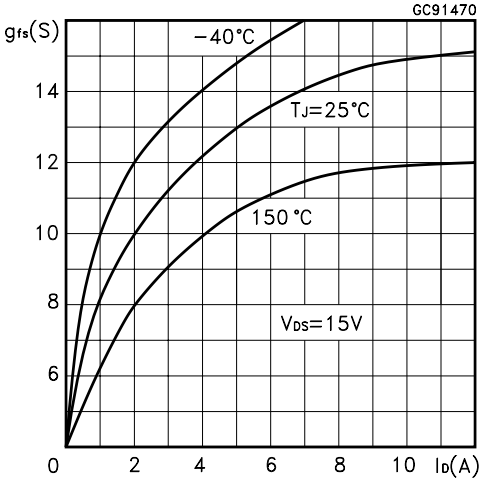


Figure 20: Static Drain-Source On Resistance p-channel



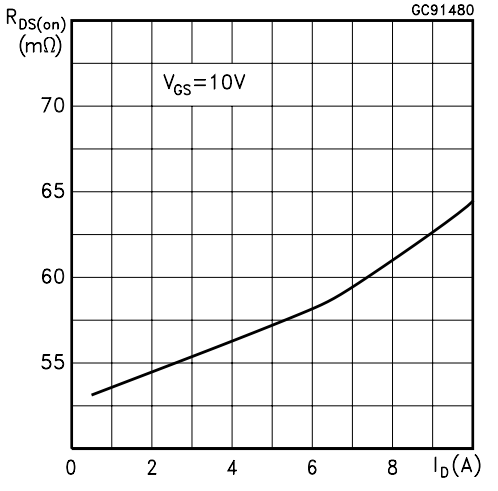


Figure 21: Gate Charge vs Gate-Source Voltage p-channel

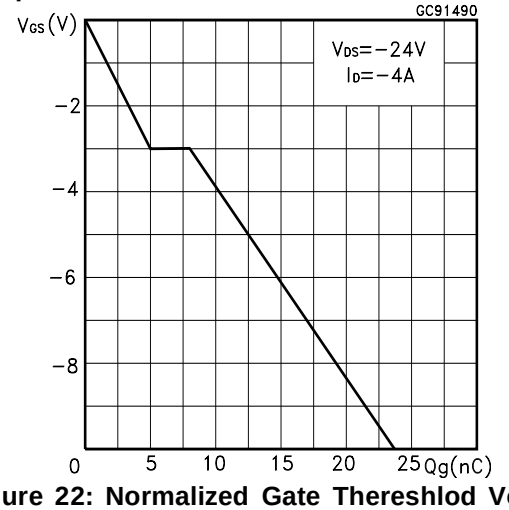


Figure 22: Normalized Gate Thereshlod Voltage vs Temperature p-channel

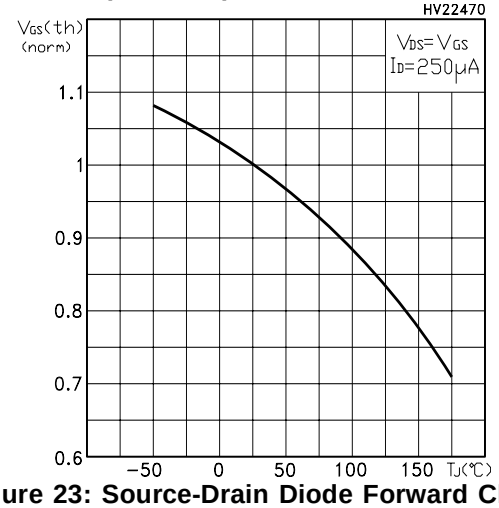


Figure 23: Source-Drain Diode Forward Characteristics p-channel

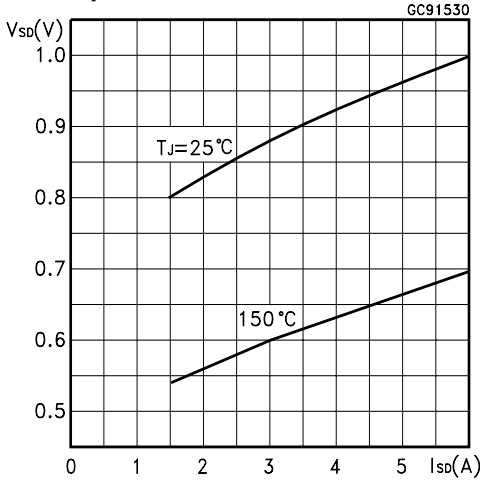


Figure 24: Capacitances Variations p-channel

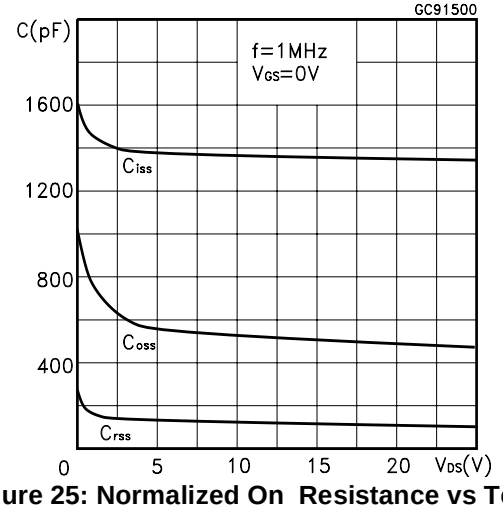


Figure 25: Normalized On Resistance vs Temperature p-channel

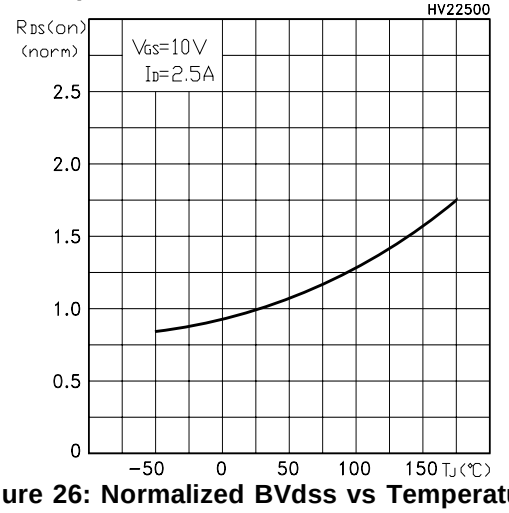


Figure 26: Normalized BVdss vs Temperature p-channel

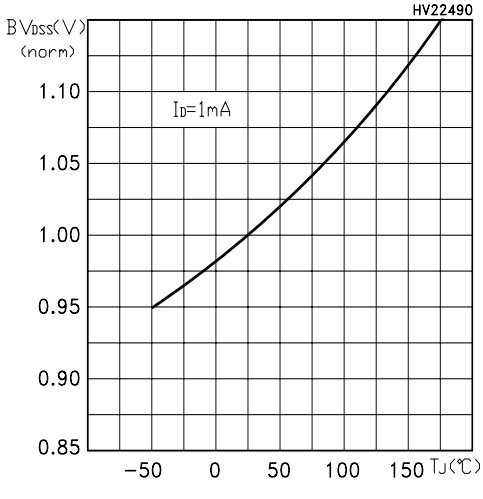


Figure 27: Unclamped Inductive Load Test Circuit

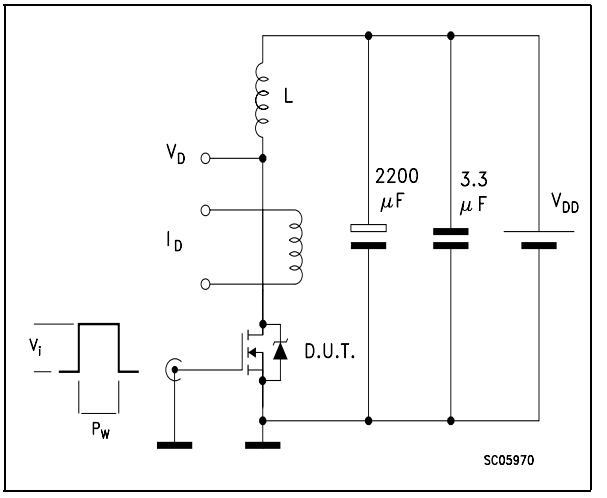


Figure 28: Switching Times Test Circuit For Resistive Load

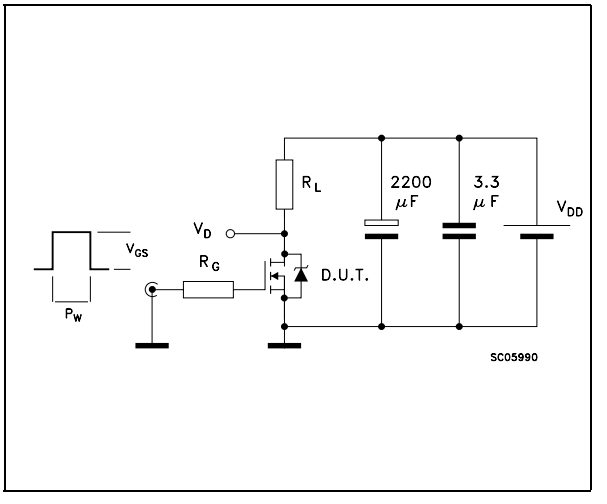


Figure 29: Test Circuit For Inductive Load Switching and Diode Recovery Times

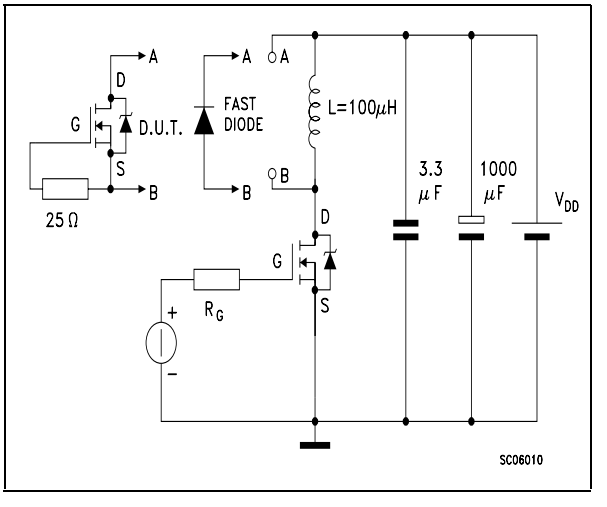


Figure 30: Unclamped Inductive Wafeform

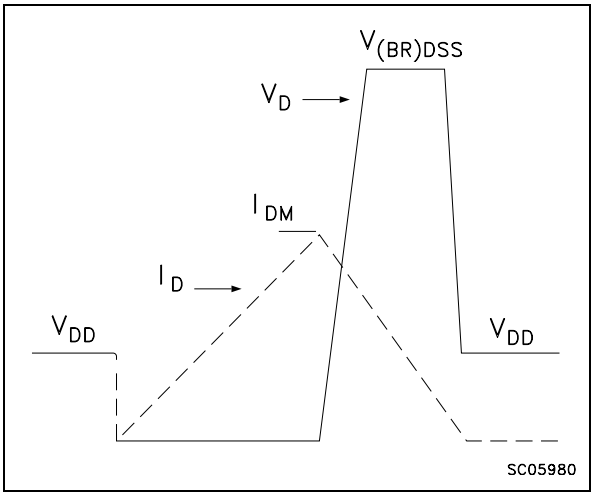
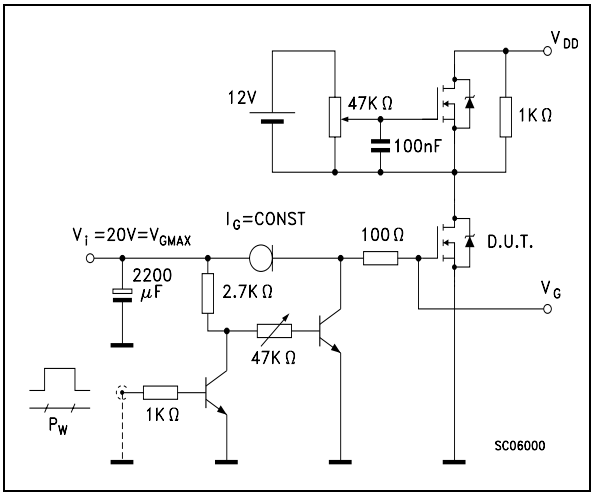


Figure 31: Gate Charge Test Circuit



SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					

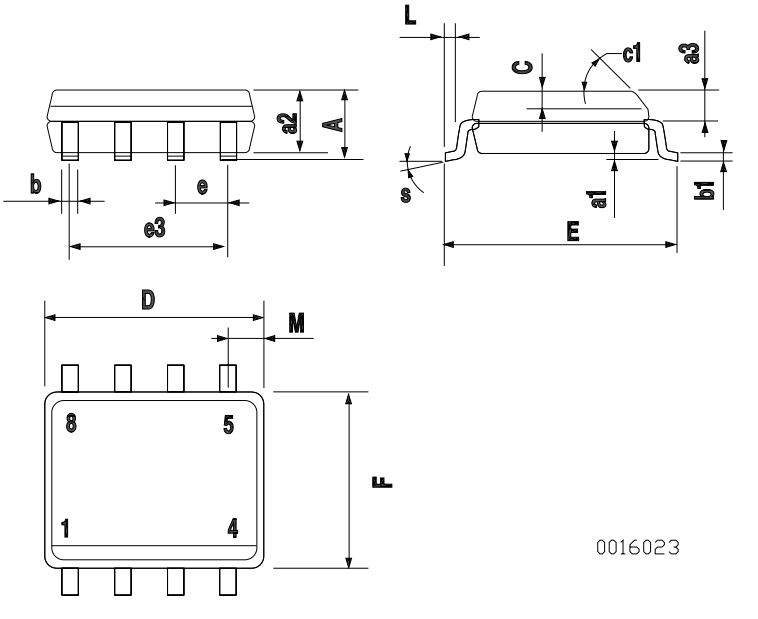


Table 10: Revision History

Date	Revision	Description of Changes
10-Aug-2004	1	First Revision
10-Sep-2004	2	Complete Version