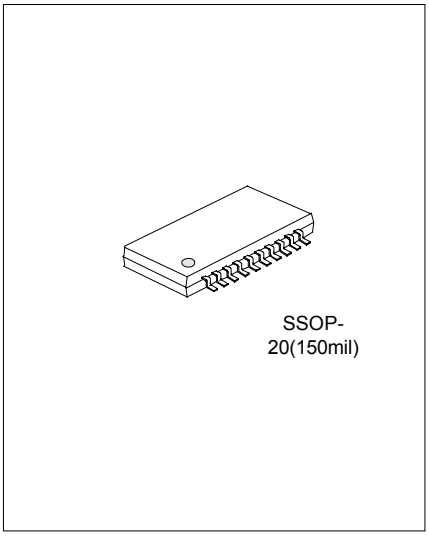
FET BIAS CONTROLLER WITH POLARISATION SWITCH AND TONE DETECTION



DESCRIPTION

The UTC X3211 is designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs, PMR, cellular telephones etc. with a minimum of external components.

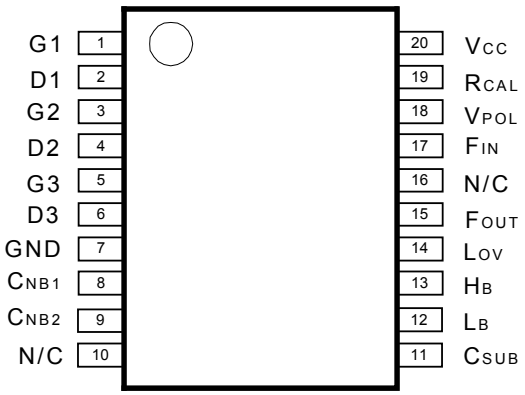
FEATURES

* Provides bias for GaAs and HEMT FETs
* Drives up to three FETs
* Dynamic FET protection
* Drain current set by external resistor
* Polarisation switch for LNBs –supporting zero volt gate switching topology.
* 22kHz tone detection for band switching

APPLICATIONS

*Satellite receiver LNBs
* Private mobile radio (PMR)
* Cellular telephones

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc	-0.6~12	V
Supply Current	I_{CC}	100	mA
Drain Current (per FET) (set by R_{CAL})	I_D	0~15	mA
Input Voltage (V_{POL})	V_{IN}	25 continuous	V
Operating Temperature	Topr	-40~70	°C
Storage Temperature	T_{Stg}	-50~85	°C
Power Disspation(Ta=25°C)	P_D	500	mW

ELECTRICAL CHARACTERISTICS

(Ta = 25 °C,Vcc=5V,I_D=10mA, R_{CAL} =33kΩ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc		5		10	V
Supply Current	I_{CC}	I_{D1} to I_{D3}=0		6	15	mA
		I_{D1} =0, I_{D2} to I_{D3}=10mA,V_{POL}=14V		25	35	mA
		I_{D2}=0, I_{D1} to I_{D3}=10mA,V_{POL}=15.5V		25	35	mA
		I_{D1} to I_{D3}=0,I_{LB}=10mA		16	25	mA
		I_{D1} to I_{D3}=0,I_{HB}=10mA		16	25	mA
Substrate Voltage	V_{SUB}	(Internally generated) I_{SUB} =0	-3.5	-3	-2.5	V
		I_{SUB} = -200μA			-2.4	V
Output Noise						
Drain Voltage	E_{ND}	C_G=4.7nF,C_D=10nF			0.02	Vpkpk
Gate Voltage	E_{NG}	C_G=4.7nF,C_D=10nF			0.005	Vpkpk
Oscillator Freq	f_O		200	350	800	kHz

GATE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Current Range	I_{GO}		-30		2000	μA
Output Voltage						
Gate 1 Off	V_{G1O}	I_{D1}=0mA, V_{POL}=14V, I_{GO1}=0μA	-0.05	0	0.05	V
Low	V_{G1L}	I_{D1}=12mA, V_{POL}=15.5V, I_{GO1}=-10μA	-2.7	-2.4	-2	
High	V_{G1H}	I_{D1}=8mA, V_{POL}=15.5V, I_{GO1}=0μA	0.4	0.75	1.0	
Output Voltage						
Gate 2 Off	V_{G2O}	I_{D2}=0mA, V_{POL}=15.5V, I_{GO2}=0μA	-0.05	0	0.05	V
Low	V_{G2L}	I_{D2}=12mA, V_{POL}=14V, I_{GO2}=-10μA	-2.7	-2.4	-2	
High	V_{G2H}	I_{D2}=8mA, V_{POL}=14V, I_{GO2}=0μA	0.4	0.75	1.0	
Output Voltage						
Gate 3 Low	V_{G3L}	I_{D3}=12mA, I_{GO3}=-10μA	-3.5	-2.9	-2	V
High	V_{G3H}	I_{D3}=8mA, I_{GO3}=0μA	0.4	0.75	1.0	

DRAIN CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current	I_D		8	10	12	mA
Current Change With Vcc With Tj	 ΔI_{DV} ΔI_{DT}	 Vcc=5 to12V Tj= -40 to +70°C		 0.5 0.05		 %/V %/°C
Drain 1 Change : High	V_{D1}	I_{D1} =10mA V_{POL}=15.5V	1.8	2.0	2.2	V
Drain 2 Change : High	V_{D2}	I_{D2} =10mA V_{POL}=14V	1.8	2.0	2.2	V
Drain 3 Change : High	V_{D3}	I_{D3} =10mA	1.8	2.0	2.2	V
Voltage Change With Vcc With Tj	 ΔV_{DV} ΔV_{DT}	 Vcc=5 to10V Tj= -40 to +70°C		 0.5 50		 %/V ppm
Leakage Current Drain 1 Drain 2	 I_{L1} I_{L2}	 V_{D1}=0.5V, V_{POL}=14V V_{D2}=0.5V, V_{POL}=15.5V		 	 10 10	 μA

TONE DETECTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter Amplifier Input Bias Current	 I_B	 R_{F1}=150kΩ	 0.02	 0.07	 0.25	μA
Output Voltage [5]	V_{OUT}	R_{F1}=150kΩ	1.75	1.95	2.05	V
Output Current [5]	I_{OUT}	V_{OUT}=1.96V, V_{FIN}=2.1V	400	520	650	μA
Voltage Gain	G_V	f=22kHz, V_{IN}=1mV		46		dB
Rejection Frequency	f_R	$V_{(AC)IN}$=1V p/p sq.w[6]	1.0	7.5		kHz
V Threshold [5]	FVT		100		350	mV p/p
Output Stage Lov Volt.Range	 V_{LOV}	 I_L=50mA(L_B or H_B)	 -0.5	 	 Vcc-1.8	 V
Lov Bias Current	I_{LOV}	V_{LOV}=0	0.02	0.15	1.0	μA
L_B Output Low	V_{LBL}	V_{LOV}=0, I_L= -10μA, Enable [6] V_{LOV}=3V, I_L=0, Enable [7]	-3.5 -0.01	-2.75 0	-2.5 0.01	V V
L_B Output High	V_{LBH}	V_{LOV}=0, I_L=10 mA, Disable [6] V_{LOV}=3V, I_L=50mA, Disable [7]	-0.025 2.9	0 3.0	0.025 3.1	V V
H_B Output Low	V_{HBL}	V_{LOV}=0, I_L= -10 μ A, Disable [6] V_{LOV}=3V, I_L=0, Disable [7]	-3.5 -0.01	-2.75 0	-2.5 0.01	V V
H_B Output High	V_{HBH}	V_{LOV}=0, I_L=10mA, Enable [6] V_{LOV}=3V, I_L=50mA, Enable [7]	-0.025 2.9	0 3.0	0.025 3.1	V V

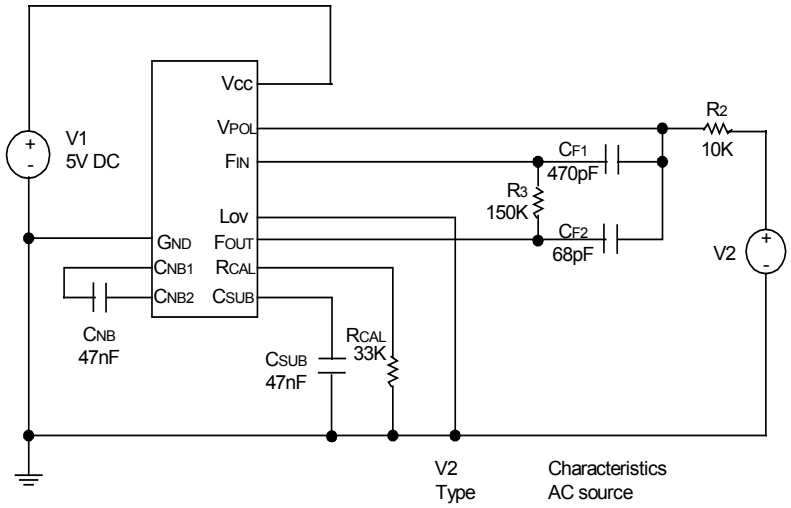
POLY SWITCH CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Current	I_{POL}	V_{POL}=25V (Applied via R_{POL}=10kΩ)	10	20	40	μA
Threshold Voltage	V_{TPOL}	V_{POL}=25V (Applied via R_{POL}=10kΩ)	14	14.75	15.5	V
Switching Speed	T_{SPOL}	V_{POL}=25V (Applied via R_{POL}=10kΩ)			100	ms

NOTES:

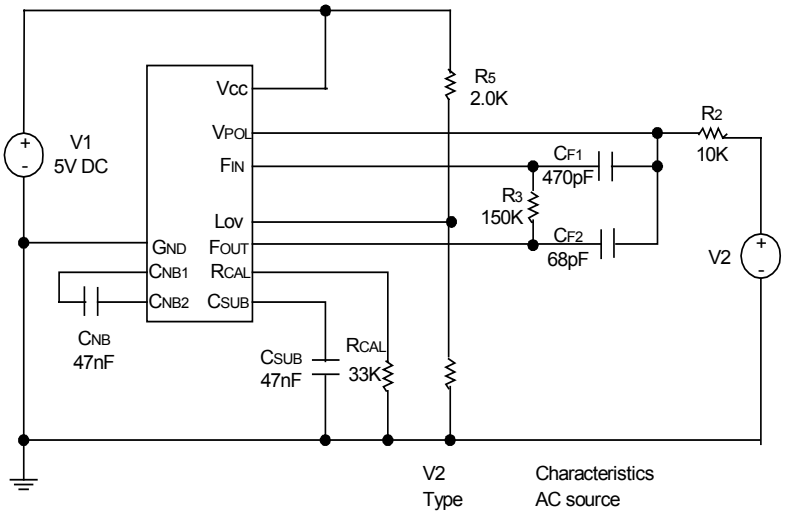
1. The negative bias voltages specified are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB} of 47nFare required for this purpose.
2. The characteristics are measured using an external reference resistors R_{CAL} of value 33kΩ wired from pins R_{CAL} to ground.
3. Noise voltage is not measured in production.
4. Noise voltage measurement is made with FETs and gate drain capacitors in place on all outputs. CG,4.7nF,are connected between gate outputs and ground,C_D,10nF,are connected between drain outputs and ground.
5. These parameters are linearly related to Vcc
6. These parameters are measured using Test Circuit 1
7. These parameters are measured using Test Circuit 2

TEST CIRCUIT 1

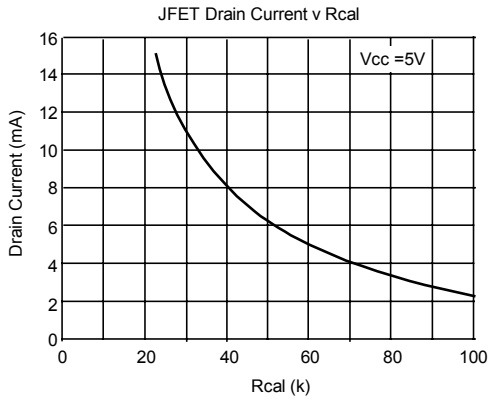


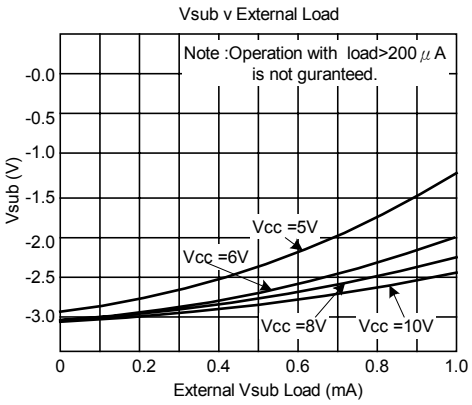
V2	Characteristics
Type	AC source
Frequency	22kHz
Voltage	350mV p/p enabled 100mV p/P disabled

TEST CIRCUIT 2

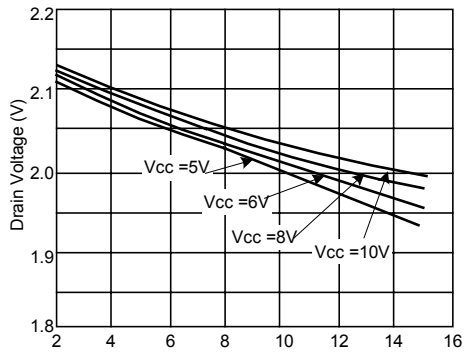


TYPICAL CHARACTERISTICS

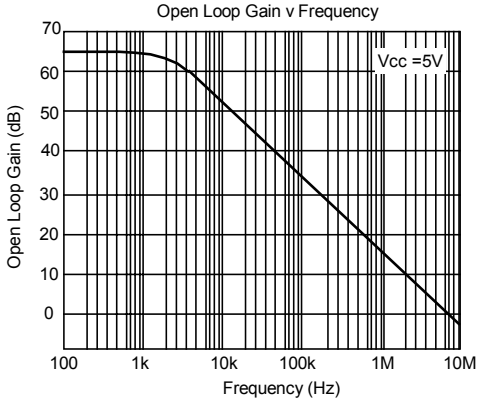




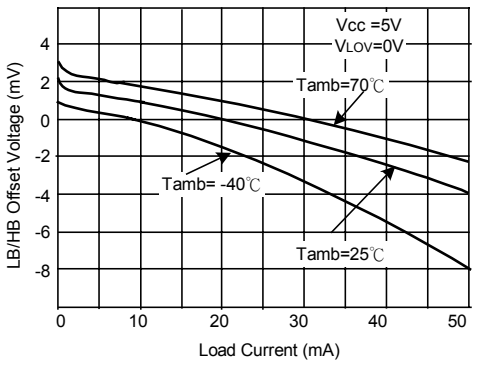
JFET Drain Voltage v Drain Current



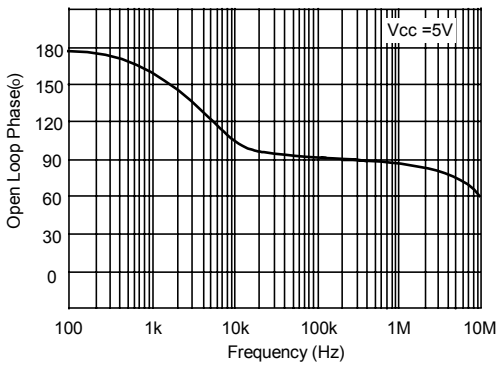
Open Loop Gain v Frequency



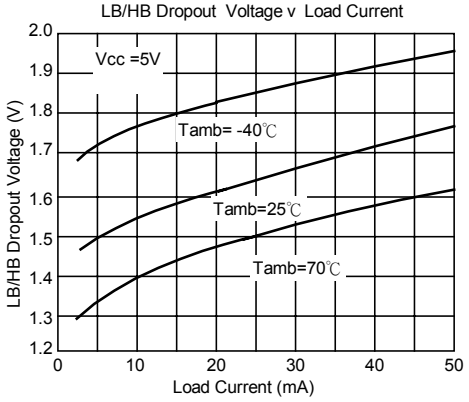
LB/HB Offset Voltage v Load Current



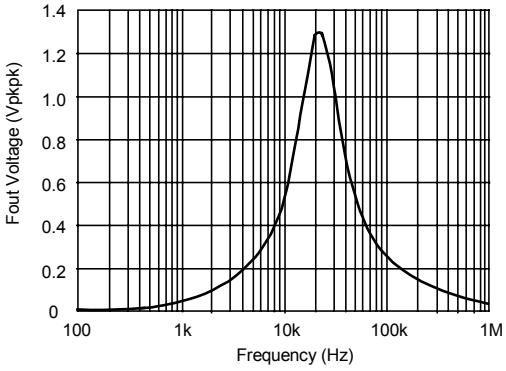
Open Loop Phase v Frequency



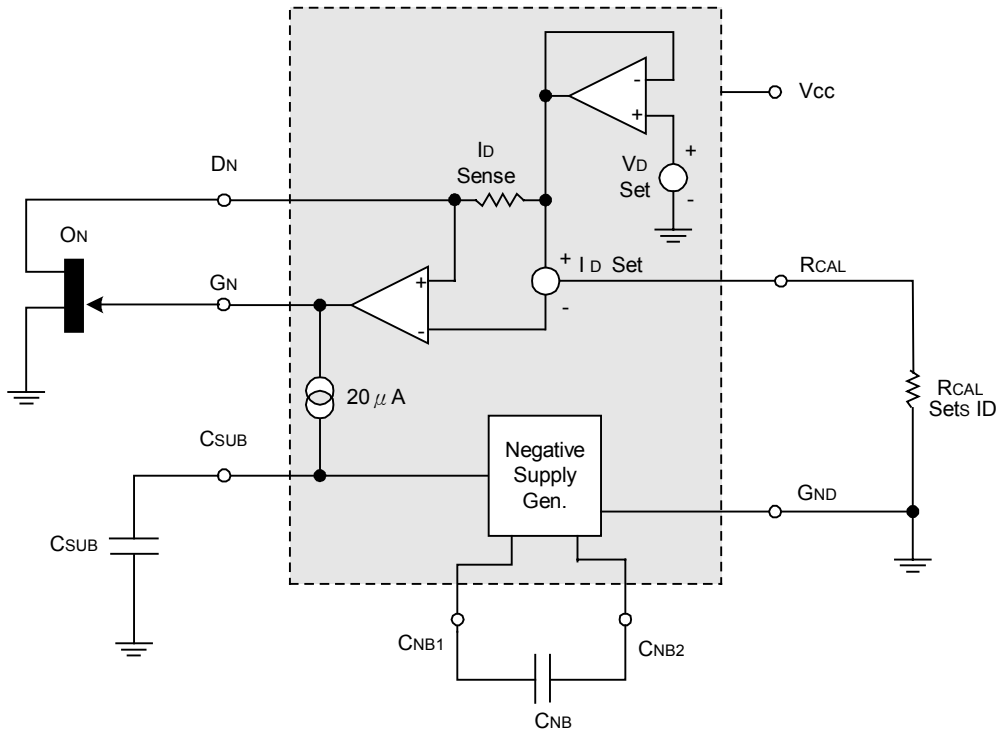
LB/HB Dropout Voltage v Load Current



Filter Response



FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

The X3211 provides all the bias requirements for external FETs, including the generation of the negative supply required for gate biasing, from the single supply voltage. It contains 3 such stages. The negative rail generator is common to all devices.

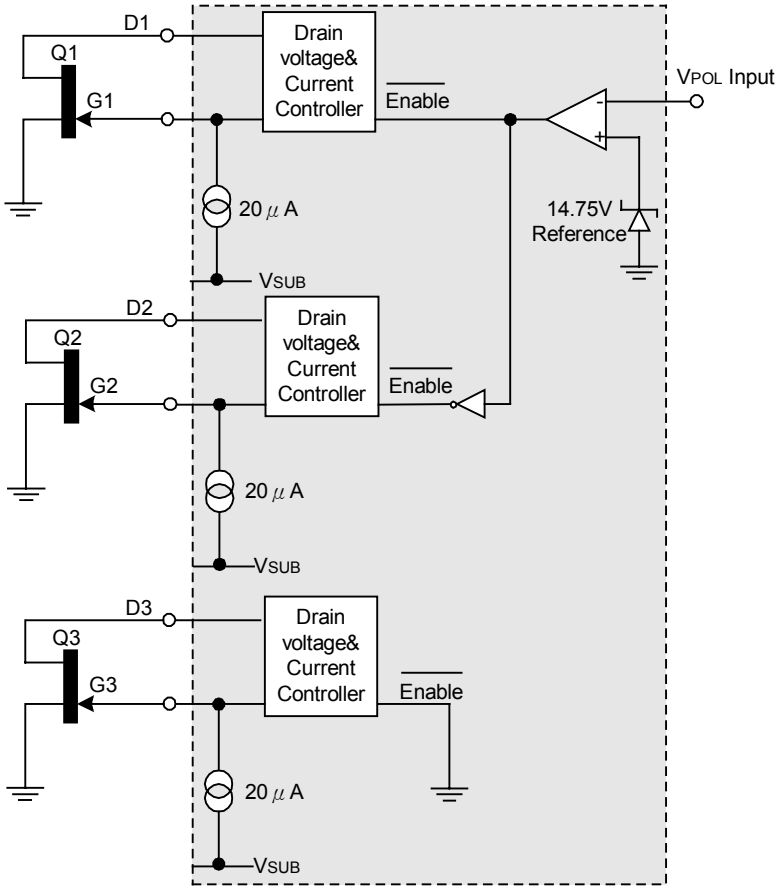
The drain voltage of the external FET Q_N is set by the X3211 device to its normal operating voltage. This is determined by the on board V_D Set reference, the X3211 provides nominally 2 volts .

The drain current taken by the FET is monitored by the low value resistor ID Sense. The amplifier driving the gate of the FET adjusts the gate voltage of Q_N so that the drain current taken matches the current called for by an external resistor R_{CAL}.

Since the FET is a depletion mode transistor, it is usually necessary to drive its gate negative with respect to ground to obtain the required drain current. To provide this capability powered from a single positive supply, the device includes a low current negative supply generator. This generator uses an internal oscillator and two external capacitors, C_{NB} and C_{SUB}.

The following schematic shows the function of the Vpol input. Only one of the two external FETs numberd Q1 and Q2 are powered at any one time, their selection is controlled by the input Vpol. This input is designed to be wired to

the power input of the LNB via a high value (10k) resistor. With th input voltage of the LNB set at or below 14V.FET Q2 will be enabled. With the input voltage at or above 15.5V,FET Q1 will be enabled.The disabled FET has its gate driven to 0V and its drain terminal is switched open circuit.FET number Q3 is always active regardless of the voltage applied to Vpol.

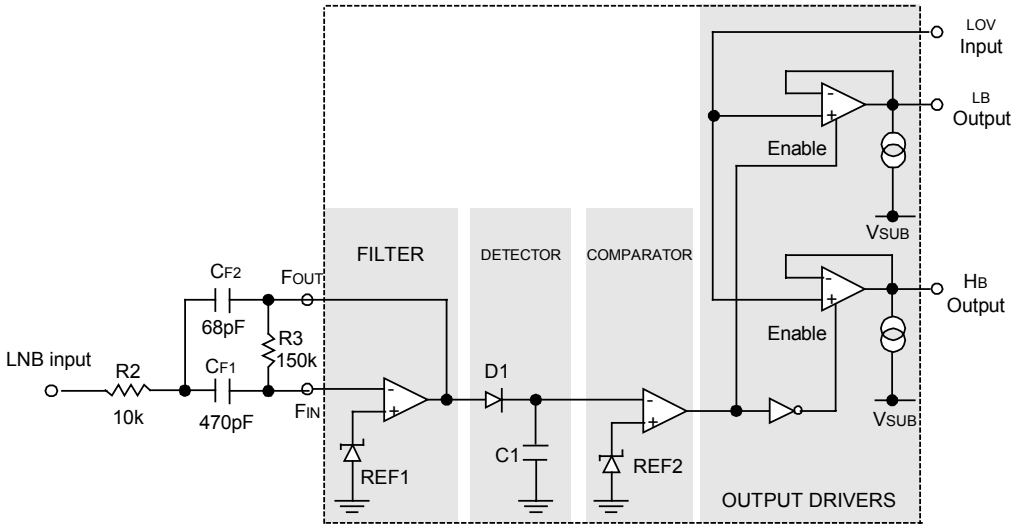


Control input switch function

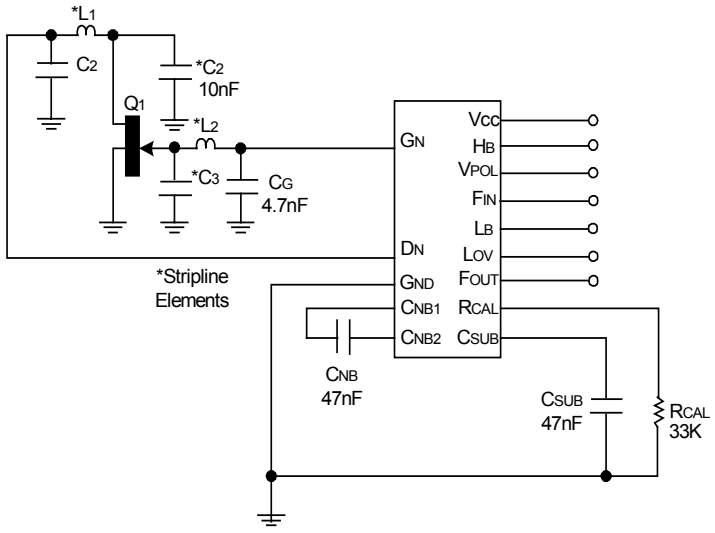
INPUT SENSE	POLARISATION	SELECT
<= <= ≤14 volts	Vertical	FET Q2
≥15.5 volts	Horizontal	FET Q1

For many LNB application tone detection and band switching is required.The X3211 includes the circuitry necessary to detect the presence of a 22kHz tone modulated on the supply input to the LNB.Referrring to the following schematic diagram,the main elements of this detector are an op-amp enabling the construction of a Sallen key filter,a rectifier/smoother and a comparator.Full control is given over the center frequency and bandwidth of the filter

by the selection of two external resistors and capacitors (one of these resistors,R2, shares the functionof overvoltge protection of pin Vpol).



APPLICATION CIRCUIT



APPLICATIONS INFORMATION

The device is a partial application circuit for the X3211 showing all external components required for appropriate biasing. The bias circuits are unconditionally stable over the full temperature range with the associated FETs and gate drain capacitors in circuit.

Capacitors C_D and C_G ensure that residual power supply and substrate generator noise is not allowed to affect other external circuits which may be sensitive to RF interference. They also serve to suppress any potential RF feedthrough between stages via the X3211. These capacitor are required for all stages used Values of 10nF and 4.7nF respectively are recommended however this is design dependent and any value between 1nFand 100nF could be used.

The capacitors C_{NB} and C_{SUB} are an integral part of the X3211 negative supply generator. The negative bias voltage is generated on-chip using an internal oscillator. The required value of capacitors C_{NB} and C_{SUB} is 47nF. This generator produces a low current supply of approximately –3 volts. Although this generator is intended purely to bias the external FETs, it can be used to power other external circuits via the C_{SUB} pin.

Resistors R_{CAL} sets the drain current at which all external FETs are operated. If any bias control circuit is not required, its related drain and gate connections may be left open circuit without affecting the operation of the remaining bias circuits.

The X3211 has been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range –3.5V to 1V,under any conditions including power up and powerdown transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current.

Tone detection and band switching is provided on the X3211. The following diagrams describes how this feature operates in an LNB and the external components required. The presence or absence of a 22kHz tone applied to pin FIN enables one of two outputs, L_B and H_B.A tone present enables H_B and tone absent enables L_B. The L_B and H_B outputs are designed to be compatible with both MMIC and discrete local oscillator applications, selected by pin L_{OV}. Referring to Figure 1 wiring pin L_{OV} to ground will force L_B and H_B to switch between –2.6V (disabled) and 0V (enabled).Referring to Figure 2 wiring pin L_{OV} to a positive voltage source (e.g. a potential divider across Vcc and ground set to the required oscillator supply,Vosc when enabled.

Tone Detection Function

L_{OV}	F_{IN}	L_B	H_B	L_B	H_B
GND	22kHz	Disabled	Enabled	-2.6 volts	GND
	-	Enabled	Disabled	GND	-2.6 volts
GND	22kHz	Disabled	Enabled	Note 1	Vosc
	-	Enabled	Disabled	Vosc	Note 1

Note 1: 0 volts in typical LNB applications but dependent on external circuits.

APPLICATIONS INFORMATION (cont)

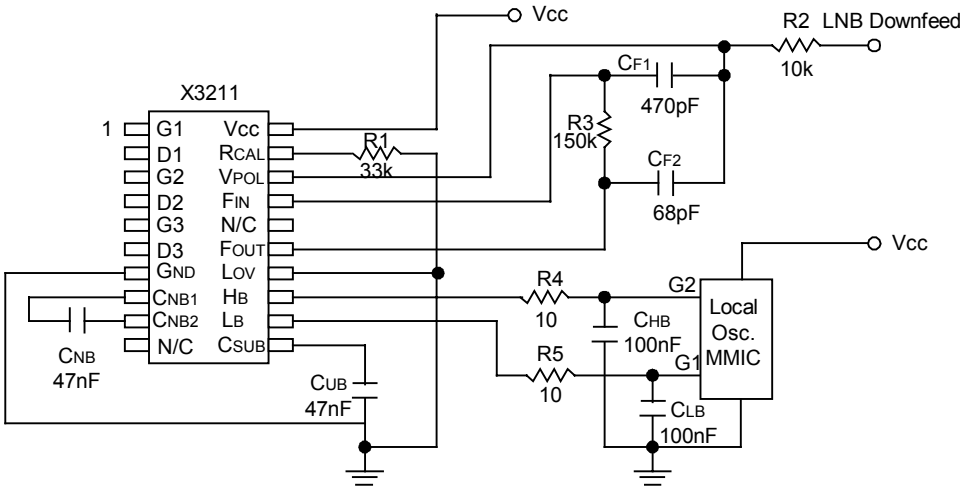


Figure 1 Lov grounded

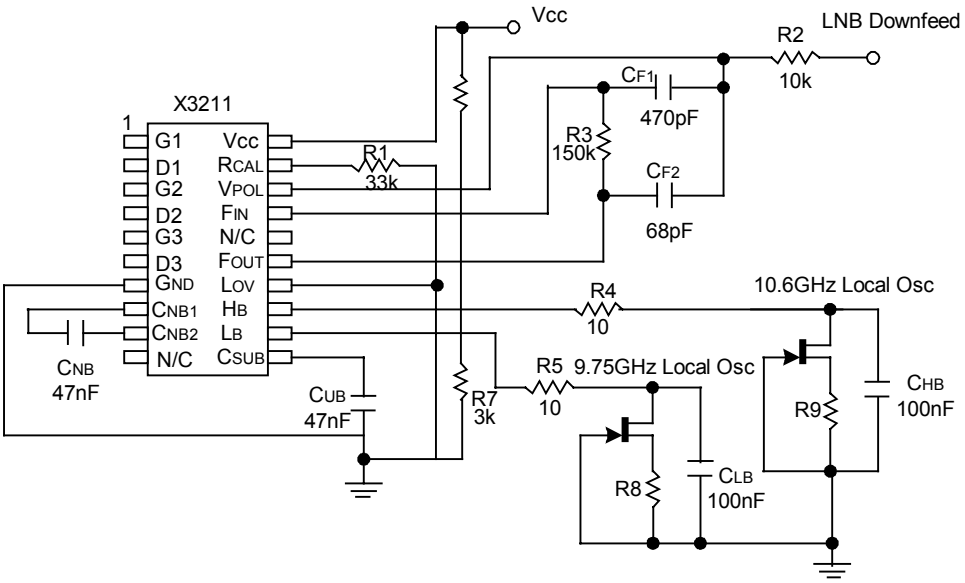


Figure 2 Lov connected to Vosc

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