

GENERAL DESCRIPTION

The HI-3182, HI-3183, HI-3184, HI-3185, HI-3186, HI-3187 and HI-3188 bus interface products are silicon gate CMOS devices designed as a line driver in accordance with the ARINC 429 bus specifications. In addition to being functional upgrades of Holt's HI-8382 & HI-8383 products, they are also alternate sources for the HS-3182 (Intersil/Harris), the RM3182 (Fairchild /Raytheon) and a variety of similar line driver products from other manufacturers.

Inputs are provided for clocking and synchronization. These signals are AND'd with the DATA inputs to enhance system performance and allow the HI-318X series of products to be used in a variety of applications. Both logic and synchronization inputs feature built-in 2,000V minimum ESD input protection as well as TTL and CMOS compatibility.

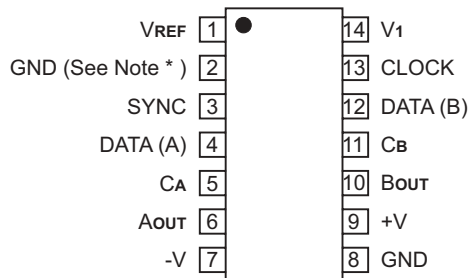
The differential outputs of the HI-318X series of products are programmable to either the high speed or low speed ARINC 429 output rise and fall time specifications through the use of two external capacitors. The output voltage swing is also adjustable by the application of an external voltage to the VREF input. Products with 0, 13 or 37.5 ohm resistors in series with each ARINC output are available. In addition, the HI-3182, HI-3184 and HI-3187 products also have a fuse in series with each output.

The HI-318X series of line drivers are intended for use where logic signals must be converted to ARINC 429 levels such as when using an ASIC, the HI-3282/HI-8282A ARINC 429 Serial Transmitter/Dual Receiver, the HI-6010 ARINC 429 Transmitter/Receiver or the HI-8783 ARINC Interface Device. Holt products are readily available for both industrial and military applications. Please contact the Holt Sales Department for additional information.

FEATURES

- Low power CMOS
- TTL and CMOS compatible inputs
- Programmable output voltage swing
- Adjustable ARINC rise and fall times
- Plastic 14 & 16-pin thermally enhanced SOIC packages available
- Pin-for-Pin alternative for Intersil/Fairchild applications
- Operates at data rates up to 100 Kbits
- Overvoltage protection
- Industrial and Military temperature ranges

PIN CONFIGURATION (Top View)



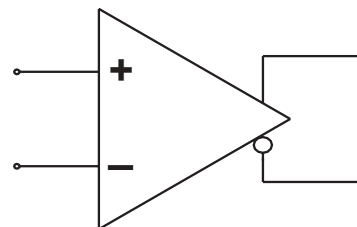
HI-3184PS, HI-3185PS, HI-3186PS & HI-3187PS

14 - PIN PLASTIC SMALL OUTLINE (ESQIC)** NB

Notes: * Pin 2 may be left floating
** Thermally Enhanced SOIC Package

(See Page 6 for additional package pin configurations)

FUNCTION



ARINC 429 DIFFERENTIAL LINE DRIVER

TRUTH TABLE

| SYNC | CLOCK | DATA(A) | DATA(B) | AOUT | BOUT | COMMENTS |
|------|-------|---------|---------|-------|-------|----------|
| X | L | X | X | 0V | 0V | NULL |
| L | X | X | X | 0V | 0V | NULL |
| H | H | L | L | 0V | 0V | NULL |
| H | H | L | H | -VREF | +VREF | LOW |
| H | H | H | L | +VREF | -VREF | HIGH |
| H | H | H | H | 0V | 0V | NULL |

FUNCTIONAL DESCRIPTION

The SYNC and CLOCK inputs establish data synchronization utilizing two AND gates, one for each data input (figure 2). Each logic input, including the power enable (STROBE) input, are TTL/CMOS compatible.

Figure 1 illustrates a typical ARINC 429 bus application. Three power supplies are necessary to operate the HI-3182; typically +15V, -15V and +5V. The chip also works with $\pm 12V$ supplies. The +5V supply can also provide a reference voltage that determines the output voltage swing. The differential output voltage swing will equal $2V_{REF}$. If a value of V_{REF} other than +5V is needed, a separate +5V power supply is required for pin V1.

With the DATA (A) input at a logic high and DATA (B) input at a logic low, AOUT will switch to the +VREF rail and BOUT will switch to the -VREF rail (ARINC HIGH state). With both data input signals at a logic low state, the outputs will both switch to 0V (ARINC NULL state).

The driver output impedance, ROUT, is nominally 75, 26 or 0 ohms depending on the option chosen. The rise and fall times of the outputs can be calibrated through the selection of two external capacitor values that are connected to the CA and CB input pins. Typical values for high-speed operation (100KBPS) are CA = CB = 75pF and for low-speed operation (12.5 to 14KBPS) CA = CB = 500pF.

The CA and CB pins swing between +5V and ground allowing the switching of capacitor values with an external single-supply analog switch.

The ARINC outputs can be put in a tri-state mode by applying a logic high to the STROBE input pin. If this feature is not being used, the pin should be tied to ground. The STROBE

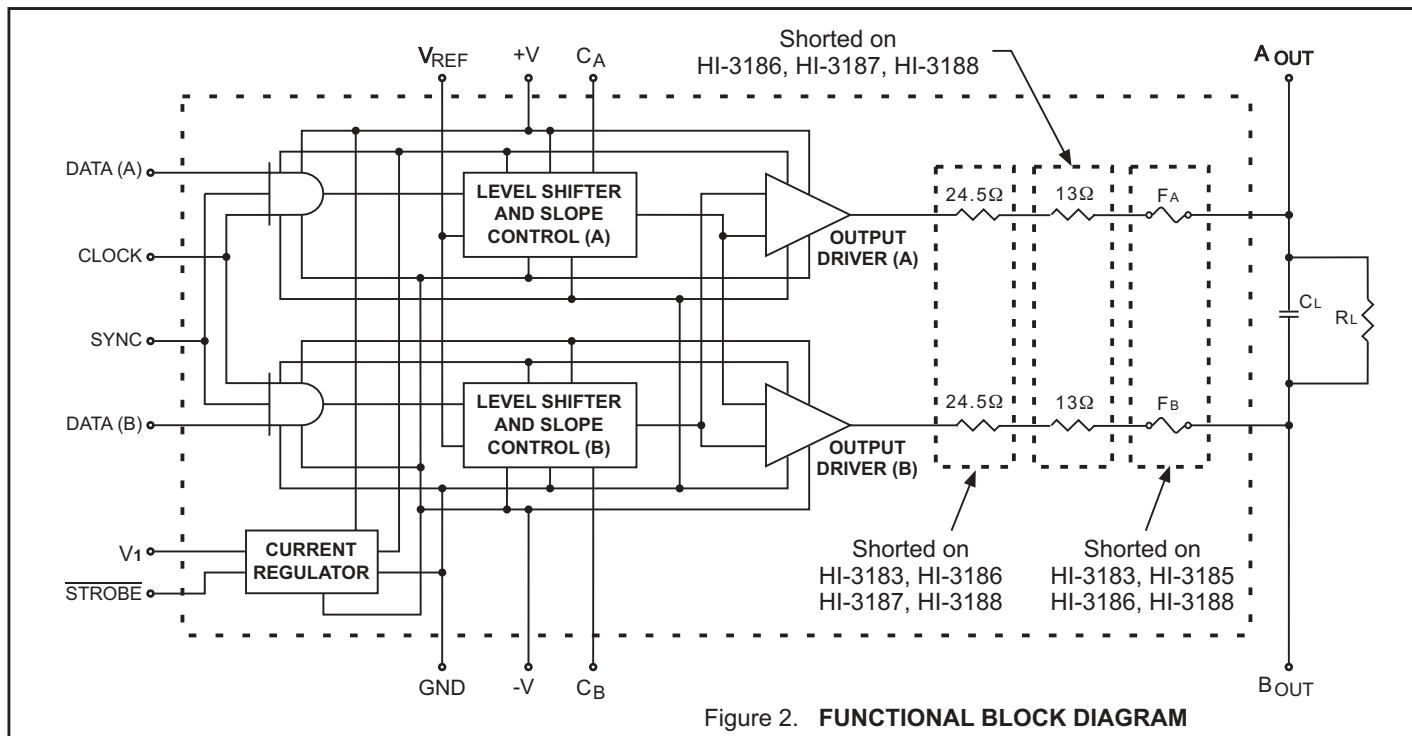
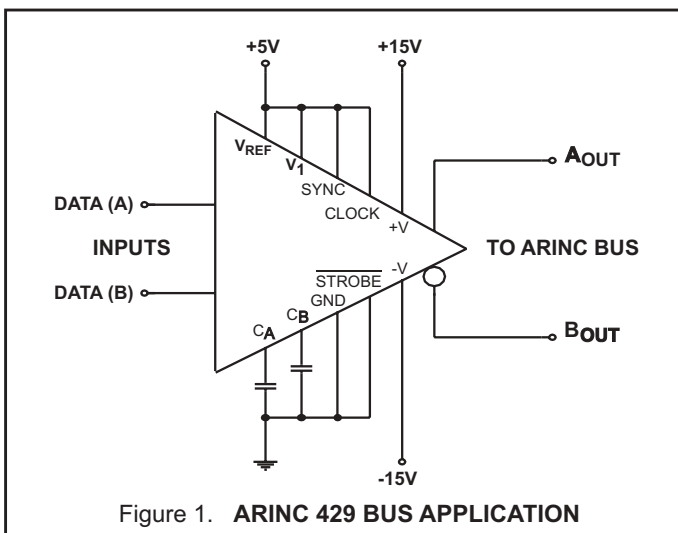
function is not available in the 14 & 16-pin SOIC package configurations where the pin is internally connected to ground.

The ARINC outputs of the HI-3182, HI-3184 and HI-3187 are protected by internal fuses capable of sinking between 800 - 900 mA for short periods of time (125 μ s).

The Vref pin has an internal pull-up resistor to V+, allowing the use of a simple external zener diode to set the reference voltage.

POWER SUPPLY SEQUENCING

The power supplies should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is +V followed by V1, always ensuring that +V is the most positive supply. The -V supply is not critical and can be asserted at any time.



PIN DESCRIPTIONS

| SYMBOL | FUNCTION | DESCRIPTION |
|----------|----------|---|
| VREF | ANALOG | Ref. voltage used to determine output voltage swing. Pin sources current to allow use of a zener reference. |
| STROBE | INPUT | A logic high tri-states the ARINC outputs. Not available in the 14-pin SOIC package (tied to GND internally). |
| SYNC | INPUT | Synchronizes data inputs |
| DATA (A) | INPUT | Data input terminal A |
| CA | INPUT | Connection for DATA (A) slew-rate capacitor |
| AOUT | OUTPUT | ARINC output terminal A |
| -V | POWER | -12V to -15V |
| GND | POWER | 0.0V |
| +V | POWER | +12V to +15V |
| BOUT | OUTPUT | ARINC output terminal B |
| Cb | INPUT | Connection for DATA (B) slew-rate capacitor |
| DATA (B) | INPUT | Data input terminal B |
| CLOCK | INPUT | Synchronizes data inputs |
| V1 | POWER | +5V ±5% |

ABSOLUTE MAXIMUM RATINGS

All Voltages referenced to GND, TA = Operating Temperature Range (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | OPERATING RANGE | MAXIMUM | UNIT |
|--|------------------|--|--|-------------------------|-------------|
| Differential Voltage | V _{DIF} | Voltage between +V and -V terminals | | 40 | V |
| Supply Voltage | +V -V V1 | | +10.8 to +16.5 -10.8 to -16.5 +5 ±5% | +7 | V V V |
| Voltage Reference | VREF | For ARINC 429 For Applications other than ARINC | +5 ±5% 1.5 to 6 | 6 6 | V V |
| Input Voltage Range | V _{IN} | | | ≥ GND -0.3 ≤ V1 +0.3 | V V |
| Output Short-Circuit Duration | | See Note: 1 | | | |
| Output Overvoltage Protection | | See Note: 2 | | | |
| Operating Temperature Range | TA | High-temp & Military Industrial | -55 to +125 -40 to +85 | | °C °C |
| Storage Temperature Range | T _{STG} | Ceramic & Plastic | -65 to +150 | | °C |
| Lead Temperature | | Soldering, 10 seconds | | +275 | °C |
| Junction Temperature | T _J | | | +175 | °C |
| Note 1. Heatsinking may be required for continuous Output Short Circuit at +125°C and for 100KBPS at +125°C. Note 2. The fuses used for Output Overvoltage Protection may be blown by the presence of a voltage at either output that is greater than ±12.0V with respect to GND. (HI-3182, 3184 & 3187 only) | | | | | |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V₁ = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

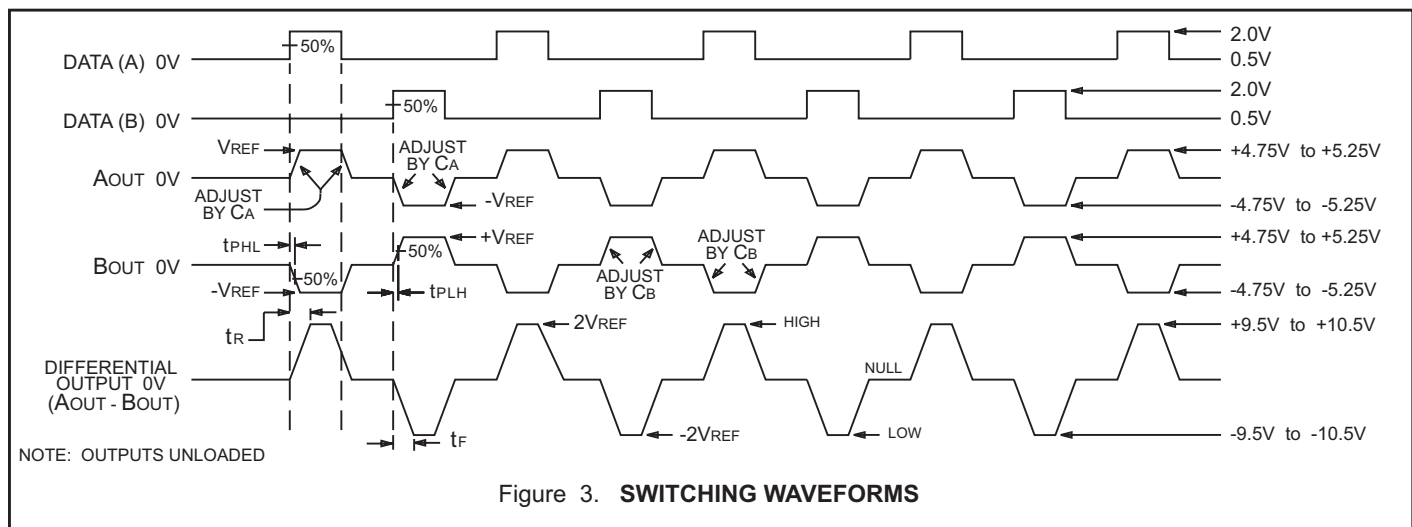
| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|--|---------------------------|---|---------------------------|------|---------------------------|-------|
| Supply Current +V (Operating) | ICCOP (+V) | No Load (0 - 100KBPS) | | | +16 | mA |
| Supply Current -V (Operating) | ICCOP (-V) | No Load (0 - 100KBPS) | -16 | | | mA |
| Supply Current V ₁ (Operating) | ICCOP (V ₁) | No Load (0 - 100KBPS) | | | 500 | μA |
| Reference Pin Current V _{REF} (Operating) | ICCOP (V _{REF}) | No Load, V _{REF} = 5V (0 - 100KBPS) | -1.0 | -0.4 | -0.15 | mA |
| Supply Current +V (During Short Circuit Test) | ISC (+V) | Short to Ground (See Note: 1) | | | 150 | mA |
| Supply Current -V (During Short Circuit Test) | ISC (-V) | Short to Ground (See Note: 1) | -150 | | | mA |
| Output Short Circuit Current (Output High) | IOHSC | Short to Ground V _{MIN} =0 (See Note: 2) | | | -80 | mA |
| Output Short Circuit Current (Output Low) | IOLSC | Short to Ground V _{MIN} =0 (See Note: 2) | +80 | | | mA |
| Input Current (Input High) | I _{IH} | | | | 1.0 | μA |
| Input Current (Input Low) | I _{IL} | | -1.0 | | | μA |
| Input Voltage High | V _{IH} | | 2.0 | | | V |
| Input Voltage Low | V _{IL} | | | | 0.5 | V |
| Output Voltage High (Output to Ground) | V _{OH} | No Load (0 -100KBPS) | +V _{REF} -.25 | | +V _{REF} +.25 | V |
| Output Voltage Low (Output to Ground) | V _{OL} | No Load (0 -100KBPS) | -V _{REF} -.25 | | -V _{REF} +.25 | V |
| Output Voltage Null | V _{NULL} | No Load (0-100KBPS) | -250 | | +250 | mV |
| Input Capacitance | C _{IN} | See Note 1 | | 15 | | pF |

Note 1. Not tested, but characterized at initial device design and after major process and/or design change which affects this parameter.
 Note 2. Interchangeability of force and sense is acceptable.

AC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V₁ = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|--|------------------|--|-----|-----|-----|-------|
| Rise Time (A _{OUT} , B _{OUT}) | t _R | C _A = C _B = 75pF See Figure 3. | 1.0 | | 2.0 | μs |
| Fall Time (A _{OUT} , B _{OUT}) | t _F | C _A = C _B = 75pF See Figure 3. | 1.0 | | 2.0 | μs |
| Propagation Delay Input to Output | t _{PLH} | C _A = C _B = 75pF See Figure 3. | | | 3.0 | μs |
| Propagation Delay Input to Output | t _{PHL} | C _A = C _B = 75pF See Figure 3. | | | 3.0 | μs |



HI-318X PACKAGE THERMAL CHARACTERISTICS

MAXIMUM ARINC LOAD ^{3, 6, 7}

| PACKAGE STYLE ¹ | HEAT SINK | ØJA (°C/W) | SUPPLY CURRENT ² | JUNCTION TEMPERATURE, T _j | | |
|--|------------|---------------|-----------------------------|--------------------------------------|-----------|------------|
| | | | | TA = 25°C | TA = 85°C | TA = 125°C |
| 14-pin Thermally Enhanced Plastic SOIC (ESOIC) | Unsoldered | 82 | 20 mA | 57°C | 117°C | 157°C |
| | Soldered | 65 | 20 mA | 51°C | 111°C | 151°C |
| 14-pin Thermally Enhanced Plastic SOIC (ESOIC) | Unsoldered | 51 | 20 mA | 45°C | 105°C | 145°C |
| | Soldered | 28 | 20 mA | 36°C | 96°C | 136°C |
| 28-pin Plastic PLCC | N/A | 70 | 25 mA | 56°C | 110°C | 150°C |

AOUT and BOUT Shorted to Ground ^{3, 4, 5, 6, 7}

| PACKAGE STYLE ¹ | HEAT SINK | ØJA (°C/W) | SUPPLY CURRENT ² | JUNCTION TEMPERATURE, T _j | | |
|--|------------|---------------|-----------------------------|--------------------------------------|-----------|------------|
| | | | | TA = 25°C | TA = 85°C | TA = 125°C |
| 14-pin Thermally Enhanced Plastic SOIC (ESOIC) | Unsoldered | 82 | 36 mA | 57°C | 147°C | 187°C |
| | Soldered | 65 | 36 mA | 78°C | 138°C | 178°C |
| 14-pin Thermally Enhanced Plastic SOIC (ESOIC) | Unsoldered | 51 | 40 mA | 64°C | 124°C | 164°C |
| | Soldered | 28 | 40 mA | 53°C | 113°C | 153°C |
| 28-pin Plastic PLCC | N/A | 70 | 63 mA | 100°C | 150°C | 182°C |

Notes:

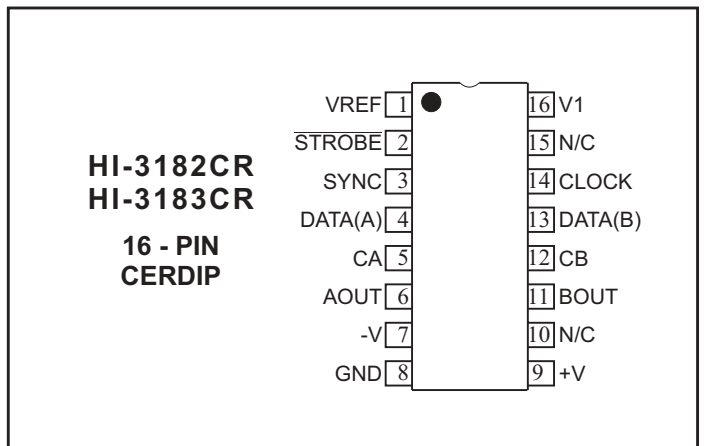
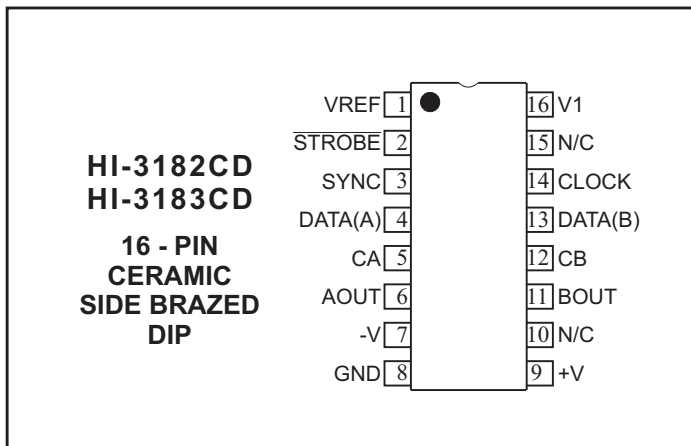
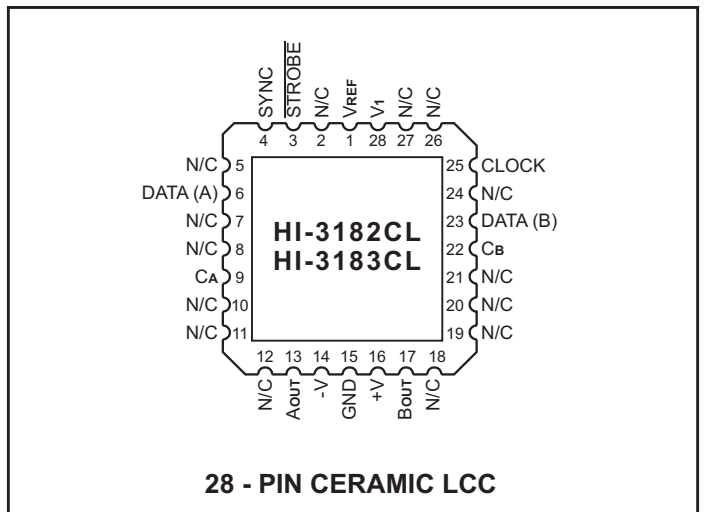
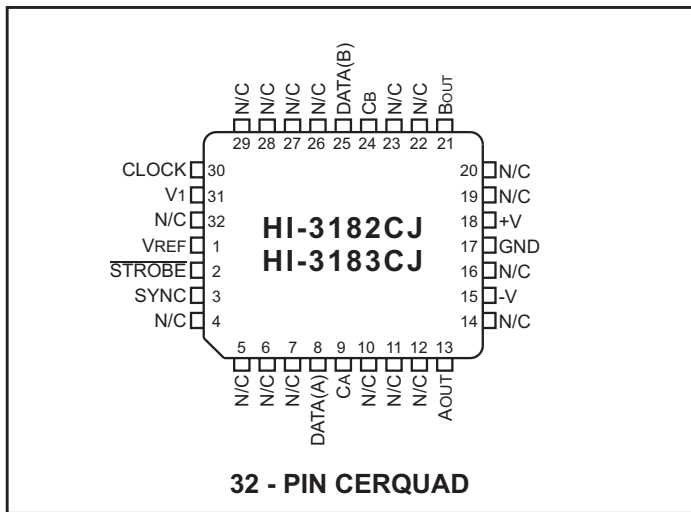
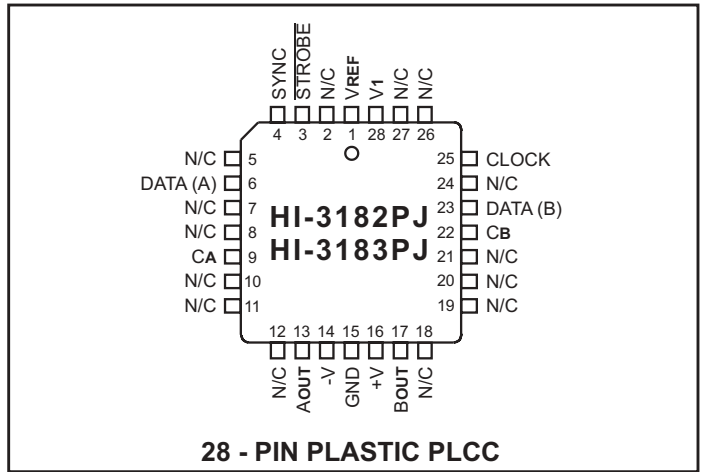
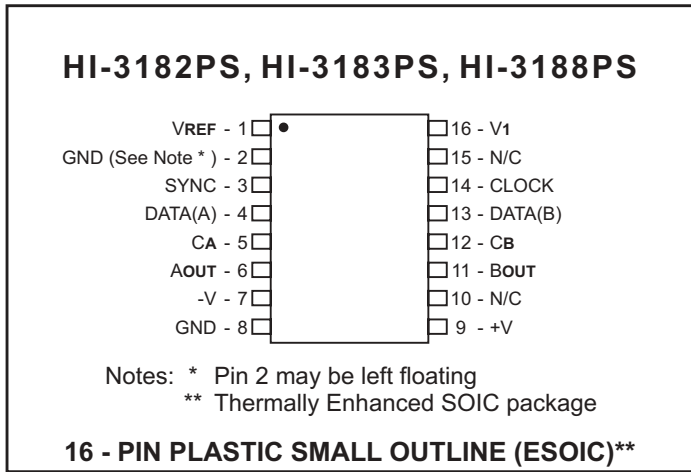
1. All data taken in still air on devices soldered to a single layer copper PCB (3" X 4.5" X .062").
2. At 100% duty cycle, 15V power supplies. For 12V power supplies multiply all tabulated values by 0.8.
3. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
4. Similar results would be obtained with AOUT shorted to BOUT.
5. For applications requiring survival with continuous short circuit, operation above T_j = 175°C is not recommended.
6. Data will vary depending on air flow and the method of heat sinking employed.
7. Current values listed are for each of the +V and -V supplies.

HEAT SINK - ESOIC PACKAGES

Both the 14-pin and 16-pin thermally enhanced SOIC packages are used for HI-318X products. These ESOIC packages include a metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board for optimum thermal

dissipation. The heat sink is electrically isolated from the chip and can be soldered to any ground or power plane. However, since the chip's substrate is at +V, connecting the heat sink to this power plane is recommended to avoid coupling noise into the circuit.

ADDITIONAL PIN CONFIGURATIONS (See page 1 for 14-Pin Small Outline SOIC)



ORDERING INFORMATION

HI - 318x x x - xx (Ceramic)

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|-------------|-------------------|------|---------|
| I | -40°C TO +85°C | I | NO |
| T | -55°C TO +125°C | T | NO |
| M | -55°C TO +125°C | M | YES |

| PART NUMBER | PACKAGE DESCRIPTION | LEAD FINISH (1) |
|-------------|---|-------------------------|
| CD | 16 PIN CERAMIC SIDE BRAZED DIP | Gold ('M' flow: solder) |
| CJ | 32 PIN J-LEAD CERQUAD (not available with 'M' flow) | Solder |
| CL | 28 PIN CERAMIC LEADLESS CHIP CARRIER (LCC) | Gold ('M' flow: solder) |
| CR | 16 PIN CERDIP (not available with 'M' flow) | Solder |

| PART NUMBER | OUTPUT SERIES | |
|-------------|---------------|------|
| | RESISTANCE | FUSE |
| 3182 | 37.5 Ohms | YES |
| 3183 | 13 Ohms | NO |

HI - 318xxx x x (Plastic)

| PART NUMBER | LEAD FINISH |
|-------------|--|
| Blank | Tin / Lead (Sn / Pb) Solder |
| F | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|-------------|-------------------|------|---------|
| I | -40°C TO +85°C | I | NO |
| T | -55°C TO +125°C | T | NO |
| M (2) | -55°C TO +125°C | M | YES |

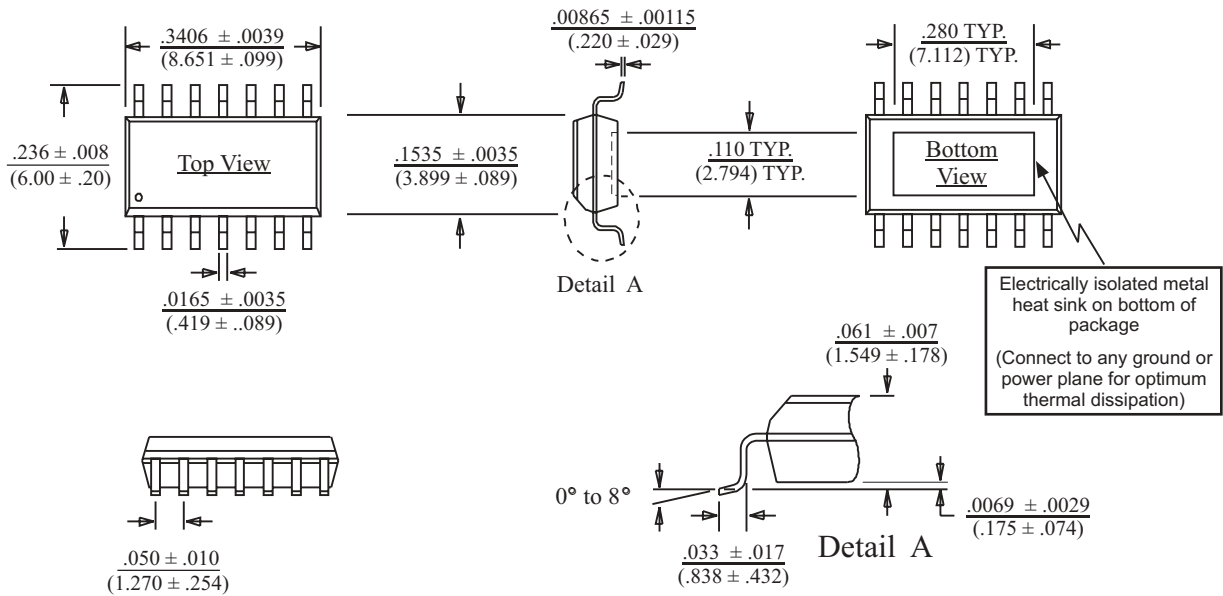
| PART NUMBER | PACKAGE DESCRIPTION | OUTPUT SERIES | |
|-------------|---|---------------|------|
| | | RESISTANCE | FUSE |
| 3182PJ | 28 PIN PLASTIC J-LEAD PLCC | 37.5 Ohms | YES |
| 3182PS | 16 PIN PLASTIC SMALL OUTLINE - WB (ESOIC) | 37.5 Ohms | YES |
| 3183PJ | 28 PIN PLASTIC J-LEAD PLCC | 13 Ohms | NO |
| 3183PS | 16 PIN PLASTIC SMALL OUTLINE - WB (ESOIC) | 13 Ohms | NO |
| 3184PS | 14 PIN PLASTIC SMALL OUTLINE - NB (ESOIC) | 37.5 Ohms | YES |
| 3185PS | 14 PIN PLASTIC SMALL OUTLINE - NB (ESOIC) | 37.5 Ohms | NO |
| 3186PS | 14 PIN PLASTIC SMALL OUTLINE - NB (ESOIC) | 13 Ohms | NO |
| 3187PS | 14 PIN PLASTIC SMALL OUTLINE - NB (ESOIC) | 13 Ohms | YES |
| 3188PS | 16 PIN PLASTIC SMALL OUTLINE - WB (ESOIC) | 13 Ohms | NO |

Legend: ESOIC - Thermally Enhanced Small Outline Package (SOIC w/built-in heat sink)
 NB - Narrow Body
 WB - Wide Body

- (1) Gold terminal finish is Pb-Free, RoHS compliant.
 (2) Only available with '3182PJ'.

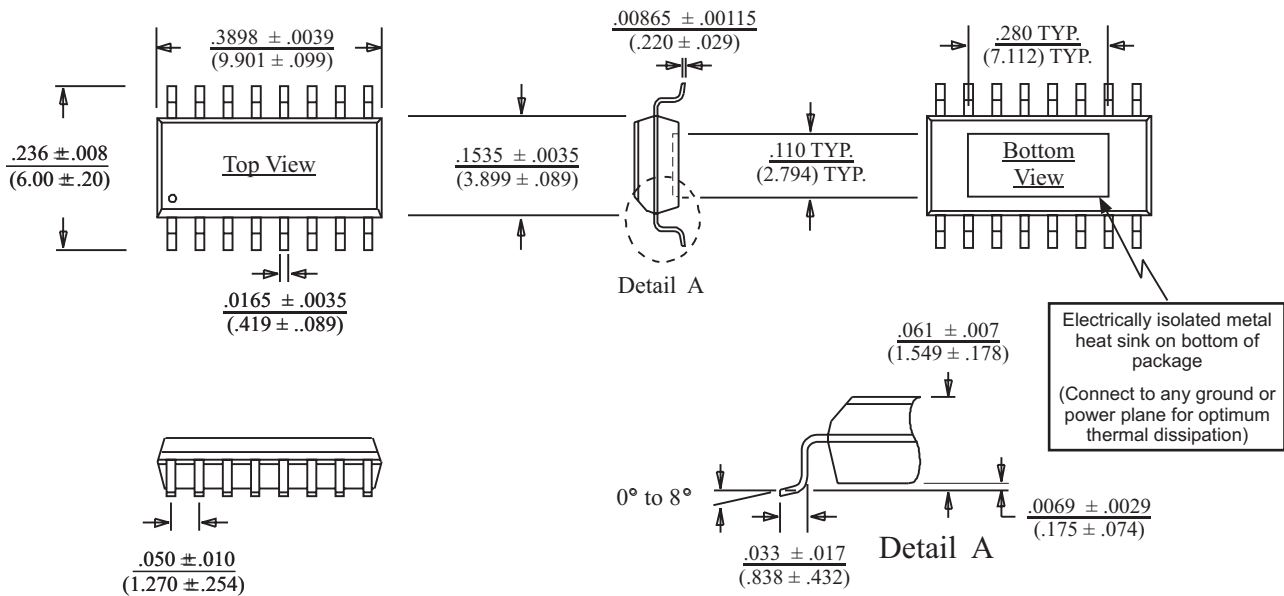
14-PIN PLASTIC SMALL OUTLINE (ESOC) - NB
(Narrow Body, Thermally Enhanced)

Package Type: 14HNE



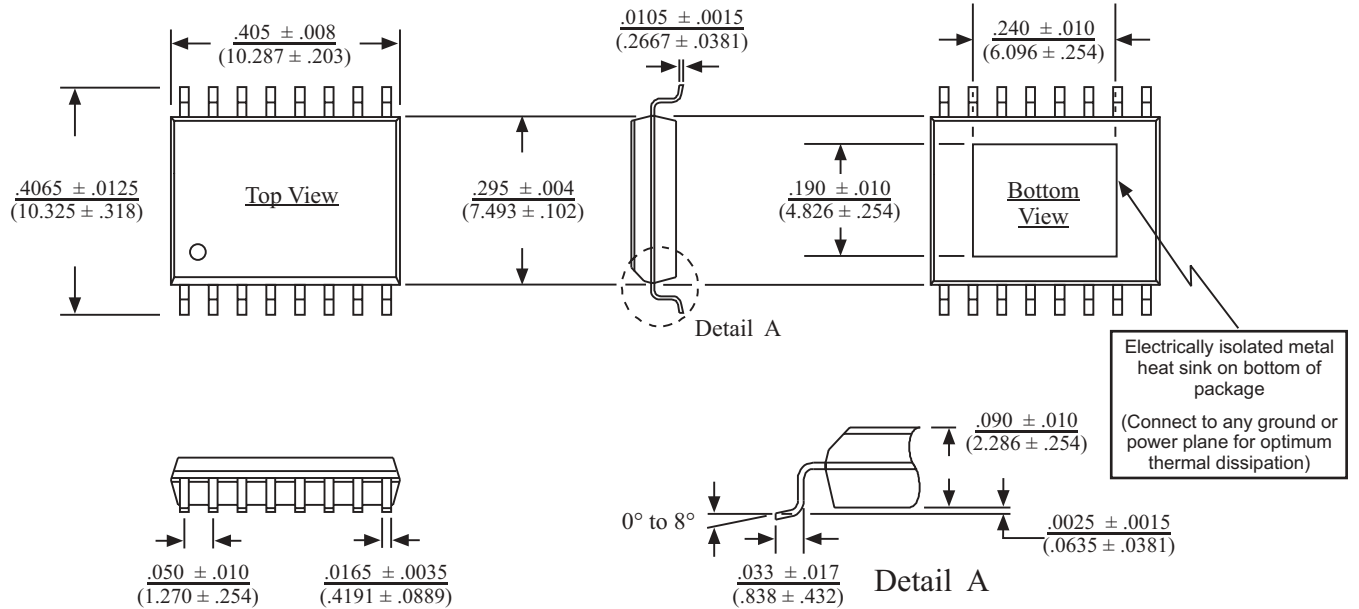
16-PIN PLASTIC SMALL OUTLINE (ESOC) - NB
(Narrow Body, Thermally Enhanced)

Package Type: 16HNE



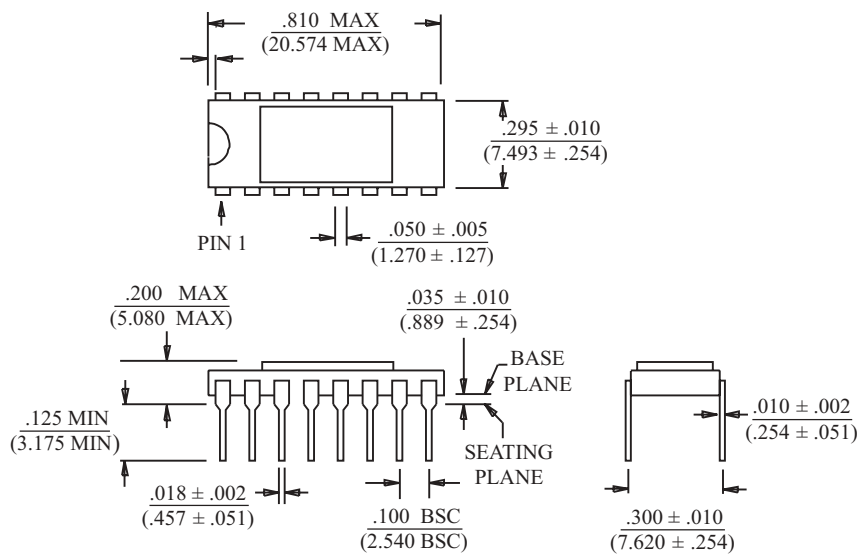
16-PIN PLASTIC SMALL OUTLINE (ESQIC) - WB
(Wide Body, Thermally Enhanced)

Package Type: 16HWE



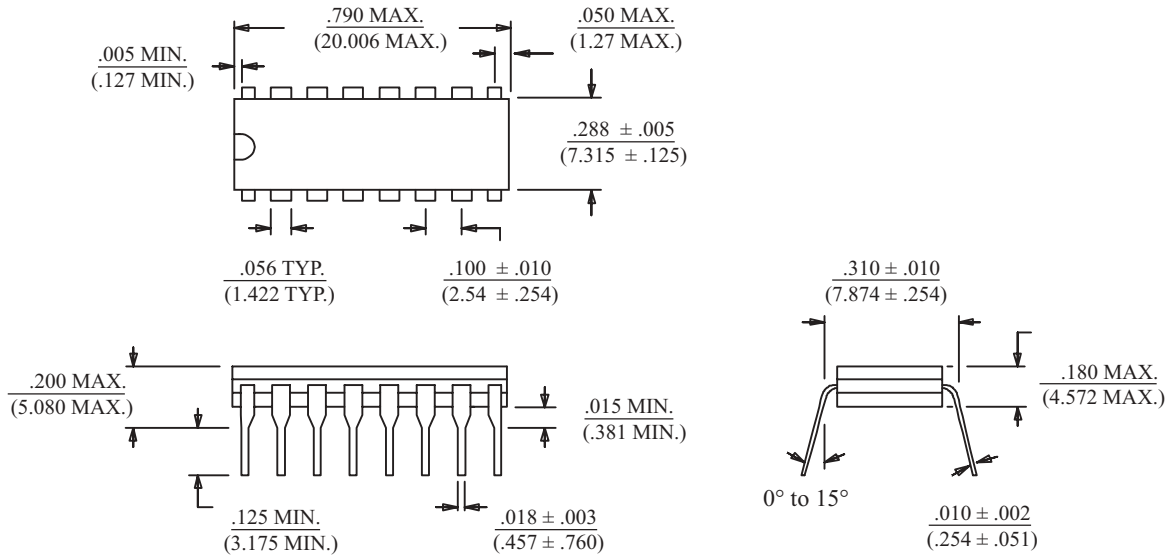
16-PIN CERAMIC SIDE-BRAZED DIP

Package Type: 16C



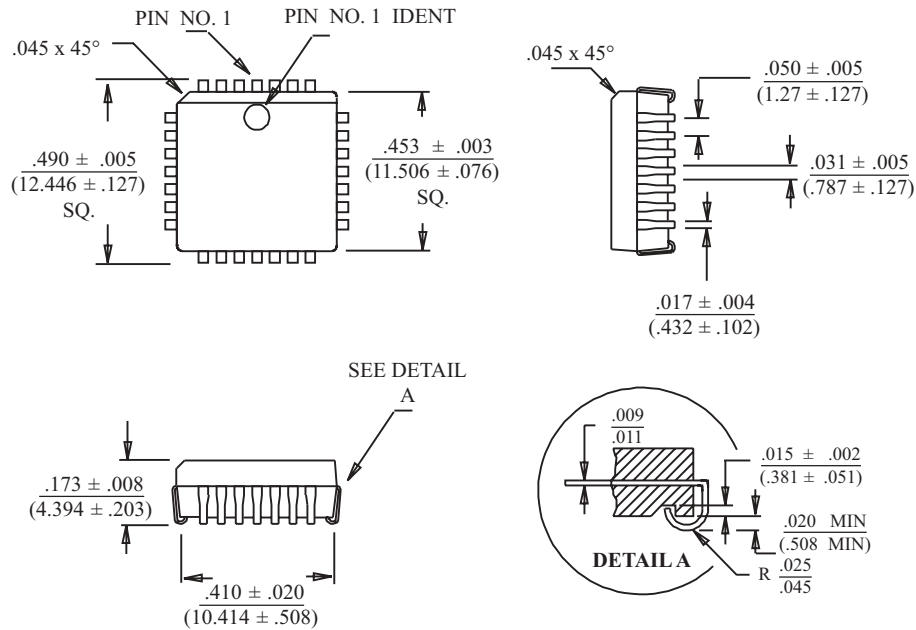
16-PIN CERDIP

Package Type: 16D



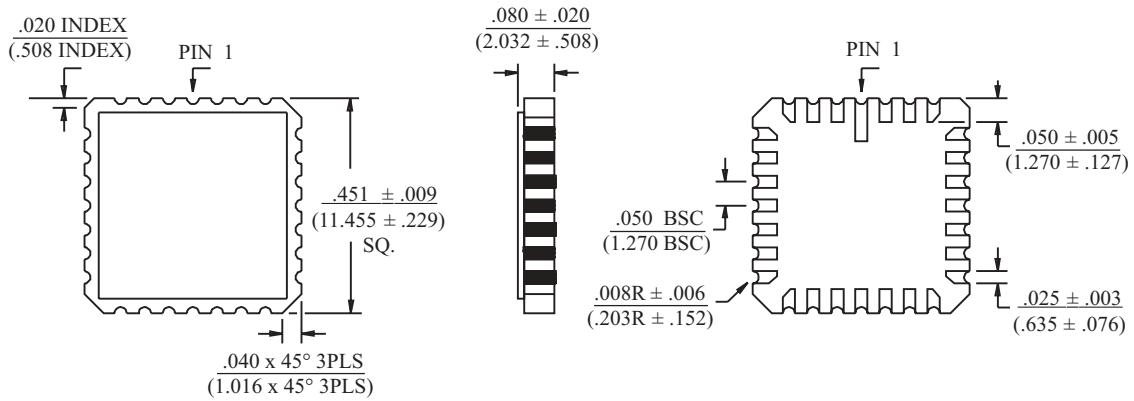
28-PIN PLASTIC PLCC

Package Type: 28J



28-PIN CERAMIC LEADLESS CHIP CARRIER

Package Type: 28S



32-PIN J-LEAD CERQUAD

Package Type: 32U

