Data Sheet No.PD60221

International
IOR Rectifier

IRS2011SPBF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational up to +200V
  Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10V to 20V
- Independent low and high side channels
- Input logic HIN/LIN active high
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels

Product Summary

V_{OFFSET}	200V max.
I_O+/-	1.0A /1.0A typ.
V_{OUT}	10 - 20V
$t_{on/off}$	60 ns typ.
Delay Matching	20 ns max.

Applications

- Audio Class D amplifiers
- High power DC-DC SMPS converters
- Other high frequency applications

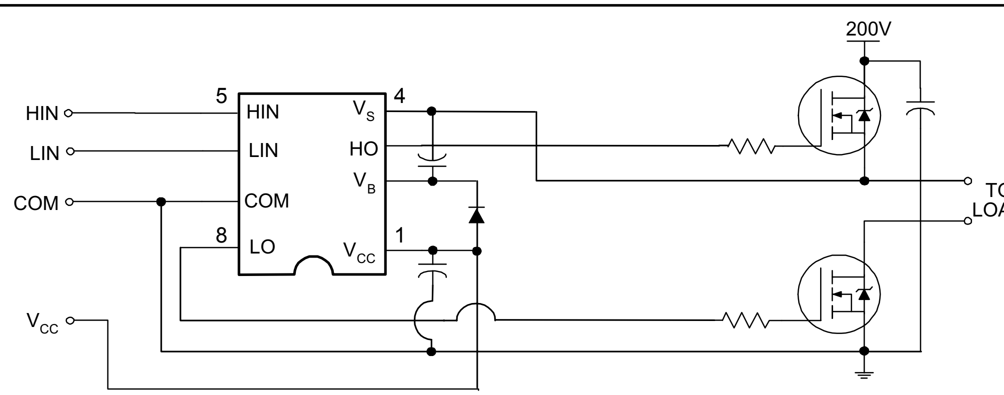
Packages

8-Lead SOIC

Description

The IRS2011 is a high power, high speed power MOSFET driver with independent high and low side referenced output channels, ideal for Audio Class D and DC-DC converter applications. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.0V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 200 volts. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

Typical Connection



(Refer to Lead Assignments for correct configuration). This/These diagram(s) show electrical connections only.
Please refer to our Application Notes and DesignTips for proper circuit board layout.

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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	220	V
V_S	High side floating supply offset voltage		V_B - 20	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage		-0.3	20	
V_{LO}	Low side output voltage		-0.3	V_{CC} +0.3	
V_{IN}	Logic input voltage (HIN & LIN)		-0.3	V_{CC} +0.3	
dV_s/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ T_A = +25°C	(8-lead DIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
R_{THJA}	Thermal resistance, junction to ambient	(8-lead DIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S and COM offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	200	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)	COM	5.5	
T_A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -8V to +200V. Logic state held for V_S of -8V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF, T_A = 25°C unless otherwise specified. Figure 1 shows the timing definitions.

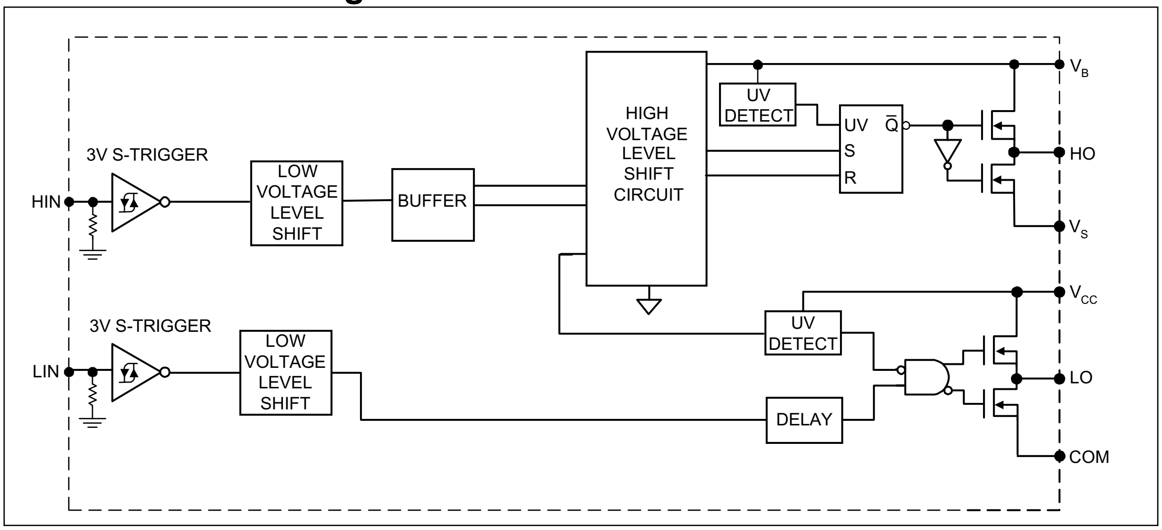
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	60	80	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	60	80		V_S = 200V
t_r	Turn-on rise time	—	25	40		
t_f	Turn-off fall time	—	15	35		
DM1	Turn-on delay matching $\vert t_{on}$ (H) - t_{on} (L) $\vert$	—	—	20		
DM2	Turn-off delay matching $\vert t_{off}$ (H) - t_{off} (L) $\vert$	—	—	20		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.5	—	—	V	V_{CC} = 10V - 20V
V_{IL}	Logic "0" input voltage	—	—	1.2		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B=V_S = 200V
I_{QBS}	Quiescent V_{BS} supply current	—	120	210		V_{IN} = 0V or 3.3V
I_{QCC}	Quiescent V_{CC} supply current	—	200	300		V_{IN} = 0V or 3.3V
I_{IN+}	Logic "1" input bias current	—	3	10		V_{IN} = 3.3V
I_{IN-}	Logic "0" input bias current	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.3	9.0	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.5	8.2	8.9		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.3	9.0	9.7		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.5	8.2	8.9		
I_{O+}	Output high short circuit pulsed current	—	1.0	—	A	V_O = 0V, PW = 10 µs
I_{O-}	Output low short circuit pulsed current	—	1.0	—		V_O = 15V, PW = 10 µs

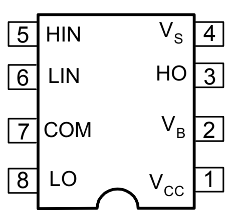
Functional Block Diagram



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



8-Lead SOIC

IRS2011SPBF

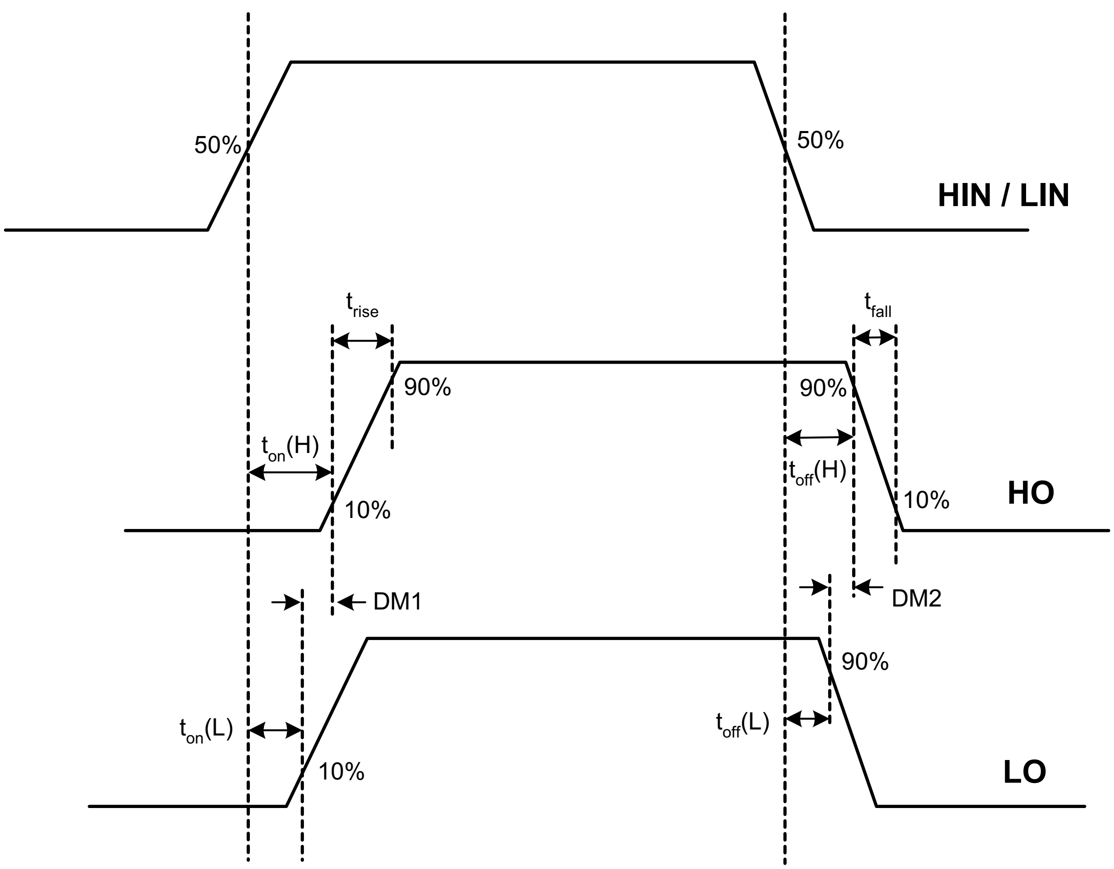


Figure 1. Timing Diagram

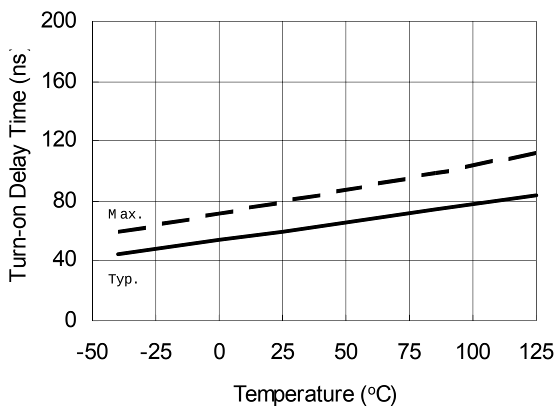


Figure 2A. Turn-On Time vs. Temperature

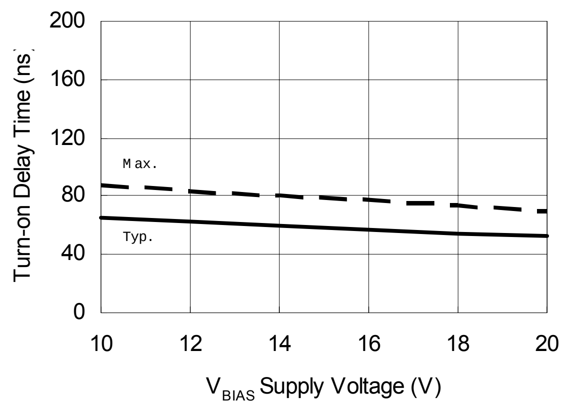


Figure 2B. Turn-On Time vs. Supply Voltage

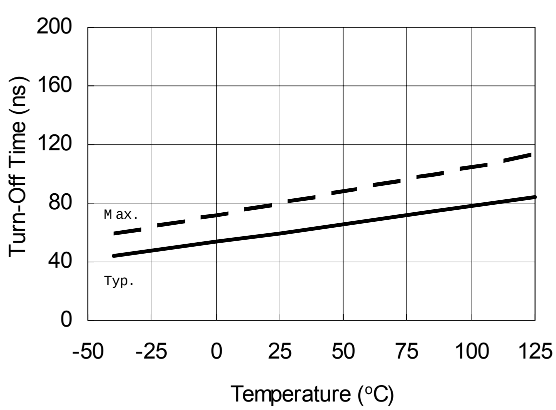


Figure 3A. Turn-Off Time vs. Temperature

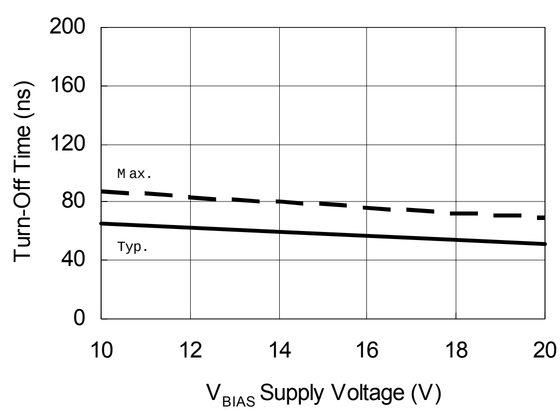
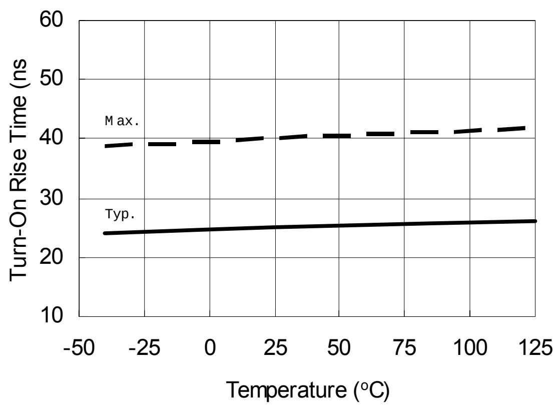


Figure 3B. Turn-Off Time vs. Supply Voltage



Fiure 4A. Turn-On Rise Time
vs.Temperature

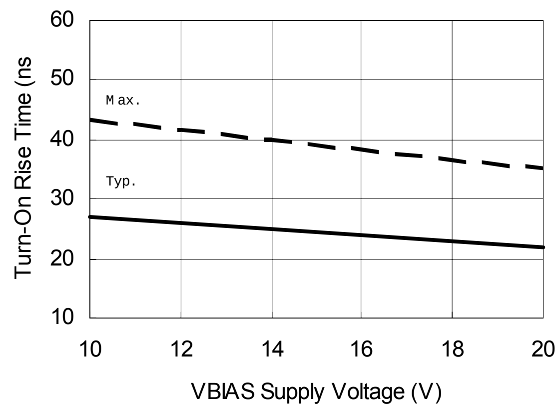


Figure 4B. Turn-On Rise Time
vs. Supply Voltage

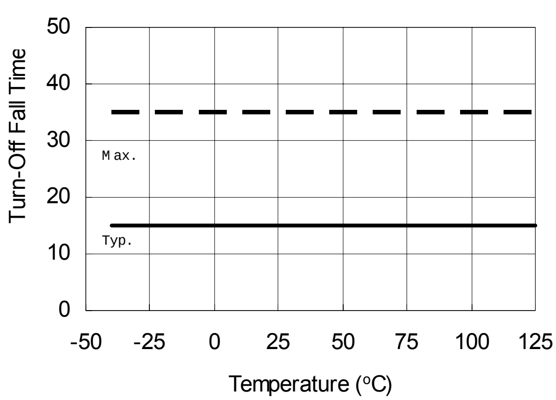


Figure 5A. Turn-Off Fall Time
vs. Temperature

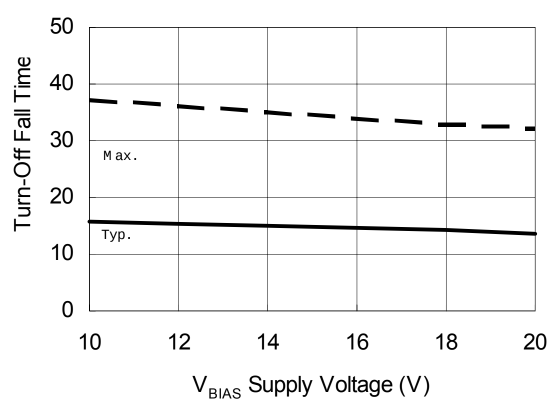


Figure 5B. Turn-Off Fall Time
vs. Supply Voltage

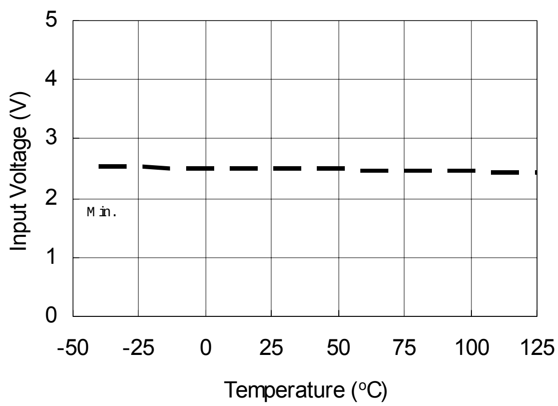


Figure 6A. Logic "1" Input Voltage vs. Temperature

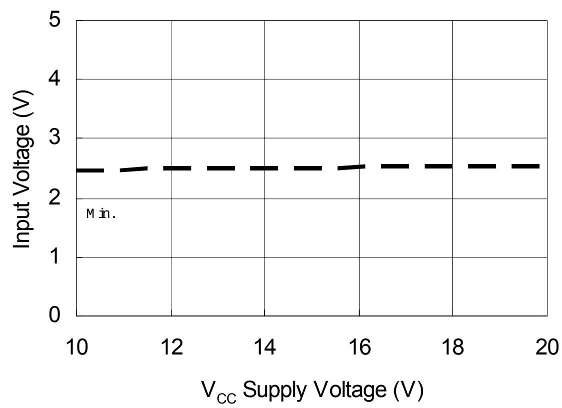


Figure 6B. Logic "1" Input Voltage vs. Supply Voltage

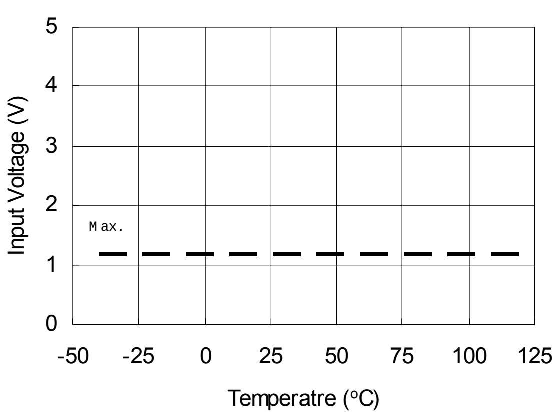


Figure 7A. Logic "0" Input Voltage vs. Temperature

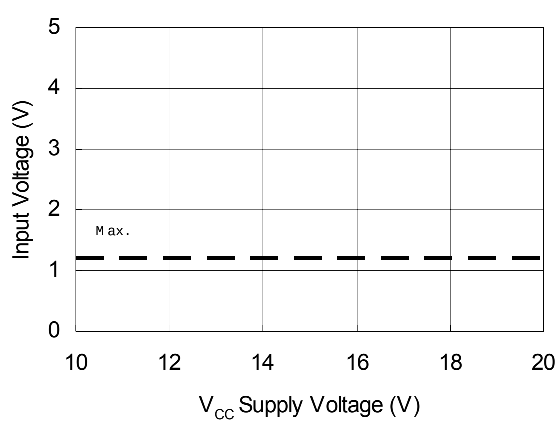


Figure 7B. Logic "0" Input Voltage vs. Supply Voltage

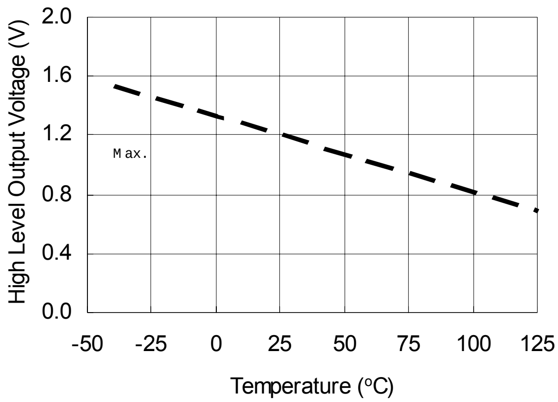


Figure 8A. High Level Output vs. Temperature

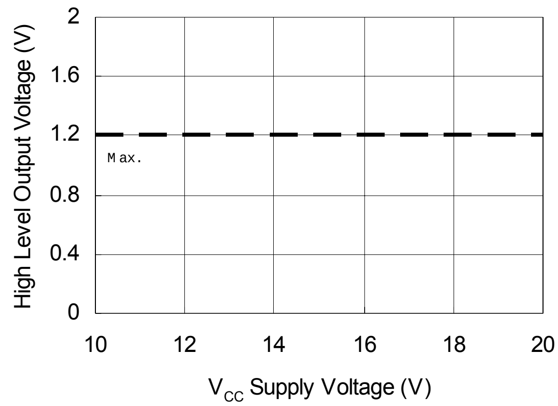


Figure 8B. High Level Output vs. Supply Voltage

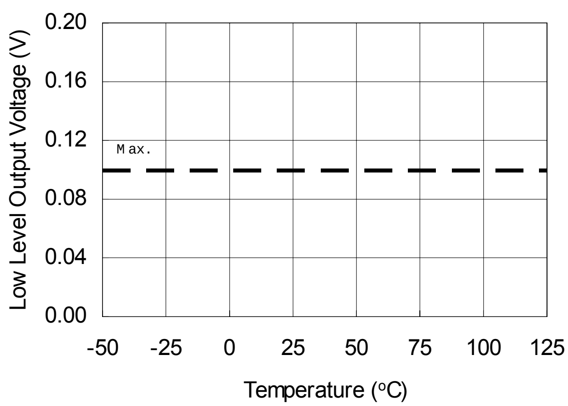


Figure 9A. Low Level Output vs.Temperature

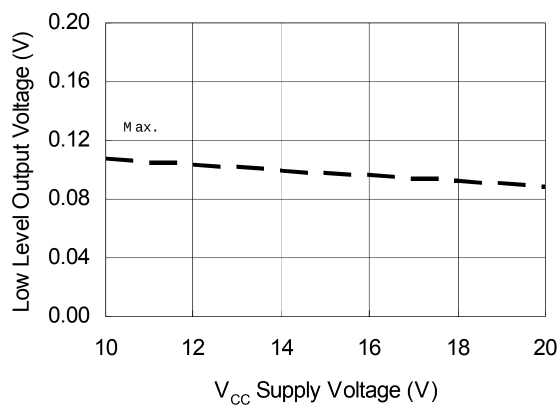


Figure 9B. Low Level Output vs. Supply Voltage

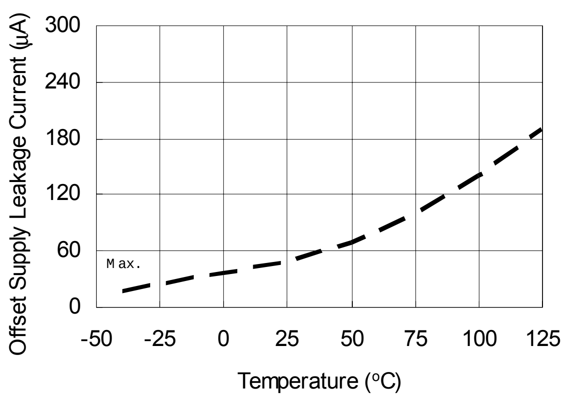


Figure 10A. Offset Supply Leakage Current vs. Temperature

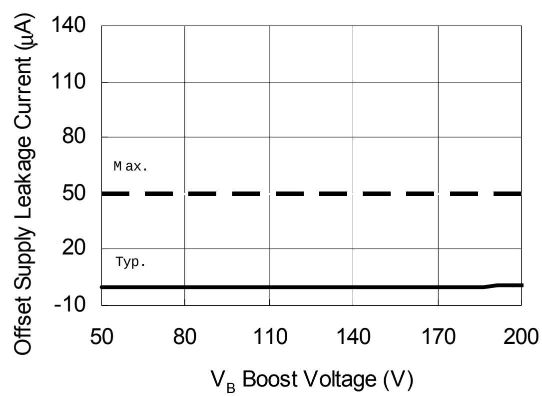


Figure 10A. Offset Supply Leakage Current vs. Temperature

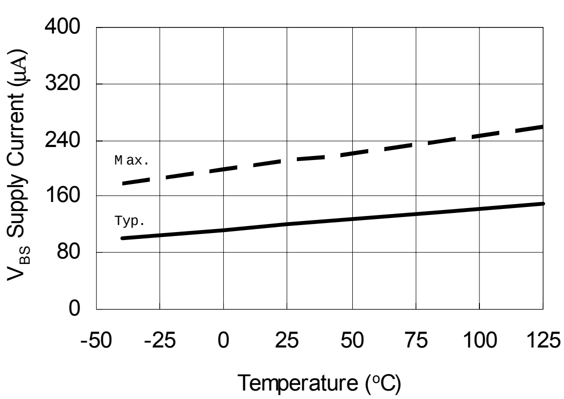


Figure 11A. V_{BS} Supply Current vs. Temperature

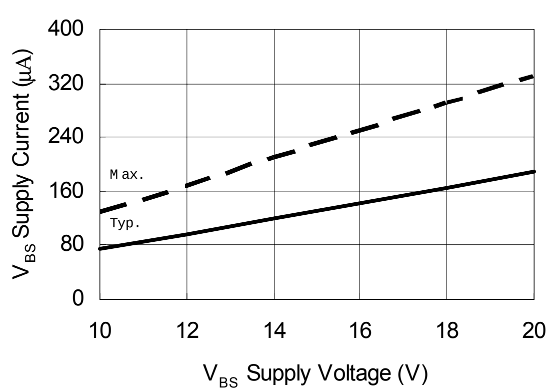


Figure 11B. V_{BS} Supply Current vs. Supply Voltage

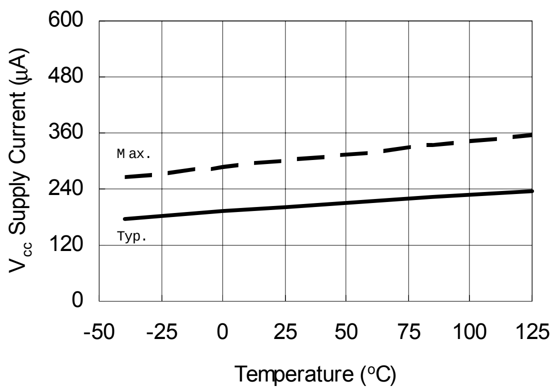


Figure 12A. V_{CC} Supply Current vs. Temperature

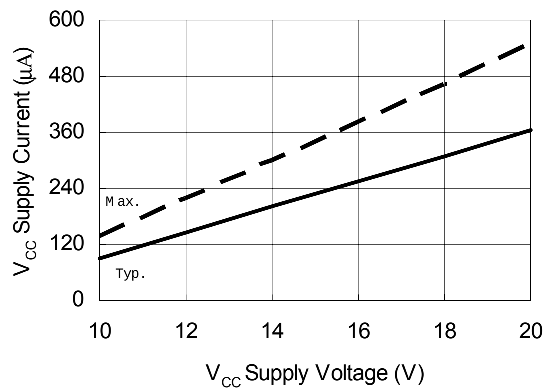


Figure 12B. V_{CC} Supply Current vs. Supply Voltage

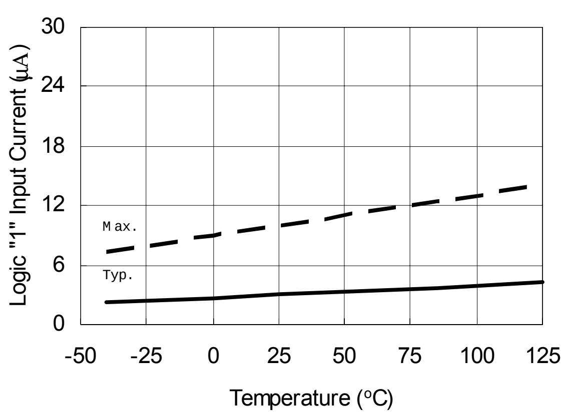


Figure 13A. Logic "1" Input Current vs. Temperature

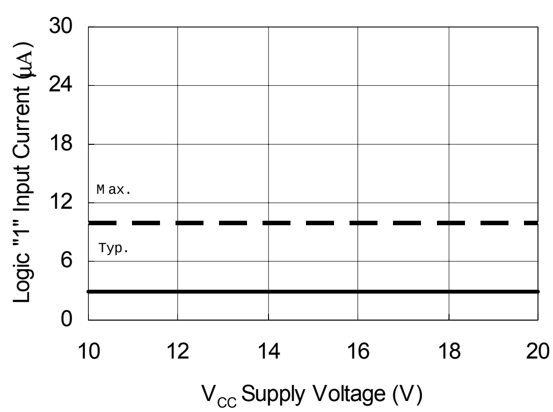


Figure 13B. Logic "1" Input Current vs. Supply Voltage

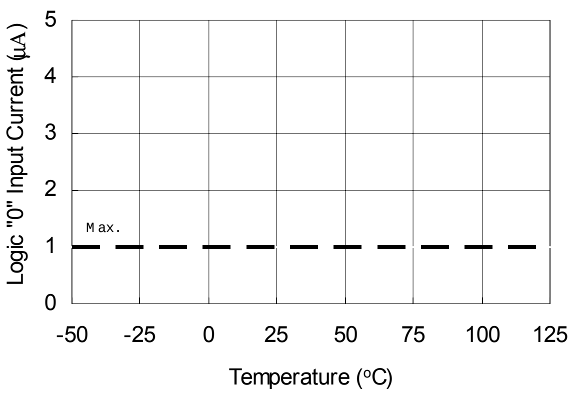


Figure 14A. Logic "0" Input Current vs. Temperature

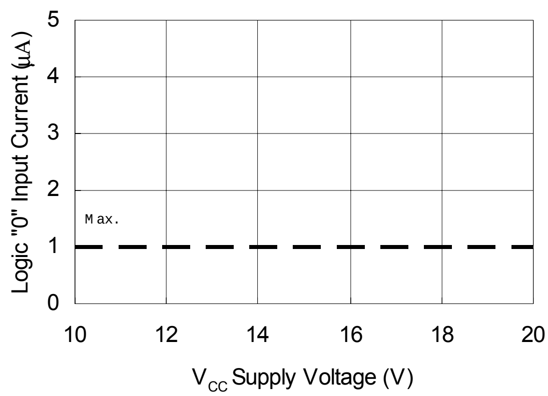


Figure 14B. Logic "0" Input Current vs. Supply Voltage

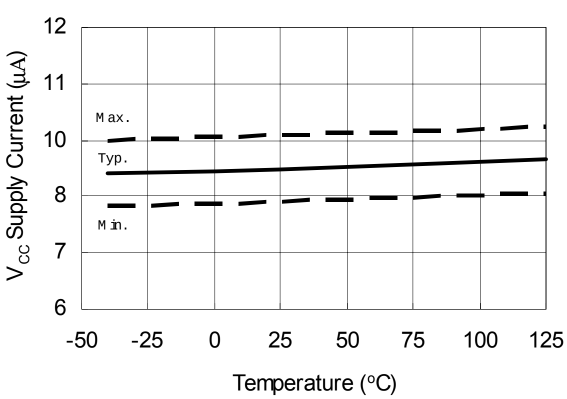


Figure 15. V_{CC} Undervoltage Threshold (+) vs. Temperature

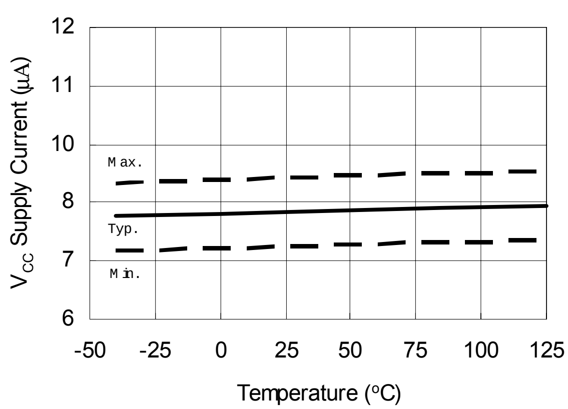


Figure 16. V_{CC} Undervoltage Threshold (-) vs. Temperature

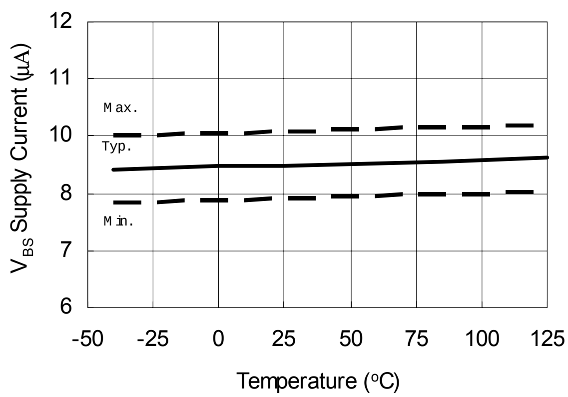


Figure 17. V_{BS} Undervoltage Threshold (+) vs. Temperature

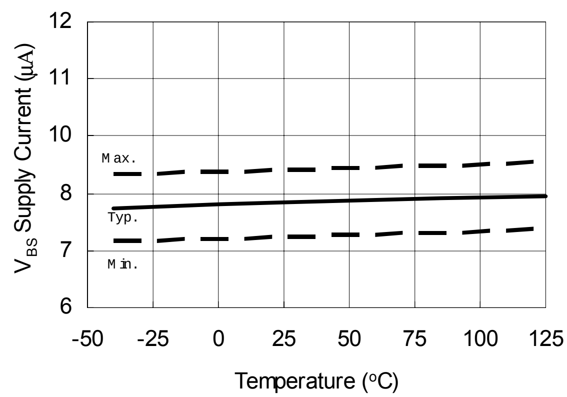


Figure 18. V_{BS} Undervoltage Threshold (-) vs. Temperature

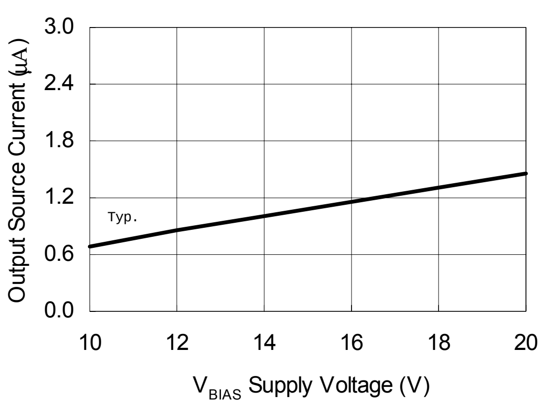


Figure 19. Output Source Current vs. Supply Voltage

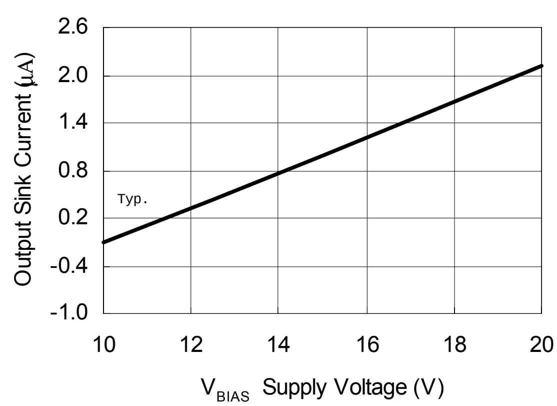


Figure 20. Output Sink Current vs. Supply Voltage

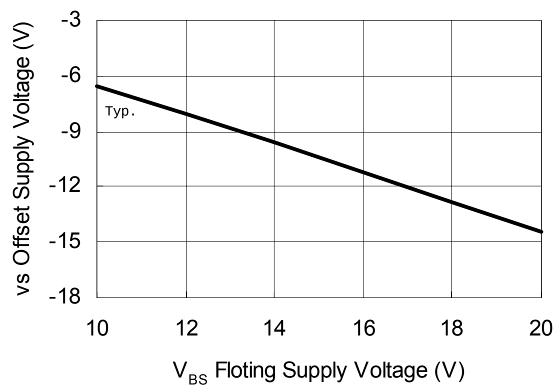


Figure 21. Maximum VS Negative Offset vs. Supply Voltage

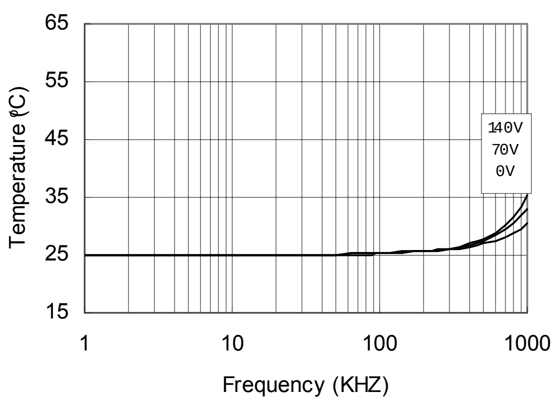


Figure 22. IRS2011s vs. Frequency (IRFBC20)
R_{gate}=33Ω , V_{CC}=12V

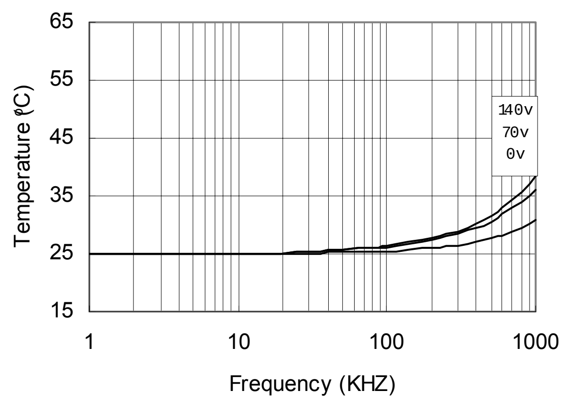


Figure 23. IRS2011s vs. Frequency (IRFBC30)
R_{gate}=22 , V_{CC}=12V

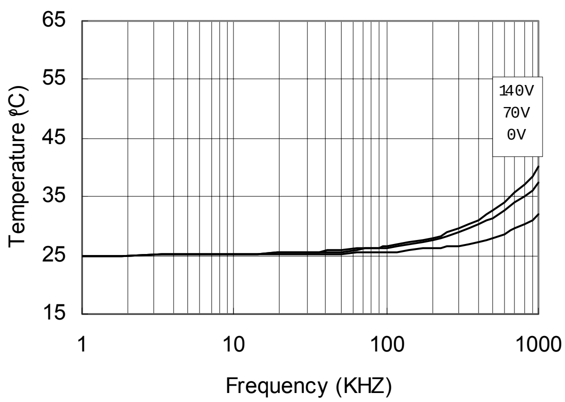


Figure 24. IRS2011s vs. Frequency (IRFBC40)
R_{gate}=15 , V_{CC}=12V

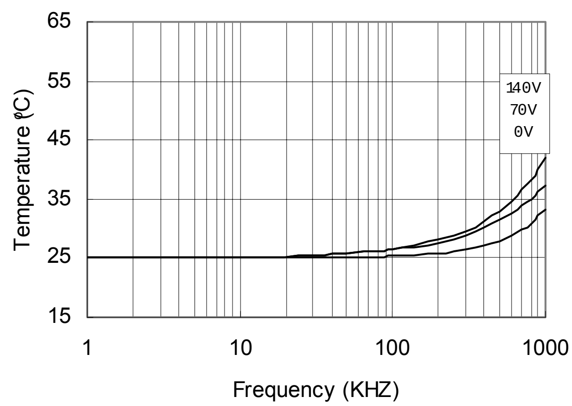


Figure 25. IRS2011s vs. Frequency (IRFB23N15D)
R_{gate}=10 , V_{CC}=12V

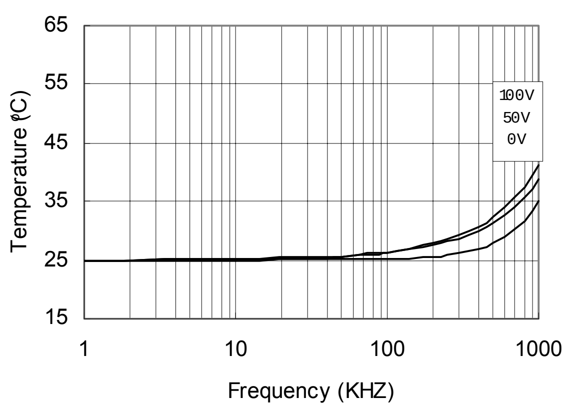
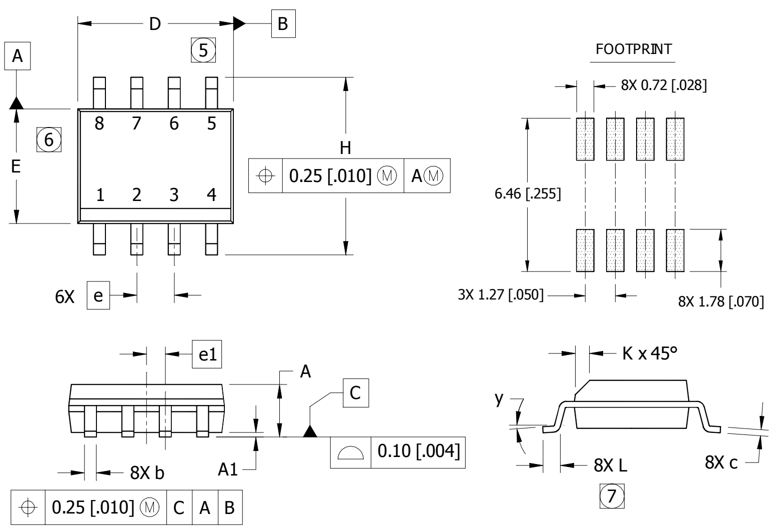


Figure 26. IRS2011s vs. Frequency (IRFB4212)
R_{gate}=10 , V_{CC}=12V

Case outlines



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

8-Lead SOIC

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas Street, El Segundo, California 90245 Tel: (310) 252-7105