True Bipolar Input, Dual 1µs, 12-Bit, 2-Channel SAR ADC

Preliminary Technical Data

AD7366

FEATURES

Dual 12-bit, 2-channel ADC
True Bipolar Analog Inputs
Programmable Input Ranges
±10, ±5, 0 to 10 V
Throughput rate: 1 MSPS
Simultaneous conversion with read in less than 1µs
Specified for V_{CC} of 5 V±5%
Low current consumption: 5.65 mA max
Wide input bandwidth
70 dB SNR at 50 kHz input frequency
On-chip reference: 2.5 V
–40°C to +85°C operation
High speed serial interface
SPI®/QSPI™/MICROWIRE™/DSP compatible
***i*CMOS™ Process Technology**
24-lead TSSOP package
For 14 bit version see AD7367

GENERAL DESCRIPTION

The AD7366[1] is a dual, 12-bit, high speed, low power, successive approximation ADC that features throughput rates up to 1 MSPS. The device contains two ADCs, each preceded by a 2-channel multiplexer, and a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 10 MHz.

The AD7366 is fabricated on Analog Devices' Industrial CMOS process, *i*CMOS, a technology platform combining the advantages of low and high voltage CMOS, bipolar and high voltage DMOS processes. The process allows the AD7366 to accept high voltage bipolar signals in addition to reducing power consumption and package size. The AD7366 can accept true bipolar analog input signals in the ±10 V range, ±5 V range and 0 to 10 V range.

The AD7366 has an on-chip 2.5 V reference that can be overdriven if an external reference is preferred. The AD7366 is available in a 24-lead TSSOP package.

*i*CMOS™ Process Technology
For analog systems designers within industrial/instrumentation equipment OEMs who need high performance ICs at higher-voltage levels, *i*CMOS is a technology platform that enables the development of analog ICs capable of 30V and operating at +/- 15V supplies while allowing dramatic reductions in power consumption and package size, and increased AC and DC performance.

FUNCTIONAL BLOCK DIAGRAM

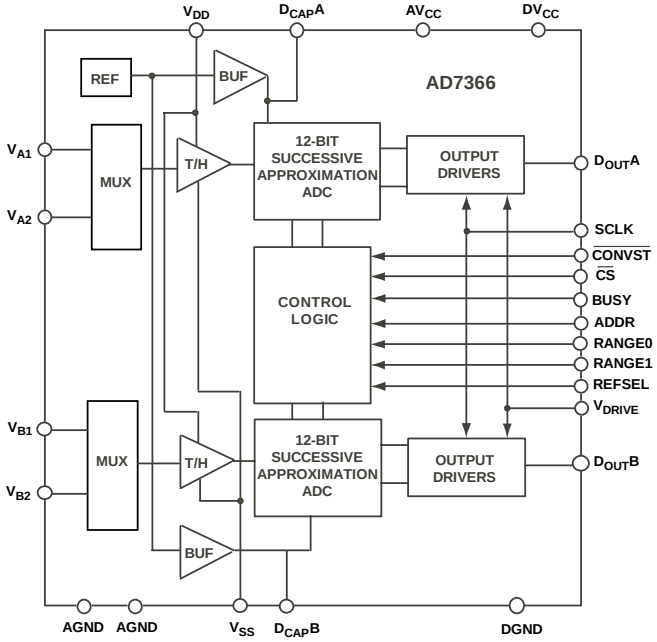

Figure 1

Table 1.Related Products

Device Number	Resolution	Throughput Rate	Number of Channels
AD7367	14-Bit	1 MSPS	Dual, 2-ch
AD7366-5	12-Bit	500 KSPS	Dual, 2-ch
AD7367-5	14-Bit	500 KSPS	Dual, 2-ch

[1]Protected by U.S. Patent No. 6,681,332.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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SPECIFICATIONS

AV_{CC} = DV_{CC} =4.75 V to 5.25 V, V_{DD} = 11.5 V to 16.5 V, V_{SS} = -11.5 V to −16.5 V, V_{DRIVE} = 2.7 V to 5.25V, f_{SAMPLE} = 1.12MSPS, f_{SCLK} = 48MHz, V_{REF} = 2.5 V Internal/External; T_A = T_{MIN} to T_{MAX}, unless otherwise noted[1].

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/ Comments
DYNAMIC PERFORMANCE					f_{IN} = 50 kHz sine wave;
Signal-to-Noise Ratio (SNR)[2]	71			dB	
Signal-to-Noise + Distortion Ratio (SINAD)[2]	70			dB	
Total Harmonic Distortion (THD)[2]			-77	dB	
Spurious Free Dynamic Range (SFDR)[2]			-75	dB	
Intermodulation Distortion (IMD)[2]					fa = 49 kHz, fb = 51 kHz
Second Order Terms		-88		dB	
Third Order Terms		-88		dB	
Channel-to-Channel Isolation[2]		-88		dB	
SAMPLE AND HOLD					
Aperture Delay[3]			10	ns	
Aperture Jitter[3]		40		ps	
Aperture Delay Matching[3]		100		ps	
Full Power Bandwidth		50		MHz	@ 3 dB, ±10 V range
		15		MHz	@ 0.1 dB, ±10 V range
DC ACCURACY					
Resolution	12			Bits	
Integral Nonlinearity[2]			±1	LSB	
Differential Nonlinearity[2]			±0.99	LSB	Guaranteed no missed codes to 12 bits
Positive Full Scale Error[2]			±2	LSB	
Positive Full Scale Error Match[2]		±0.5		LSB	
Zero Code Error[2]			±5	LSB	
Zero Code Error Match[2]		±1		LSB	
Negative Full Scale Error[2]			±2	LSB	
Negative Full Scale Error Match[2]		±0.5		LSB	
ANALOG INPUT					
Input Voltage Ranges			±10	V	V_{DD} = +11.5V min, V_{SS} = −11.5V min, V_{CC} = 4.75V to 5.25V
(Programmed via RANGE Pins)			±5	V	V_{DD} = +11.5V min, V_{SS} = −11.5V min, V_{CC} = 4.75V to 5.25V
			0 to 10V	V	V_{DD} = +11.5V min, V_{SS} = -11.5 min, V_{CC} = 4.75V to 5.25V
DC Leakage Current			±1	µA	
Input Capacitance		12		p	When in track, ±10 V range
		15		pF	When in track, ±5 V or 0 to 10 V range
		3		pF	When in hold
Input impedance		260		KΩ	For ±10V @1.12 Msps
		2.3		MΩ	For ±10V @100 Ksps
		125		KΩ	For ±5 / 0-10V @1.12 Msps
		1.1		MΩ	For ±5 / 0-10V @100Ksps

Parameter	Min	Typ	Max	Unit	Test Conditions/ Comments
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[4]	2.5		2.5	V	±0.2% max @ 25°C
Reference Input Voltage Range	+2.5		3.0	V	
DC Leakage Current			±1	µA	External reference applied to Pin $V_{REF}A$/Pin $V_{REF}B$
Input Capacitance		25		pF	
$V_{REF}A$, $V_{REF}B$ Output Impedance		8		Ω	
Reference Temperature Coefficient			20	ppm/°C	
		10		ppm/°C	
V_{REF} Noise		20		μV_{RMS}	
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7× V_{DRIVE}			V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{IN}			±1	µA max	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]		5		pF typ	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current			±1	µA	
Floating State Output Capacitance[3]		10		pF	
CONVERSION RATE					
Conversion Time			610	ns	
Track/Hold Acquisition Time[3]			140	ns	Full-scale step input;
Throughput Rate			1.12	MSPS	For 4.75V≤V_{DRIVE}≤5.25V, f_{SCLK} = 48MHz
		1		MSPS	For 2.7V≤V_{DRIVE}<4.75V , f_{SCLK} = 35MHz
POWER REQUIREMENTS					Digital I/Ps = 0 V or V_{DRIVE}
V_{CC}	4.75		5.25	V	See Table 6
V_{DD}	+11.5		+16.5	V	See Table 6
V_{SS}	-16.5		-11.5	V	See Table 6
V_{DRIVE}	2.7		5.25	V	
Normal Mode (Static)					
I_{DD}			1	µA	V_{DD} = +16.5 V
I_{SS}			1	µA	V_{SS} = −16.5 V
I_{CC}			1.8	mA	V_{CC} = 5.5 V
Normal Mode (Operational)					f_s = 1.12 MSPS
I_{DD}			925	µA	V_{DD} = +16.5 V
I_{SS}			725	µA	V_{SS} = −16.5 V
I_{CC}			4	mA	V_{CC} = 5.25 V, internal reference enabled
Shut-Down Mode					
I_{DD}			1	µA	V_{DD} = +16.5 V
I_{SS}			1	µA	V_{SS} = −16.5 V
I_{CC}			1	µA	V_{CC} = 5.25 V
Power Dissipation					
Normal Mode (Operational)			48.23	mW	V_{DD} = +16.5V, V_{SS} = −16.5V, V_{CC} = 5.25V
Shut-Down			15	µW	V_{DD} = +5V, V_{SS} = −5V, V_{CC} = 5V
Shut-Down			38.25	µW	V_{DD} = +16.5V, V_{SS} = −16.5V, V_{CC} = 5.25

[1] Temperature range is −40°C to +85°C
[2] See Terminology section.

[3] Sample tested during initial release to ensure compliance.
[4] Refers to pins $V_{REF}A$ or $V_{REF}B$.

TIMING SPECIFICATIONS

AV_{CC} = DV_{CC} =4.75 V to 5.25 V, V_{DD} = 11.5 V to 16.5 V, V_{SS} = −11.5 V to −16.5 V, V_{DRIVE} = 2.7 V to 5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted[1].

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Test Conditions / Comments
	2.7V≤V_{DRIVE}<4.75V	4.75V≤V_{DRIVE}≤5.25V		
$t_{CONVERT}$	610	610	ns max	Conversion time, Internal clock. $\overline{CONVST}$ falling edge to BUSY falling edge
f_{SCLK}	10	10	kHz min	Frequency of serial read clock.
	35	48	MHz max	
t_{QUIET}	30	30	ns min	Minimum quiet time required between end of serial read and start of next conversion
t_1	10	10	ns min	Minimum $\overline{CONVST}$ Low pulse.
t_2	5	5	ns min	$\overline{CONVST}$ falling edge to BUSY rising edge.
t_3	0	0	ns min	BUSY falling edge to MSB valid once $\overline{CS}$ is low for t_4 prior to BUSY going Low
t_4	10	10	ns max	Delay from $\overline{CS}$ falling edge until DOUTA and DOUTB are three-state disabled
t_5[2]	20	14	ns max	Data access time after SCLK falling edge
t_6	5	5	ns min	SCLK to data valid hold time
t_7	0.1 t_{SCLK}	0.1 t_{SCLK}	ns min	SCLK low pulse width
t_8	0.1 t_{SCLK}	0.1 t_{SCLK}	ns min	SCLK high pulse width
t_9	10	10	ns max	$\overline{CS}$ rising edge to DOUTA, DOUTB, high impedance
t_{10}	5	5	ns min	SCLK falling edge to DOUTA, DOUTB, high impedance
	10	10	ns max	SCLK falling edge to DOUTA, DOUTB, high impedance
$t_{POWER-UP}$	70	70	µs	Power up time from shutdown mode. Time required between $\overline{CONVST}$ rising edge and $\overline{CONVST}$ falling edge.

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used. See Terminology section and Figure 9.

[2] The time required for the output to cross 0.4 V or 2.4 V.

ABSOLUTE MAXIMUM RATINGS

Table 4

Parameter	Rating
V_{DD} to AGND, DGND	−0.3 V to +16.5 V
V_{SS} to AGND, DGND	−0.3 V to +16.5 V
V_{DRIVE} to DGND	−0.3 V to DV_{DD}
V_{DD} to AVcc	Vcc – 0.3V to +16.5V
AV_{CC} to AGND, DGND	-0.3V to +7V
DV_{CC} to AV_{CC}	-0.3 V to + 0.3V
DV_{CC} to DGND	-0.3 V to + 7V
V_{DRIVE} to AGND	−0.3 V to DV_{CC}
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	V_{SS} −0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
V_{REF}A, V_{REF}B input to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	128°C/W
θ_{JC} Thermal Impedance	42°C/W
Pb-free Temperature, Soldering Reflow	260(+0)°C
ESD	TBD kV

[1] Transient currents of up to 100 mA will not cause latch up.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

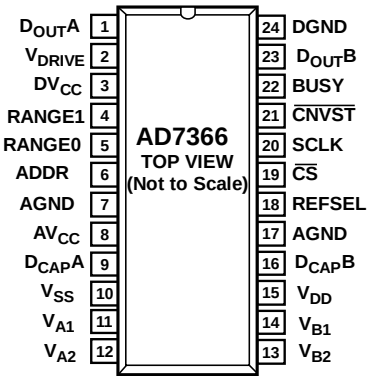


Figure 2 24-Lead RU-24.

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 23	$D_{OUT}A$, $D_{OUT}B$	Serial Data Outputs. The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input and 12 SCLK cycles are required to access the data. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data stream consists of the 12 bits of conversion data and is provided MSB first. If $\overline{CS}$ is held low for a further 12 SCLK cycles on either $D_{OUT}A$ or $D_{OUT}B$, the data from the other ADC follows on the D_{OUT} pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either $D_{OUT}A$ or $D_{OUT}B$ using only one serial port. See the Serial Interface section.
2	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface will operate. This pin should be decoupled to DGND. The voltage range on this pin is 2.7V to 5.25V and may be different to that at AV_{CC} and DV_{CC} but should never exceed either by more than 0.3V. To achieve a throughput rate of 1.12Msps V_{DRIVE} must be greater than or equal to 4.75V
3	DV_{CC}	Digital Supply Voltage, 4.75V to 5.25V. The DV_{CC} and AV_{CC} voltages should ideally be at the same potential. For best performance it is recommended that DV_{CC} and AV_{CC} pins be shorted together, to ensure the voltage difference between them never exceed 0.3 V even on a transient basis. This supply should be decoupled to DGND. 10 µF and 100 nF decoupling capacitors should be placed on the DV_{CC} pin.
4,5	RANGE0, RANGE1	**Analog Input Range Selection. Logic inputs. The polarity on these pins determines the input range of the analog input channels. See Analog Inputs section and** Table 7 for details
6	ADDR	Multiplexer Select. Logic input. This input is used to select the pair of channels to be simultaneously converted, either Channel 1 of both ADC A and ADC B, or Channel 2 of both ADC A and ADCB. The logic state on this pin is latched on the rising edge of BUSY to set up the multiplexer for the *next* conversion.
7,17	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7366. All analog input signals and any external reference signal should be referred to this AGND voltage. Both AGND pins should connect to the AGND plane of a system. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
8	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for the ADC cores. The AV_{CC} and DV_{CC} voltages ideally should be at the same potential. For best performance it is recommended that DV_{CC} and AV_{CC} pins be shorted together, to ensure the voltage difference between them never exceed 0.3 V even on a transient basis. This supply should be decoupled to AGND. 10 µF and 100 nF decoupling capacitors should

		be placed on the AV_{CC} pins.
9,16	$D_{CAP}A$,$D_{CAP}B$	Decoupling Capacitor Pins. Decoupling capacitors are connected to these pins to decouple the reference buffer for each respective ADC. For best performance it is recommended to use 680nF decoupling capacitor on these pins. Provided the output is buffered, the on-chip reference can be taken from these pins and applied externally to the rest of a system.
10	V_{SS}	Negative power supply voltage. This is the negative supply voltage for the Analog Input section. The supply must be less than a maximum voltage of -11.5V for all input ranges. See Table 6 for further details. 10 µF and 100 nF decoupling capacitors should be placed on the V_{SS} pin.
11,12	V_{A1}, V_{A2}	Analog Inputs of ADC A. These are both single-ended analog inputs. The Analog input range on these channels is determined by the RANGE0 and RANGE1 pins.
13,14	V_{B2}, V_{B1}	Analog Inputs of ADC B. These are both single-ended analog inputs. The Analog input range on these channels is determined by the RANGE0 and RANGE1 pins.
15	V_{DD}	Positive power supply voltage. This is the positive supply voltage for the Analog Input section. The supply must be greater than a minimum voltage of 11.5V for all the analog input ranges. See Table 6 for further details. 10 µF and 100 nF decoupling capacitors should be placed on the V_{DD} pin.
18	REFSEL	Internal/External Reference Selection. Logic input. If this pin is tied to a logic high, the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. In addition, Pin $D_{CAP}A$ and Pin $D_{CAP}B$ must be tied to decoupling capacitors. If the REF SELECT pin is tied to GND, an external reference can be supplied to the AD7366 through the $D_{CAP}A$ and/or $D_{CAP}B$ pins.
19	$\overline{CS}$	Chip Select. Active low logic input. This input frames the serial data transfer. When $\overline{CS}$ is logic low the output bus is enabled and the conversion result is output on $D_{OUT}A$, and $D_{OUT}B$.
20	SCLK	Serial Clock. Logic input. A serial clock input provides the SCLK for accessing the data from the AD7366.
21	$\overline{CONVST}$	Conversion Start. Edge triggered logic input. On the falling edge of this input the track/hold goes into hold mode and conversion is initiated. If $\overline{CONVST}$ is low at the end of a conversion, the part goes into power-down mode. In this case, the rising edge of $\overline{CONVST}$ will instruct the part to power up again.
22	BUSY	BUSY Output. Transitions high when a conversion is started and remains high until the conversion is complete.
24	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7366. The DGND pin should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.

TERMINOLOGY

Differential Nonlinearity
Differential nonlinearity is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity
Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a single (1) LSB point below the first code transition and full scale, a point 1 LSB above the last code transition.

Zero Code Error
It is the deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, i.e., AGND – 1/2 LSB for bipolar ranges and $2\times V_{REF}-1$LSB for the unipolar range.

Positive Full Scale Error
It is the deviation of the last code transition (011…110) to (011…111) from the ideal ($+4 \times V_{REF}$ - 1 LSB or + 2 x V_{REF} – 1 LSB) after the Zero Code Error has been adjusted out.

Negative Full Scale Error
This is the deviation of the first code transition (10…000) to (10…001) from the ideal (i.e., - 4 x V_{REF} + 1 LSB, - 2 x V_{REF} + 1 LSB or AGND + 1LSB) after the Zero Code Error has been adjusted out.

Zero Code Error Match
This is the difference in zero code error across all 12 channels.

Positive Full Scale Error Match
This is the difference in positive full scale error across all channels.

Negative Full Scale Error Match
This is the difference in negative full scale error across all channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This ratio is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ \text{dB}$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7366, it is defined as:

$$THD(dB) = 20\log\frac{\sqrt{V_2^{\,2}+V_3^{\,2}+V_4^{\,2}+V_5^{\,2}+V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic, or spurious noise, is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels when operating in the +/-10 V Range. It is measured by applying a full-scale, 150 kHz sine wave signal to all unselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. The figure given is the worst-case across all four channels for the AD7366. See also Typical Performance Characteristics.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum, and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7366 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order

terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PSRR (Power Supply Rejection)
Variations in power supply affect the full-scale transition but not the converter's linearity. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see figure x).

THEORY OF OPERATION

Circuit Information

The AD7366 is a fast, dual, 2-Channel, 12-bit, Bipolar Input, Serial A/D converter. The AD7366 can accept bipolar input ranges of ±10V and ±5V. It can also accept a 0 to 10V unipolar input range. The AD7366 requires V_{DD} and V_{SS} dual supplies for the high voltage analog input structure. These supplies must be equal to or greater than 11.5V. See Table 6 for the minimum requirements on these supplies for each Analog Input Range. The AD7366 requires a low voltage 4.75V to 5.25 V V_{CC} supply to power the ADC core.

Table 6. Reference and Supply Requirements for each Analog Input Range

Selected Analog Input Range (V)	Reference Voltage (V)	Full Scale Input Range(V)	AV_{CC} (V)	Minimum V_{DD}/V_{SS} (V)
±10	2.5	±10	5	±11.5
	3.0	±12	5	±12
± 5	2.5	±5	5	±11.5
	3.0	±6	5	±11.5
0 to 10	2.5	0 to 10	5	±11.5
	3.0	0 to 12	5	±12

The AD7366 contains two on-chip differential track-and-hold amplifiers, two successive approximation A/D converters, and a serial interface with two separate data output pins. It is housed in a 24-lead TSSOP package, offering the user considerable space-saving advantages over alternative solutions. The AD7366 requires a $\overline{\text{CONVST}}$ signal to start conversion. On the falling edge of $\overline{\text{CONVST}}$ both track-and-holds will be placed into hold mode and the conversions are initiated. The BUSY signal will go high to indicate the conversions are taking place. The clock source for each successive approximation ADC is provided by an internal oscillator. The BUSY signal will go low to indicate the end of conversion. On the falling edge of BUSY the track-and-hold will return to track mode. Once the conversion is finished, the serial clock input accesses data from the part.

The AD7366 has an on-chip 2.5 V reference that can be overdriven when an external reference is preferred. If the internal reference is to be used elsewhere in a system, then the output from $D_{CAP}A$ & $D_{CAP}B$ must first be buffered. On Power up the REFSEL pin must be tied to either a high or low logic state to select either the internal or external reference option. If the internal reference is the preferred option, the user must tie the REFSEL pin logic high. Alternatively, if REFSEL is tied to GND then an external reference can be supplied to both ADC's through $D_{CAP}A$ & $D_{CAP}B$ pins.

The analog inputs are configured as two single ended inputs for each ADC. The various different input voltage ranges can be selected by programming the RANGE bits as shown in Table 7.

Converter Operation

The AD7366 has two successive approximation analog-to-digital converters, each based around two capacitive DACs. Figure 3 and Figure 4 show simplified schematics of one of these ADCs in acquisition and conversion phase, respectively. The ADC is comprised of control logic, a SAR, and two capacitive DACs. In Figure 3 (the acquisition phase), SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the signal on the input.

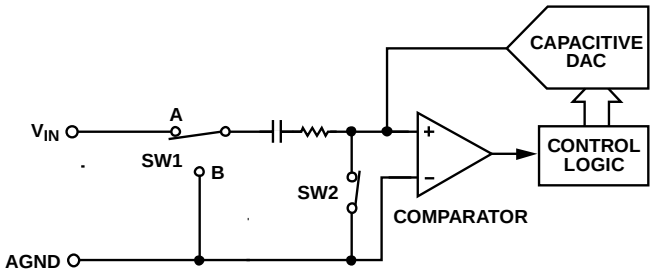


Figure 3 ADC Acquisition Phase

When the ADC starts a conversion (Figure 4), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code.

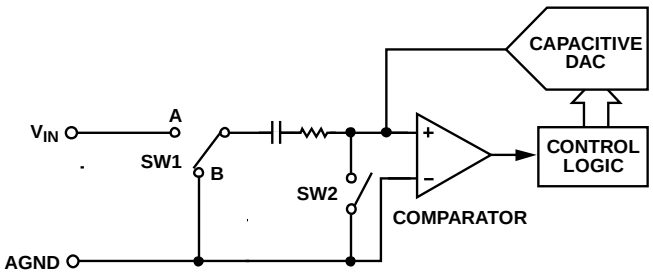


Figure 4 ADC Conversion Phase

ANALOG INPUTS

Each ADC in the AD7366 has two Single Ended Analog Inputs. Figure 5 shows the equivalent circuit of the analog input structure of the AD7366. The two diodes provide ESD protection. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and starts conducting current into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part. Capacitor C1 in Figure 5 is typically 5 pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about TBD Ω. Capacitor C2 is the ADC's sampling capacitors with a capacitance of approximately TBDpF for the ±10V input range and approximately TBDpF for all other input ranges.

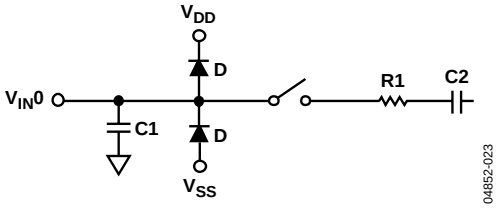


Figure 5 Equivalent Analog Input Structure

The AD7366 can handle true bipolar input voltages. The Analog input can be set to one of three ranges; ±10V, ±5V, 0-10V. The logic levels on pins RANGE0 and RANGE1 determine which input range is selected as outlined in

Table 7. These range bits should not be changed during the acquisition time prior to a conversion but may change at any other time.

Table 7. Analog Input Range Selection

RANGE1	RANGE0	Range Selected
0	0	±10V
0	1	±5V
1	0	0 to 10V
1	1	Do not program

The AD7366 requires V_{DD} and V_{SS} dual supplies for the high voltage analog input structures. These supplies must be equal to or greater than ±11.5V. See Table 6 for the requirements on these supplies. The AD7366 requires a low voltage 4.75V to 5.25V AV_{CC} supply to power the ADC core, a 4.75V to 5.25V DV_{CC} supply for the Digital Power and a 2.7V to 5.25V V_{DRIVE} supply for the interface power.

Channel selection is made via the ADDR pin as shown in Table 8. The logic level on the ADDR pin is latched on the rising edge of BUSY for the *next* conversion, not the one in progress. When power is first supplied to the AD7366 the default channel selection will be V_{A1} and V_{B1}.

Table 8. Channel Selection

ADDR	Channels Selected
0	V_{A1}, V_{B1}
1	V_{A2}, V_{B2}

Transfer Function

The AD7366 output coding is two's complement. The designed code transitions occur at successive integer LSB values (i.e. 1 LSB, 2 lSB, and so on). The LSB size is dependant on the analog input range selected.

Table 9 LSB sizes for each Analog Input Range.

Input Range	Full Scale Range/4096	LSB Size
±10 V	20 V/4096	4.88mV
±5 V	10 V/4096	2.44mV
0 to 10 V	10V/4096	2.44mV

The ideal transfer characteristic is shown in Figure 6

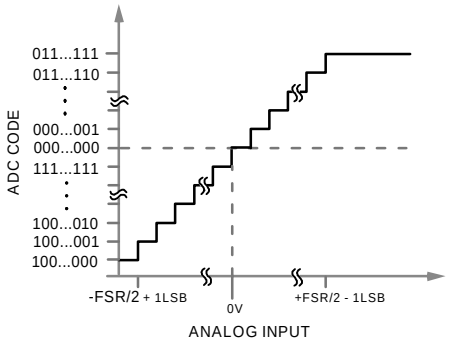


Figure 6.Transfer Characteristic

V_{DRIVE}

The AD7366 also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7366 was operated with a V_{CC} of 5 V, the V_{DRIVE} pin could be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors. Thus, the AD7366 could be used with the ±10 V input range while still being able to interface to 3 V digital parts.

To achieve the maximum throughput rate of 1.12Msps V_{DRIVE} must be greater than or equal to 4.75V, see table 3. The maximum throughput rate for the AD7366 with the V_{DRIVE} voltage set to less than 4.75 and greater than 2.7 is 1 Msps.

REFERENCE

The AD7366 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The logic state of the REFSEL pin determines whether the internal reference is used. The internal reference is selected for both ADC when the REFSEL pin is tied to logic high. If the REFSEL pin is tied to GND then an external reference can be supplied through the $D_{CAP}A$ and $D_{CAP}B$ pins. On power-up, the REFSEL pin must be tied to either a low or high logic state for the part to operate. Suitable reference sources for the AD7366 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When operating the AD7366 in internal reference mode, the 2.5 V internal reference is available at $D_{CAP}A$ and $D_{CAP}B$ pins, which should be decoupled to AGND using a 680nF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system. The internal reference is capable of sourcing up to 150 µA with an analog input range of ±10 and 60 µA for both the ±5V and 0-10V ranges.

If the internal reference operation is required for the ADC conversion, the REFSEL pin must be tied to logic high on power-up. The reference buffer requires 500 µs to power up and charge the 680nF decoupling capacitor during the power-up time.

The AD7366 is specified for a 2.5 V to 3 V reference range. When a 3V reference is selected, the ranges are ±12 V, ±6 V, and 0 V to +12 V. For these ranges, the V_{DD} and V_{SS} supply must be equal to or greater than the +12V &-12V respectively.

MODES OF OPERATION

The mode of operation of the AD7366 is selected by the (logic) state of the $\overline{\text{CONVST}}$ signal at the end of a conversion. There are two possible modes of operation: normal mode and shut-down mode. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

NORMAL MODE

This mode is intended for applications needing fast throughput rates since the user does not have to worry about any power-up times with the AD7366 remaining fully powered at all times. Figure 7 shows the general mode of operation of the AD7366 in this mode.

The conversion is initiated on the falling edge of $\overline{\text{CONVST}}$ as described in the Circuit Information section. To ensure that the part remains fully powered up at all times, $\overline{\text{CONVST}}$ must be at logic state high prior to the BUSY signal going low. If $\overline{\text{CONVST}}$ is at logic state low when the BUSY signal goes low, the analogue circuitry will power down and the part will cease converting. The BUSY signal remains high for the duration of the conversion. The $\overline{\text{CS}}$ pin must be brought low to bring the data bus out of three-sate, subsequently twelve serial clock cycles are required to read the conversion result. The D_{OUT} lines return to three-state when $\overline{\text{CS}}$ is brought high and not after 12 SCLK cycles has elapsed. If $\overline{\text{CS}}$ is left low for a further 12 SCLK cycles, the result from the other on chip ADC is also accessed on the same D_{OUT} line, as shown in Figure 10 (see the Serial Interface section)

Once 24 SCLK cycles have elapsed, the D_{OUT} line returns to three-state when $\overline{\text{CS}}$ is brought high and not on the 24th SCLK falling edge. If $\overline{\text{CS}}$ is brought high prior to this, the D_{OUT} line returns to three-state at that point. Thus, $\overline{\text{CS}}$ must be brought high once the read is completed, as the bus does not automatically return to three-state upon completion of the dual result read.

Once a data transfer is complete and $D_{OUT}A$ and $D_{OUT}B$ have returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{\text{CONVST}}$ low again.

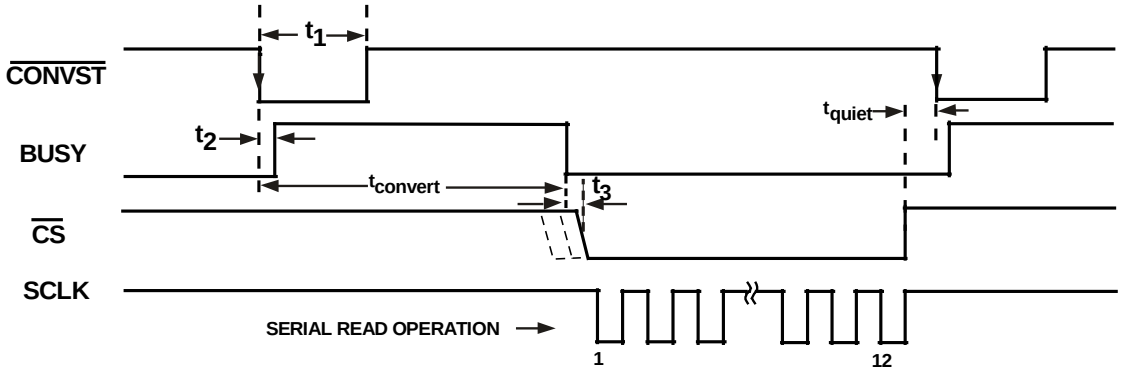


Figure 7. Normal Mode Operation

SHUT-DOWN MODE

This mode is intended for use in applications where slow throughput rates are required. This mode is suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus, shut-down. When the AD7366 is in full power-down, all analog circuitry is powered down. As already stated, the falling edge of $\overline{\text{CONVST}}$ initiates the conversion. The BUSY output subsequently goes high to indicate that the conversion is in progress. Once the conversion is completed, the BUSY output returns low. If the $\overline{\text{CONVST}}$ signal is at logic low when BUSY goes low then the part will enter shut-down at the end of the conversion phase. While the part is in shut-down mode the digital output code from the last conversion on each ADC can still be read from the D_{OUT} pins. To read the D_{OUT} data $\overline{\text{CS}}$ must be brought low as described in the Serial Interface Section. The D_{OUT} pins return to three-state once $\overline{\text{CS}}$ is brought back to logic high.

To exit full power-down and power up the AD7366, A rising edge of $\overline{\text{CONVST}}$ is required. After the required power up time has elapsed, $\overline{\text{CONVST}}$ may be brought low again to initiate another conversion, as shown in Figure 8 See the Power up time section for power-up times associated with the AD7366.

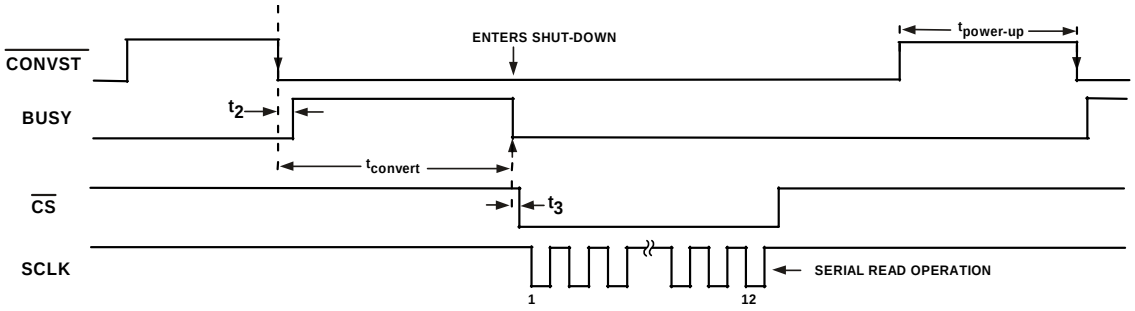


Figure 8. Auto-Shutdown Mode

POWER-UP TIMES

The AD7366 has one power down mode, which has already been described in detail. This section deals with the power-up time required when coming out of this modes. It should be noted that the power-up time, as explained in this section, applies with the recommended capacitors in place on the $D_{CAP}A$ and $D_{CAP}B$ pins. To power up from shut-down, $\overline{CONVST}$ must be brought high and remain high for a minimum of 100µs, as shown in Figure 8.

When power supplies are first applied to the AD7366, the ADC may power up with $\overline{CONVST}$ in either the low or high logic state. Before attempting a valid conversion $\overline{CONVST}$ must be brought high and remain high for the recommended power up time of 70µs, it can then be brought low to initiate a conversion.

With the AD7366 no dummy conversion is required before valid data can be read from the D_{OUT} pins. If it is intended to place the part in shut-down mode when the supplies are first applied, then the AD7366 must be powered up as explained about and a conversion initiated, but $\overline{CONVST}$ should remain in the logic low state and when the BUSY signal goes low thus the part enters shut-down.

Once supplies are applied to the AD7366, enough time must be allowed for any external reference to power up and charge the various reference buffer decoupling capacitors to their final values.

SERIAL INTERFACE

Figure 9 shows the detailed timing diagram for serial interfacing to the AD7366. On the falling edge of $\overline{CONVST}$ the AD7366 will simultaneously convert the selected channels. These conversions are performed using the on-chip oscillator. After the falling edge of $\overline{CONVST}$ the BUSY signal goes high, indicating the conversion has started. It returns low once the conversion has been completed. The data can now be read from the D_{OUT} pins.

$\overline{CS}$ and SCLK signals are required to transfer data from the AD7366. The AD7366 has two output pins corresponding to each ADC. Data can be read from the AD7366 using both $D_{OUT}A$ & $D_{OUT}B$, alternatively a single output pin of your choice can be used. The SCLK input signal provides the clock source for the serial interface. The $\overline{CS}$ goes low to access data from the AD7366. The falling edge of $\overline{CS}$ takes the bus out of three-state and clocks out the MSB of the conversion result. The data stream consists of 12 bits of data MSB first. The first bit of the conversion result is valid on the first SCLK falling edge after the $\overline{CS}$ falling edge. The subsequent 11 bits of data are clocked out on the falling edge of the SCLK signal. A minimum of 12 Clock pulses must be provided to AD7366 to access each conversion result. Figure 9 shows how a 12 SCLK read is used to access the conversion results.

On the rising edge of $\overline{CS}$, the conversion will be terminated and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is not brought high, but is instead held low for a further 12 SCLK cycles on either $D_{OUT}A$ or $D_{OUT}B$, the data from the other ADC follows on the D_{OUT} pin. This is illustrated in Figure 10 where the case for $D_{OUT}A$ is shown. In this case, the D_{OUT} line in use goes back into three-state on the rising edge of $\overline{CS}$

If the falling edge of SCLK coincides with the falling edge of $\overline{CS}$, then the falling edge of SCLK is not acknowledged by the AD7366, and the next falling edge of the SCLK will be the first registered after the falling edges of the $\overline{CS}$.

The $\overline{CS}$ pin can be brought low before the BUSY signal goes low to indicate the end of a conversion. The data bus is bought out of three-state by taking the $\overline{CS}$ pin low. This feature can be utilized to ensure that the MSB is valid on the falling edge of BUSY by bring $\overline{CS}$ low a minimum of t_4 nanoseconds before the BUSY signal goes low. The dotted $\overline{CS}$ line in Figure 7 illustrates this.

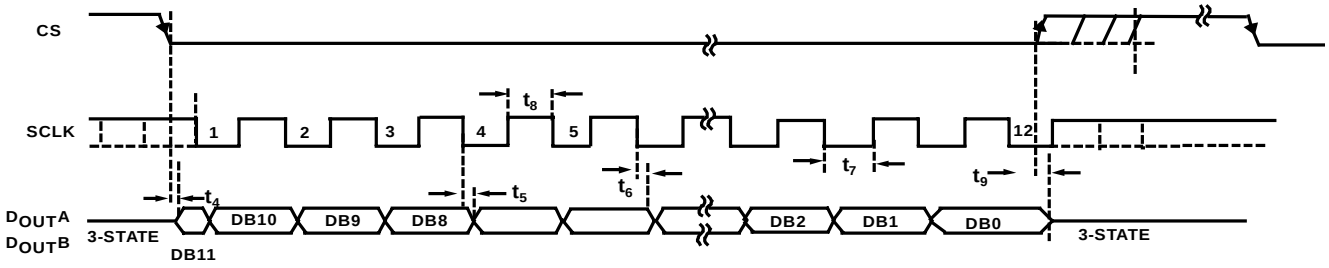


Figure 9. Serial Interface Timing diagram

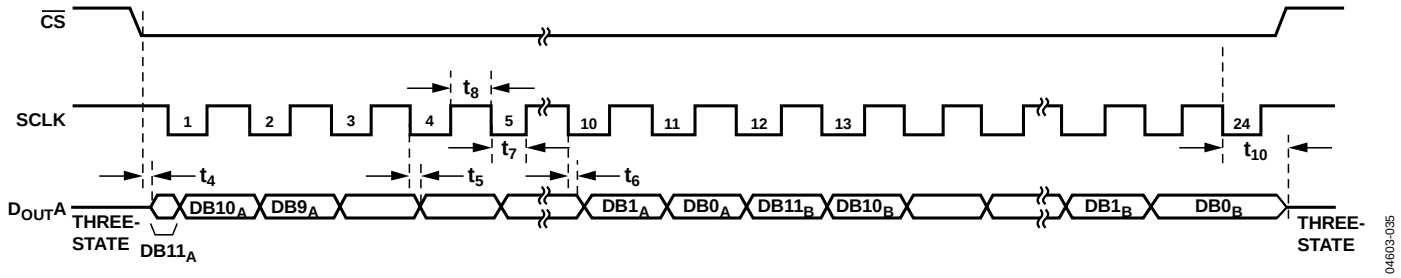
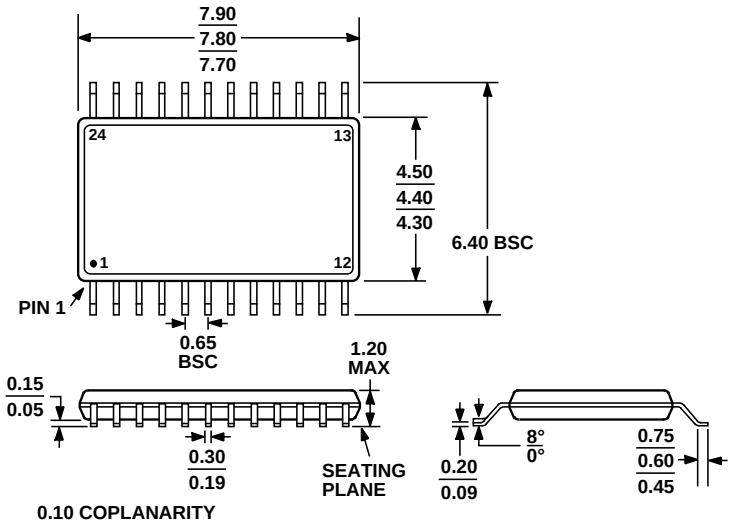


Figure 10. Reading Data from Both ADC's on ONE D_{OUT} Line with 28 SCLK's

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 11. 24-Lead TSSOP

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7366ARUZ[1]	−40°C to +85°C	Thin Shrink Small Outline Package	RU-24
AD7366ARUZ-REEL7[1]	−40°C to +85°C	Thin Shrink Small Outline Package	RU-24
AD7366BRUZ[1]	−40°C to +85°C	Thin Shrink Small Outline Package	RU-24
AD7366BRUZ-REEL7[1]	−40°C to +85°C	Thin Shrink Small Outline Package	RU-24
AD7366-5ARUZ[1]	−40°C to +85°C	Thin Shrink Small Outline Package	RU-24
AD7366-5ARUZ-REEL7[1]	−40°C to +85°C	Thin Shrink Small Outline Package	RU-24
AD7366-5BRUZ[1]	−40°C to +85°C	Thin Shrink Small Outline Package	RU-24
AD7366-5BRUZ-REEL7[1]	−40°C to +85°C	Thin Shrink Small Outline Package	RU-24

[1] Z = Pb-free part.

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