MPC8347EA PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications

The MPC8347EA contains a PowerPC™ processor core (built on Power Architecture™ technology) with system logic for networking, storage, and general-purpose embedded applications. For functional characteristics of the processor, refer to the *MPC8349EA PowerQUICC™ II Pro Integrated Host Processor Reference Manual*, Rev. 0.

To locate published errata or updates for this document, contact your Freescale sales office.

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for devices with part numbers ending in A or B, such as the MPC8347EA or MPC8347EB). For information on revision 1.1 silicon and earlier versions (*MPC8347E/MPC8347*), see the *PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications.*

See Section 23.1, "Part Numbers Fully Addressed by this Document," for silicon revision level determination.

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1   Overview

This section provides a high-level overview of the MPC8347EA features. Figure 1 shows the major functional units within the MPC8347EA.
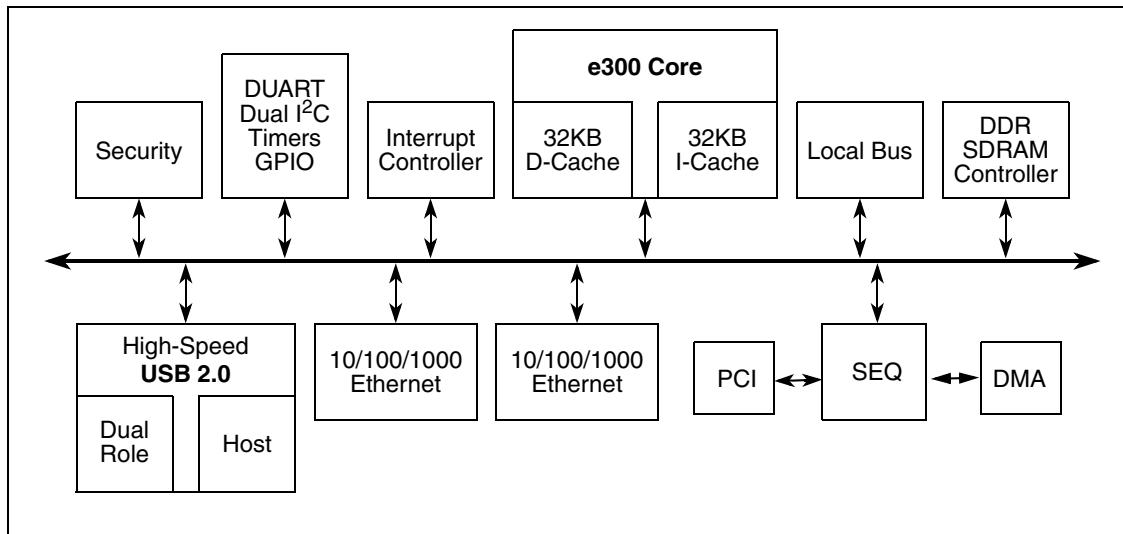
Figure 1. MPC8347EA Block Diagram

Major features of the MPC8347EA are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement the PowerPC architecture
- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- or 64-bit data interface, up to 400 MHz data rate for TBGA, 266 MHz for PBGA
  - Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full error checking and correction (ECC) support
  - Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep-mode support for SDRAM self refresh
  - Auto refresh

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- — On-the-fly power management using CKE
- — Registered DIMM support
- — 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - — Dual controllers designed to comply with IEEE Std. 802.3™, 802.3u, 820.3x, 802.3z, 802.3ac
  - — Ethernet physical interfaces:
    - – 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - – 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - — Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - — 9.6-Kbyte jumbo frame support
  - — RMON statistics support
  - — Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - — MII management interface for control and status
  - — Programmable CRC generation and checking
- PCI interface
  - — Designed to comply with PCI specification revision 2.3
  - — Data bus width:
    - – 32-bit data PCI interface operating at up to 66 MHz
  - — PCI 3.3-V compatible
  - — PCI host bridge capabilities
  - — PCI agent mode on PCI interface
  - — PCI-to-memory and memory-to-PCI streaming
  - — Memory prefetching of PCI read accesses and support for delayed read transactions
  - — Posting of processor-to-PCI and PCI-to-memory writes
  - — On-chip arbitration supporting five masters on PCI
  - — Accesses to all PCI address spaces
  - — Parity supported
  - — Selectable hardware-enforced coherency
  - — Address translation units for address mapping between host and peripheral
  - — Dual address cycle for target
  - — Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i™, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
  - — Public key execution unit (PKEU) :
    - – RSA and Diffie-Hellman algorithms
    - – Programmable field size up to 2048 bits

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- Elliptic curve cryptography
- F2m and F(p) modes
- Programmable field size up to 511 bits

— Data encryption standard (DES) execution unit (DEU)

- DES and 3DES algorithms
- Two key (K1, K2) or three key (K1, K2, K3) for 3DES
- ECB and CBC modes for both DES and 3DES

— Advanced encryption standard unit (AESU)

- Implements the Rijndael symmetric-key cipher
- Key lengths of 128, 192, and 256 bits
- ECB, CBC, CCM, and counter (CTR) modes

— XOR parity generation accelerator for RAID applications

— ARC four execution unit (AFEU)

- Stream cipher compatible with the RC4 algorithm
- 40- to 128-bit programmable key

— Message digest execution unit (MDEU)

- SHA with 160-, 224-, or 256-bit message digest
- MD5 with 128-bit message digest
- HMAC with either algorithm

— Random number generator (RNG)

— Four crypto-channels, each supporting multi-command descriptor chains

- Static and/or dynamic assignment of crypto-execution units through an integrated controller
- Buffer size of 256 bytes for each execution unit, with flow control for large data sizes

- Universal serial bus (USB) dual role controller
  — USB on-the-go mode with both device and host functionality
  — Complies with USB specification Rev. 2.0
  — Can operate as a stand-alone USB device
    - One upstream facing port
    - Six programmable USB endpoints
  — Can operate as a stand-alone USB host controller
    - USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
    - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  — External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
  — Can operate as a stand-alone USB host controller
    - USB root hub with one or two downstream-facing ports

- – Enhanced host controller interface (EHCI) compatible
- – Complies with USB specification Rev. 2.0
- — High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- — Direct connection to a high-speed device without an external hub
- — External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
  - — Multiplexed 32-bit address and data operating at up to 133 MHz
  - — Eight chip selects for eight external slaves
  - — Up to eight-beat burst transfers
  - — 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - — Three protocol engines on a per chip select basis:
    - – General-purpose chip select machine (GPCM)
    - – Three user-programmable machines (UPMs)
    - – Dedicated single data rate SDRAM controller
  - — Parity support
  - — Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - — Functional and programming compatibility with the MPC8260 interrupt controller
  - — Support for 8 external and 35 internal discrete interrupt sources
  - — Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - — Programmable highest priority request
  - — Four groups of interrupts with programmable priority
  - — External and internal interrupts directed to host processor
  - — Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  - — Unique vector number for each interrupt source
- Dual industry-standard I^2C interfaces
  - — Two-wire interface
  - — Multiple master support
  - — Master or slave I^2C mode support
  - — On-chip digital filtering rejects spikes on the bus
  - — System initialization data optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - — Four independent virtual channels
  - — Concurrent execution across multiple channels with programmable bandwidth control
  - — Handshaking (external control) signals for all channels: $\overline{\text{DMA\_DREQ}}[0:3]$, $\overline{\text{DMA\_DACK}}[0:3]$, $\overline{\text{DMA\_DDONE}}[0:3]$
  - — All channels accessible to local core and remote PCI masters

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- — Misaligned transfer capability
- — Data chaining and direct mode
- — Interrupt on completed segment and chain
- DUART
  - — Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - — Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
  - — 52 parallel I/O pins multiplexed on various chip interfaces
- System timers
  - — Periodic interrupt timer
  - — Real-time clock
  - — Software watchdog timer
  - — Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal charaistics for the MPC8347EA. The MPC8347EA is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	−0.3 to 1.32	V	
PLL supply voltage		AV_{DD}	−0.3 to 1.32	V	
DDR and DDR2 DRAM I/O voltage		GV_{DD}	−0.3 to 2.75 −0.3 to 1.98	V	
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	−0.3 to 3.63	V	
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	−0.3 to 3.63	V	
Input voltage	DDR DRAM signals	MV_{IN}	−0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	−0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	−0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	−0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	−0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	−55 to 150	•C	

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8347EA. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	
Three-speed Ethernet I/O supply voltage	LV_{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
Three-speed Ethernet I/O supply voltage	LV_{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
PCI, local bus, DUART, system control and power management, I²C, and JTAG I/O voltage	OV_{DD}	3.3 V ± 330 mV	V	

Notes:

1. GVDD, LVDD, OVDD, AVDD, and VDD must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8347EA.

Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.
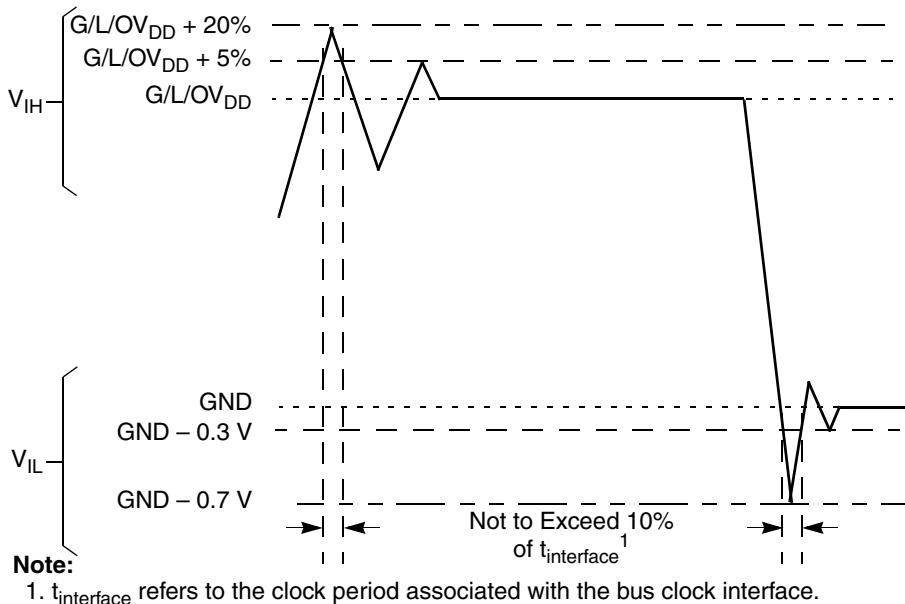
Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}/LV_{DD}

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8347EA for the 3.3-V signals, respectively.
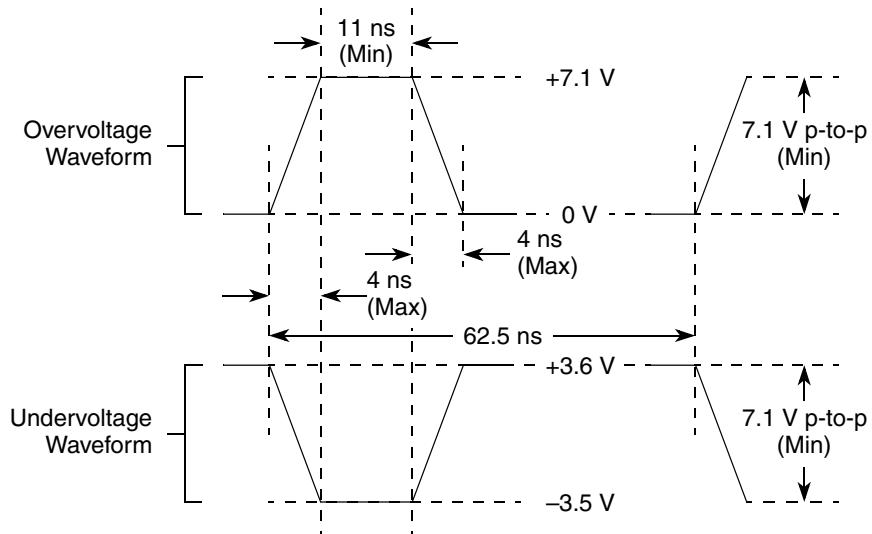

Figure 3. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3   Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV_{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20	GV_{DD} = 2.5 V
DDR2 signal	16 32 (half strength mode)	GV_{DD} = 1.8 V
TSEC/10/100 signals	42	LV_{DD} = 2.5/3.3 V
DUART, system control, I2C, JTAG	42	OV_{DD} = 3.3 V
GPIO signals	42	OV_{DD} = 3.3 V, LV_{DD} = 2.5/3.3 V

2.2 Power Sequencing

MPC8347EA does not require the core supply voltage and I/O supply voltages to be applied in any particular order. Note that during the power ramp up, before the power supplies are stable, there may be a period of time that I/O pins are actively driven. After the power is stable, as long as $\overline{\text{PORESET}}$ is asserted, most I/O pins are tri-stated. To minimize the time that I/O pins are actively driven, it is recommended to apply core voltage before I/O voltage and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up.

3   Power Characteristics

The estimated typical power dissipation for the MPC8347EA device is shown in Table 4.

Table 4. MPC8347EA Power Dissipation [1]

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at $T_J = 65$	Typical [2,3]	Maximum [4]	Unit
PBGA	266	266	1.3	1.6	1.8	W
		133	1.1	1.4	1.6	W
	400	266	1.5	1.9	2.1	W
		133	1.4	1.7	1.9	W
	400	200	1.5	1.8	2.0	W
		100	1.3	1.7	1.9	W
TBGA	333	333	2.0	3.0	3.2	W
		166	1.8	2.8	2.9	W
	400	266	2.1	3.0	3.3	W
		133	1.9	2.9	3.1	W
	450	300	2.3	3.2	3.5	W
		150	2.1	3.0	3.2	W
	500	333	2.4	3.3	3.6	W
		166	2.2	3.1	3.4	W
	533	266	2.4	3.3	3.6	W
		133	2.2	3.1	3.4	W
	667	333	3.5	4.6	5	W

[1] The values do not include I/O supply power (OVDD, LVDD, GVDD) or AVDD. For I/O power values, see Table 5.

[2] Typical power is based on a voltage of Vdd = 1.2 V, a junction temperature of $T_J = 105°C$, and a Dhrystone benchmark application.

[3] Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.

[4] Maximum Power is based on a voltage of Vdd = 1.2 V, worst case process, a junction temperature of $T_J = 105°C$, and an artificial smoke test.

Table 5 shows the estimated typical I/O power dissipation for MPC8347EA.

Table 5. MPC8347EA Typical I/O Power Dissipation

Interface	Parameter	DDR2 GVDD (1.8 V)	DDR1 GVDD (2.5 V)	OVDD (3.3 V)	LVDD (3.3 V)	LVDD (2.5 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V Rs = 20 Ω Rt = 50 Ω 2 pair of clocks	200 MHz, 32 bits	0.31	0.42	—	—	—	W	—
	200 MHz, 64 bits	0.42	0.55	—	—	—	W	—
	266 MHz, 32 bits	0.35	0.5	—	—	—	W	—
	266 MHz, 64 bits	0.47	0.66	—	—	—	W	—
	300 MHz [1], 32 bits	0.37	0.54	—	—	—	W	—
	300 MHz[1], 64 bits	0.50	0.7	—	—	—	W	—
	333 MHz[1], 32 bits	0.39	0.58	—	—	—	W	—
	333 MHz[1], 64 bits	0.53	0.76	—	—	—	W	—
	400MHz[1], 32b	0.44	—	—	—	—		—
	400MHz[1], 64b	0.59	—	—	—	—		—
PCI I/O load = 30 pf	33 MHz, 32 bits	—	—	0.04	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
Local Bus I/O Load = 25 pf	167 Mhz, 32 bits	—	—	0.34	—	—	W	—
	133 MHz, 32 bits	—	—	0.27	—	—	W	—
	83 MHz, 32 bits	—	—	0.17	—	—	W	—
	66 MHz, 32 bits	—	—	0.14	—	—	W	—
	50 Mhz, 32 bits	—	—	0.11	—	—	W	—
TSEC I/O Load = 25 pf	MII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.06	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
USB	12 MHz	—	—	0.01	—	—	W	Multiply by 2 if using 2 ports.
	480 MHz	—	—	0.2	—	—	W	
Other I/O		—	—	0.01	—	—	W	—

[1] TBGA package only.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8347EA.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8347EA.

Table 6. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD}+0.3	V
Input low voltage	—	V_{IL}	−0.3	0.4	V
CLKIN Input current	0V $\leq V_{IN} \leq$ OVDD	I_{IN}	—	±10	µA
PCI_SYNC_IN Input current	0V $\leq V_{IN} \leq$ 0.5 V or OVDD − 0.5 V $\leq V_{IN} \leq$ OVDD	I_{IN}	—	±10	µA
PCI_SYNC_IN Input current	0.5 V $\leq V_{IN} \leq$ OVDD - 0.5 V	I_{IN}	—	±50	µA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8347EA can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8347EA.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	+/− 150	ps	4, 5

Notes:

1. **Caution:** The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.

2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.

3. Timing is guaranteed by design and characterization.

4. This represents the total input jitter—short term and long term—and is guaranteed by design.

5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8347EA.

5.1 RESET DC Electrical Characteristics

Table 8 provides the DC electrical characteristics for the RESET pins of the MPC8347EA.

Table 8. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	$OV_{DD}+0.3$	V
Input low voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}			±5	µA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

Notes:

1. This table applies for pins $\overline{PORESET}$, $\overline{HRESET}$, $\overline{SRESET}$ and $\overline{QUIESCE}$.
2. $\overline{HRESET}$ and $\overline{SRESET}$ are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 RESET AC Electrical Characteristics

Table 9 provides the reset initialization AC timing specifications of the MPC8347EA.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{HRESET}$ or $\overline{SRESET}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{PORESET}$ with stable clock applied to CLKIN when the MPC8347EA is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{PORESET}$ with stable clock applied to PCI_SYNC_IN when the MPC8347EA is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{HRESET}$/$\overline{SRESET}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{HRESET}$ negation to $\overline{SRESET}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{PORESET}$ when the MPC8347EA is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{PORESET}$ when the MPC8347EA is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1

Table 9. RESET Initialization Timing Specifications (continued)

Input hold time for POR configuration signals with respect to negation of HRESET	0	—	ns	
Time for the MPC8347EA to turn off POR configuration signals with respect to the assertion of HRESET	—	4	ns	3
Time for the MPC8347EA to turn on POR configuration signals with respect to the negation of HRESET	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA Integrated Host Processor Reference Manual*.

2. tCLKIN is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349EA Integrated Host Processor Reference Manual*.

3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 lists the PLL and DLL lock times.

Table 10. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8347EA. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

NOTE

The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8347E PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications.* See Section 23.1, "Part Numbers Fully Addressed by this Document," for silicon revision level determination.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8347EA when GV_{DD}(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V	
Output leakage current	I_{OZ}	-9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	-13.4	—	mA	
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to equal $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$.

Table 12 provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 12. DDR2 SDRAM Capacitance for GV$_{DD}$(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 13 provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5$ V.

Table 13. DDR SDRAM DC Electrical Characteristics for GV$_{DD}$ (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	
Input low voltage	V_{IL}	−0.3	$MV_{REF} - 0.18$	V	
Output leakage current	I_{OZ}	−9.9	−9.9	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	−15.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 14 provides the DDR capacitance when GV_{DD} (typ)=2.5 V.

Table 14. DDR SDRAM Capacitance for GV$_{DD}$ (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 15 provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV$_{REF}$

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV$_{REF}$	I$_{MVREF}$	—	500	μA	1

1. The voltage regulator for MV$_{REF}$ must supply up to 500 μA current.

6.2   DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1   DDR and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM when GV_{DD}(typ)=1.8 V.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV$_{DD}$ of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V$_{IL}$	—	MV$_{REF}$ – 0.25	V	
AC input high voltage	V$_{IH}$	MV$_{REF}$ + 0.25	—	V	

Table 17 provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ)=2.5 V.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV$_{DD}$ of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V$_{IL}$	—	MV$_{REF}$ – 0.31	V	
AC input high voltage	V$_{IH}$	MV$_{REF}$ + 0.31	—	V	

Table 18 provides the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1
400 MHz		−600	600		2
333 MHz		−750	750		3
266 MHz		−750	750		3
200 MHz		−750	750		3

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

2. This specification applies only to the DDR2 interface.

3. This specification applies only to the DDR interface.

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 19 shows the DDR and DDR2 output AC timing specifications.

Table 19. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{MCK}$[n] crossing)	t_{MCK}	5	10	ns	2
ADDR/CMD/MODT output setup with respect to MCK	t_{DDKHAS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
ADDR/CMD/MODT output hold with respect to MCK	t_{DDKHAX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
$\overline{MCS}$(n) output setup with respect to MCK	t_{DDKHCS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		

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Table 19. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{MCS}$(n) output hold with respect to MCK	t_{DDKHCX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCK to MDQS Skew	t_{DDKHMH}	−0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	$t_{DDKHDS},$ t_{DDKLDS}			ps	5
400 MHz		700	—		
333 MHz		900	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQ/MECC/MDM output hold with respect to MDQS	$t_{DDKHDX},$ t_{DDKLDX}			ps	5
400 MHz		700	—		
333 MHz		900	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} +0.6$	ns	6

Table 19. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	−0.6	0.6	ns	6

Note:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.

2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.

3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the *MPC8349EA PowerQUICC II Pro Integrated Processor Reference Manual* for the timing modifications enabled by use of these bits.

5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.

6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).
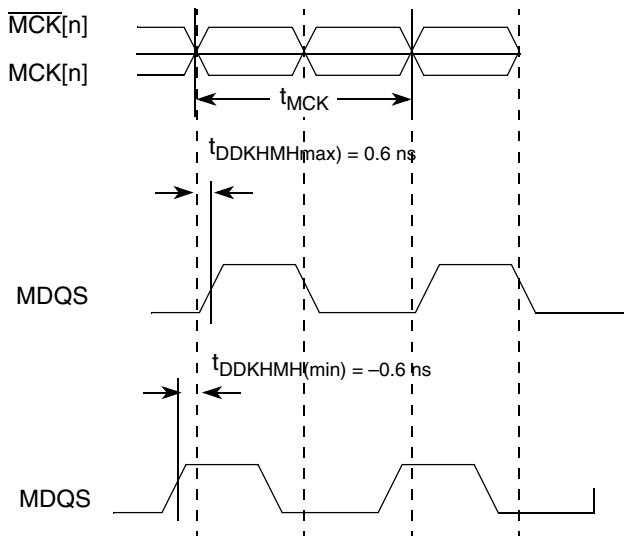
Figure 4. Timing Diagram for t_{DDKHMH}

Figure 5 shows the DDR SDRAM output timing diagram.
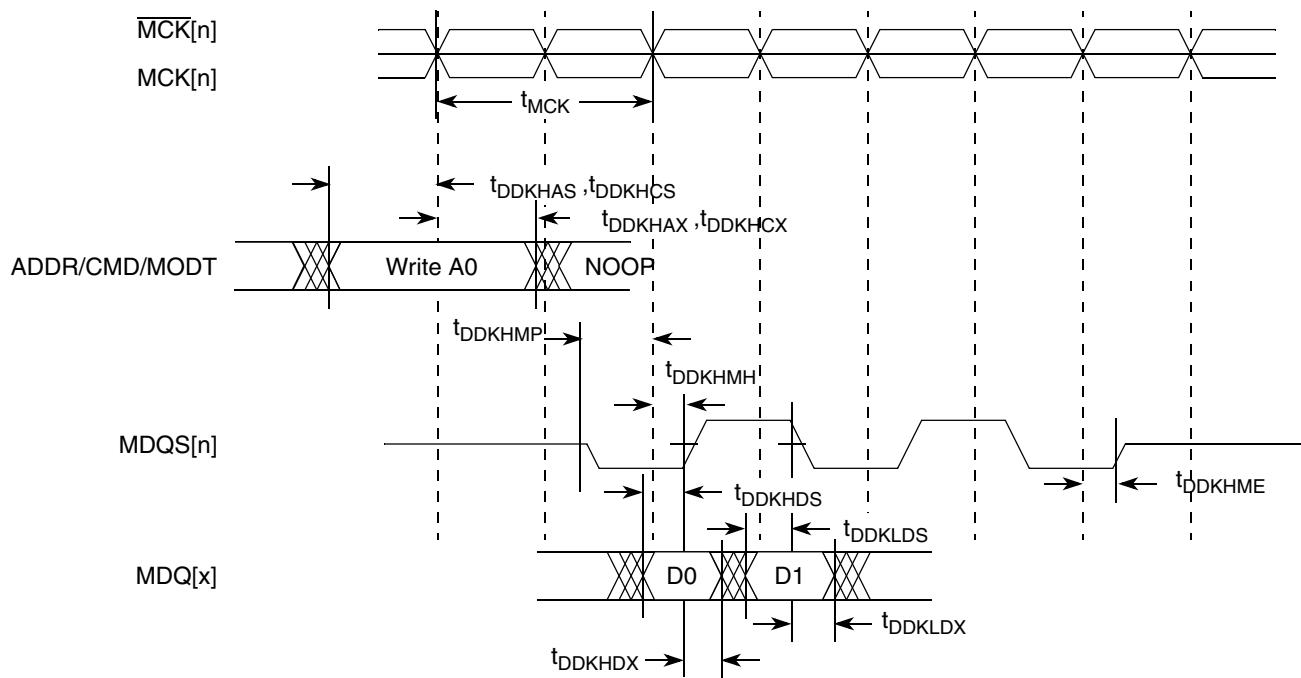
Figure 5. DDR SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.
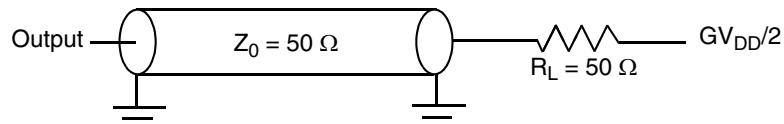
Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8347EA.

7.1 DUART DC Electrical Characteristics

Table 20 provides the DC electrical characteristics for the DUART interface of the MPC8347EA.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	−0.3	0.8	V
Input current (0.8 V $\leq V_{IN} \leq$ 2 V)	I_{IN}	—	+/- 5	μA
High-level output voltage, $I_{OH} = -100$ μA	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100$ μA	V_{OL}	—	0.2	V

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 21 provides the AC timing parameters for the DUART interface of the MPC8347EA.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC) —GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to the gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces can operate at 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 TSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 22 and Table 23. The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver power supply (that is, a RGMII driver powered from a 3.6 V supply driving V_{OH} into a RGMII receiver powered from a 2.5-V supply). Tolerance for dissimilar RGMII driver and receiver supply potentials is implicit in these specifications.The RGMII and RTBI signals are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 22. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD} [2]	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0$ mA	LV_{DD} = Min	2.40	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0$ mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	−0.3	0.90	V
Input high current	I_{IH}	V_{IN} [1] $= LV_{DD}$		—	40	μA
Input low current	I_{IL}	V_{IN} [1] $=$ GND		−600	—	μA

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the OVDD supply.

Table 23. RGMII/RTBI (When Operating at 2.5 V), DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0$ mA	LV_{DD} = Min	2.00	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0$ mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	LV_{DD} =Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} [1] = LV_{DD}		—	10	μA
Input low current	I_{IL}	V_{IN} [1] = GND		–15	—	μA

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2   GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1   GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.1.1   GMII Transmit AC Timing Specifications

Table 24 provides the GMII transmit AC timing specifications.

Table 24. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK clock rise time, V_{IL}(min) to V_{IH}(max)	t_{GTXR}	—	—	1.0	ns
GTX_CLK clock fall time, V_{IH}(max) to V_{IL}(min)	t_{GTXF}	—	—	1.0	ns
GTX_CLK125 clock period	t_{G125} [2]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle measured at LV_{DD}/ 2	t_{G125H}/t_{G125}	45	—	55	%

Notes:

1. The symbols for timing specifications follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. This symbol represents the external GTX_CLK125 signal and does not follow the original symbol naming convention.

Figure 7 shows the GMII transmit AC timing diagram.
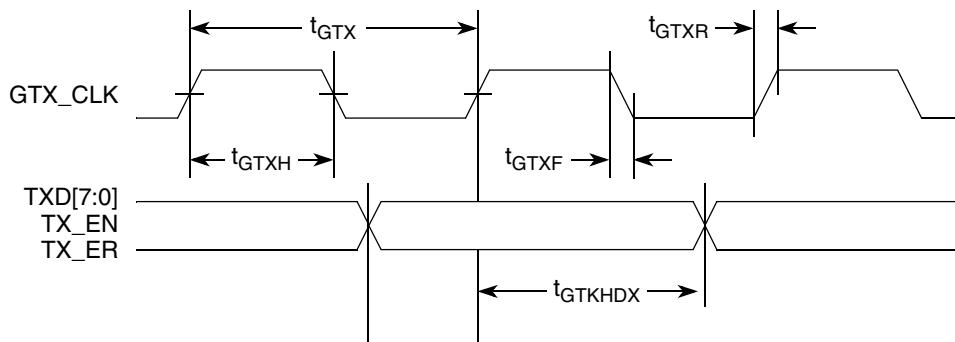
Figure 7. GMII Transmit AC Timing Diagram

8.2.1.2   GMII Receive AC Timing Specifications

Table 25 provides the GMII receive AC timing specifications.

**Table 25. GMII Receive AC Timing Specifications**

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise, V_{IL}(min) to V_{IH}(max)	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time, V_{IH}(max) to V_{IL}(min)	t_{GRXF}	—	—	1.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 shows the GMII receive AC timing diagram.
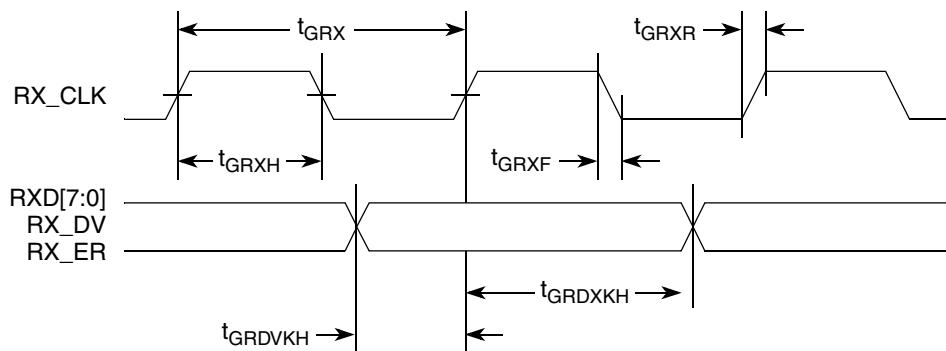
Figure 8. GMII Receive AC Timing Diagram

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8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 26 provides the MII transmit AC timing specifications.

**Table 26. MII Transmit AC Timing Specifications**

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of t(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). In general, the clock reference symbol is based on two to three letters representing the clock of a particular function. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9 shows the MII transmit AC timing diagram.
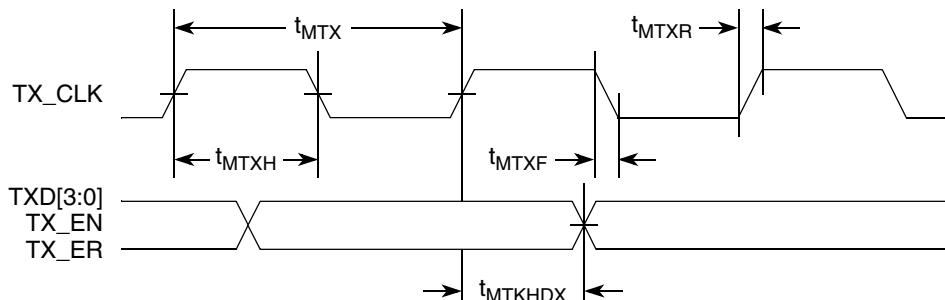
Figure 9. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

Table 27 provides the MII receive AC timing specifications.

**Table 27. MII Receive AC Timing Specifications**

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

| Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{(first two letters of functional block)(signal)(state) (reference)(state)}$ for inputs and $t_{(first two letters of functional block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular functionl. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 provides the AC test load for TSEC.
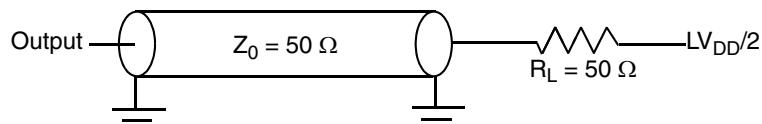
Figure 10. TSEC AC Test Load

Figure 11 shows the MII receive AC timing diagram.
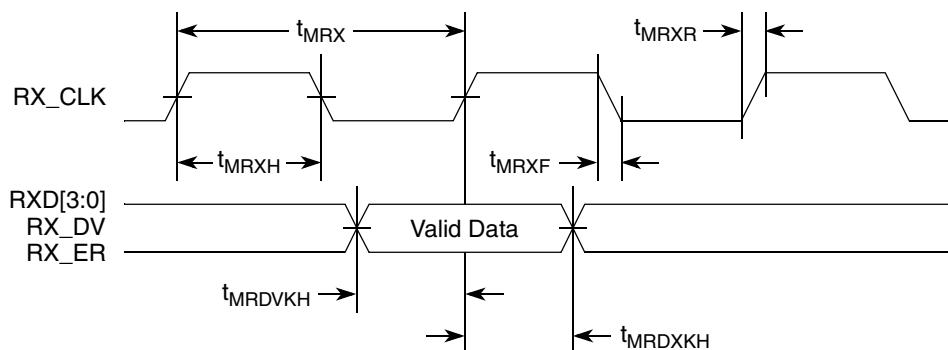
Figure 11. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 28 provides the TBI transmit AC timing specifications.

**Table 28. TBI Transmit AC Timing Specifications**

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t_{TTKHDX}	1.0	—	5.0	ns
GTX_CLK clock rise, V_{IL}(min) to V_{IH}(max)	t_{TTXR}	—	—	1.0	ns
GTX_CLK clock fall time, V_{IH}(max) to V_{IL}(min)	t_{TTXF}	—	—	1.0	ns
GTX_CLK125 reference clock period	t_{G125} [2]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	45	—	55	ns

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol represents the external GTX_CLK125 and does not follow the original symbol naming convention

Figure 12 shows the TBI transmit AC timing diagram.
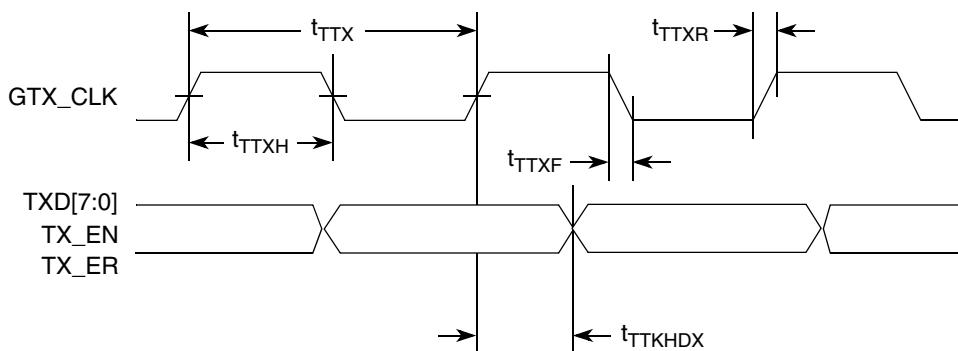
Figure 12. TBI Transmit AC Timing Diagram

8.2.3.2 TBI Receive AC Timing Specifications

Table 29 provides the TBI receive AC timing specifications.

**Table 29. TBI Receive AC Timing Specifications**

At recommended operating conditions with LV_{DD} / OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
PMA_RX_CLK clock period	t_{TRX}		16.0		ns
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t_{TRDVKH} [2]	2.5	—	—	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t_{TRDXKH} [2]	1.5	—	—	ns
RX_CLK clock rise time V_{IL}(min) to V_{IH}(max)	t_{TRXR}	0.7	—	2.4	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{TRXF}	0.7	—	2.4	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).

2. Setup and hold time of even numbered RCG are measured from the riding edge of PMA_RX_CLK1. Setup and hold times of odd-numbered RCG are measured from the riding edge of PMA_RX_CLK0.

Figure 13 shows the TBI receive AC timing diagram.
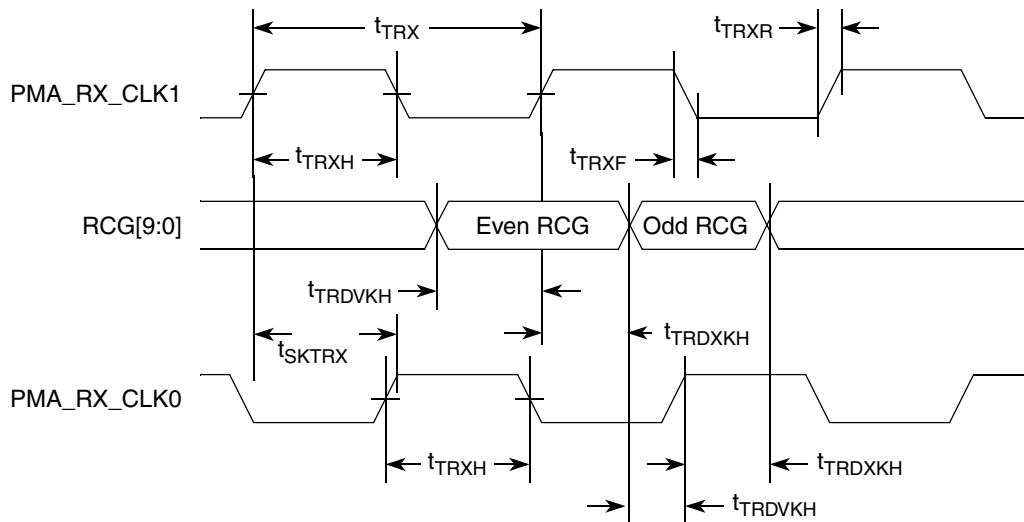
Figure 13. TBI Receive AC Timing Diagram

8.2.4 RGMII and RTBI AC Timing Specifications

Table 30 presents the RGMII and RTBI AC timing specifications.

Table 30. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).

2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.

5. Duty cycle reference is $L_{Vdd}/2$.

6. This symbol represents the external GTX_CLK125 and does not follow the original symbol naming convention.

Figure 14 shows the RBMII and RTBI AC timing and multiplexing diagrams.
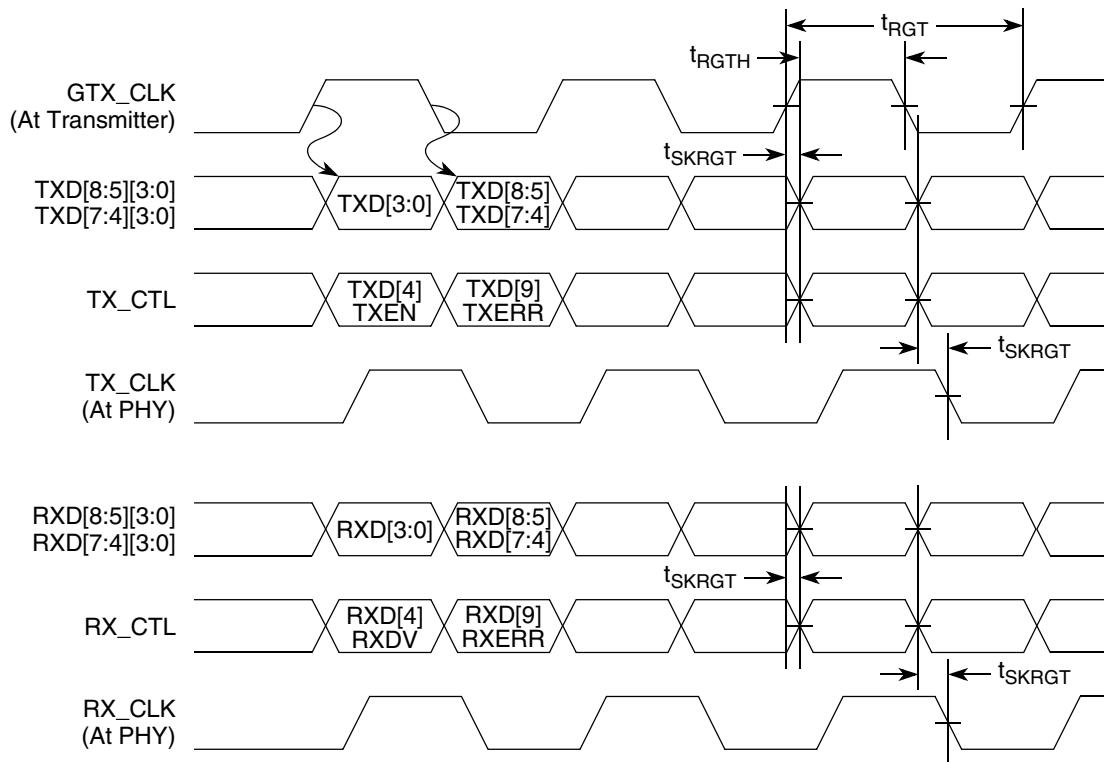
Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3　Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC) —GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1　MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 V or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 31 and Table 32.

Table 31. MII Management DC Electrical Characteristics Powered at 2.5 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (2.5 V)	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0$ mA	LV_{DD} = Min	2.00	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0$ mA	LV_{DD} = Min	GND - 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	—	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	-0.3	0.70	V
Input high current	I_{IH}	V_{IN} [1] $= LV_{DD}$		—	10	μA
Input low current	I_{IL}	$V_{IN} = LV_{DD}$		-15	—	μA

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 32. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	LV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0$ mA	LV_{DD} = Min	2.10	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0$ mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	LV_{DD} = Max	V_{IN} [1] $= 2.1$ V	—	40	μA
Input low current	I_{IL}	LV_{DD} = Max	$V_{IN} = 0.5$ V	–600	—	μA

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

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8.3.2 MII Management AC Electrical Specifications

Table 33 provides the MII management AC timing specifications.

**Table 33. MII Management AC Timing Specifications**

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).

3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 15 shows the MII management AC timing diagram.
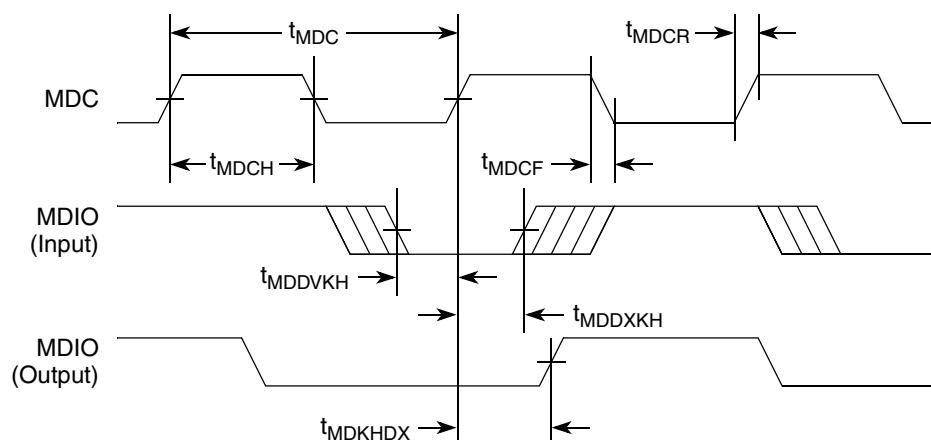
Figure 15. MII Management Interface Timing Diagram

9　USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8347EA.

9.1　USB DC Electrical Characteristics

Table 34 provides the DC electrical characteristics for the USB interface.

Table 34. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	−0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, $I_{OH} = -100\ \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100\ \mu A$	V_{OL}	—	0.2	V

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2　USB AC Electrical Specifications

Table 35 describes the general timing parameters of the USB interface of the MPC8347EA.

Table 35. USB General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Notes
usb clock cycle time	t_{USCK}	15	—	ns	
Input setup to usb clock - all inputs	t_{USIVKH}	4	—	ns	
input hold to usb clock - all inputs	t_{USIXKH}	1	—	ns	
usb clock to output valid - all outputs	t_{USKHOV}	—	7	ns	
Output hold from usb clock - all outputs	t_{USKHOX}	2	—	ns	

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(First\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(First\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{USIXKH} symbolizes usb timing (US) for the input (I) to go invalid (X) with respect to the time the usb clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 16 and Figure 17 provide the AC test load and signals for the USB, respectively.
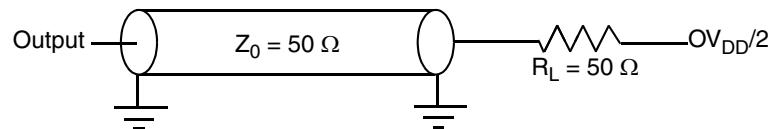

Figure 16. USB AC Test Load
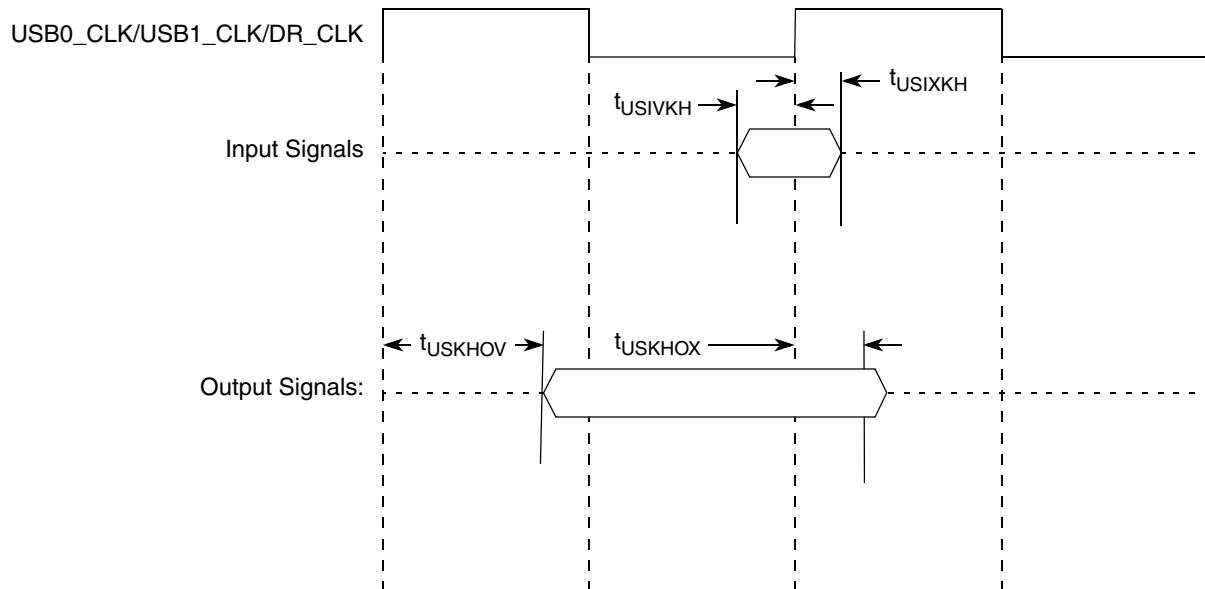
Figure 17. USB Signals

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8347EA.

10.1 Local Bus DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the local bus interface.

Table 36. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	−0.3	0.8	V
Input current	I_{IN}	—	±5	µA
High-level output voltage, $I_{OH} = -100 \ \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V_{OL}	—	0.2	V

10.2 Local Bus AC Electrical Specification

Table 37 and Table 38 describe the general timing parameters of the local bus interface of the MPC8347EA.

Table 37. Local Bus General Timing Parameters—DLL on

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	2.2	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1	—	ns	3

Table 37. Local Bus General Timing Parameters—DLL on (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(First\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(First\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to the rising edge of LSYNC_IN.

3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.

4. Input timings are measured at the pin.

5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.

6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.

7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.

8. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Table 38. Local Bus General Timing Parameters—DLL Bypass

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(First\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(First\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to the falling edge of LCLK0 (for all outputs and for $\overline{LGTA}$ and LUPWAIT inputs) or the rising edge of LCLK0 (for all other inputs).

3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.

4. Input timings are measured at the pin.

5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.

6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.the

7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals to the load on the LAD output pins.

8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

Figure 18 provides the AC test load for the local bus.
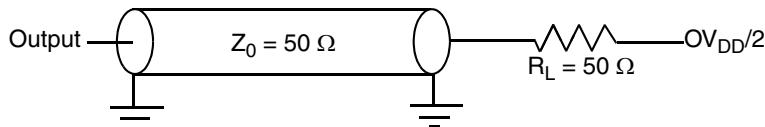
Figure 18. Local Bus C Test Load

Figure 19 through Figure 24 show the local bus signals.
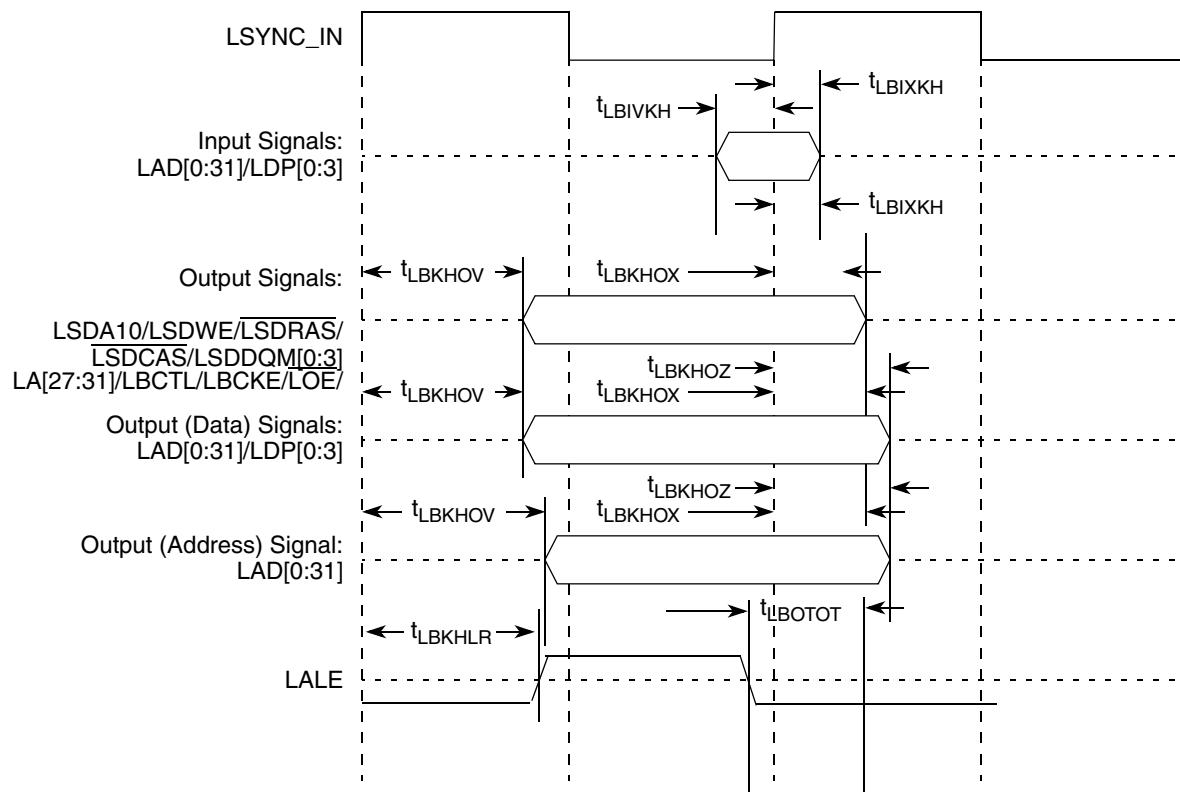
**Figure 19. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)**
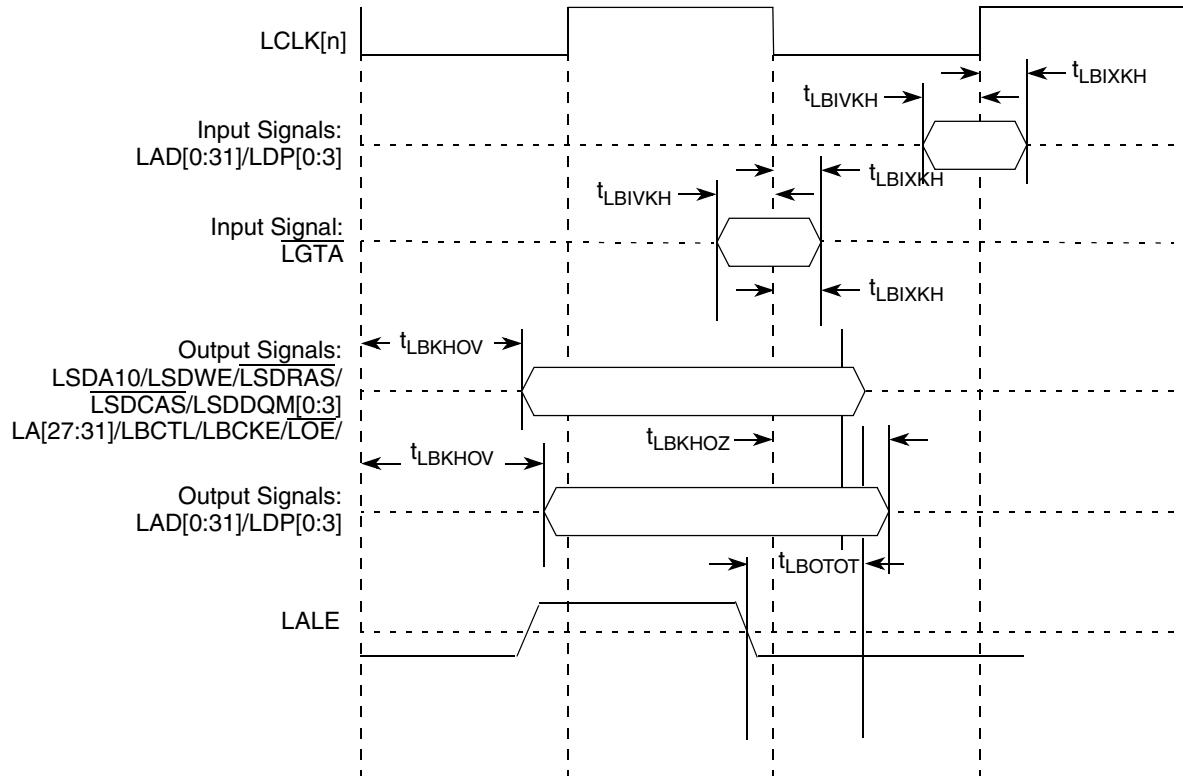
Figure 20. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)
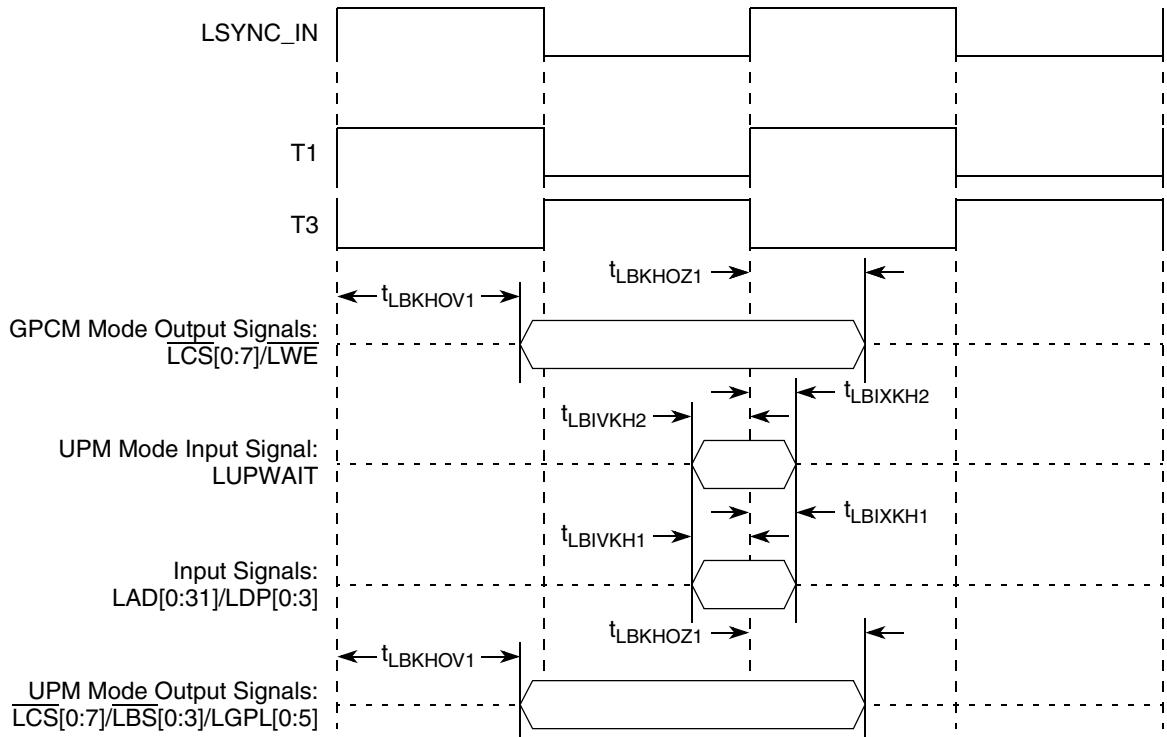
Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

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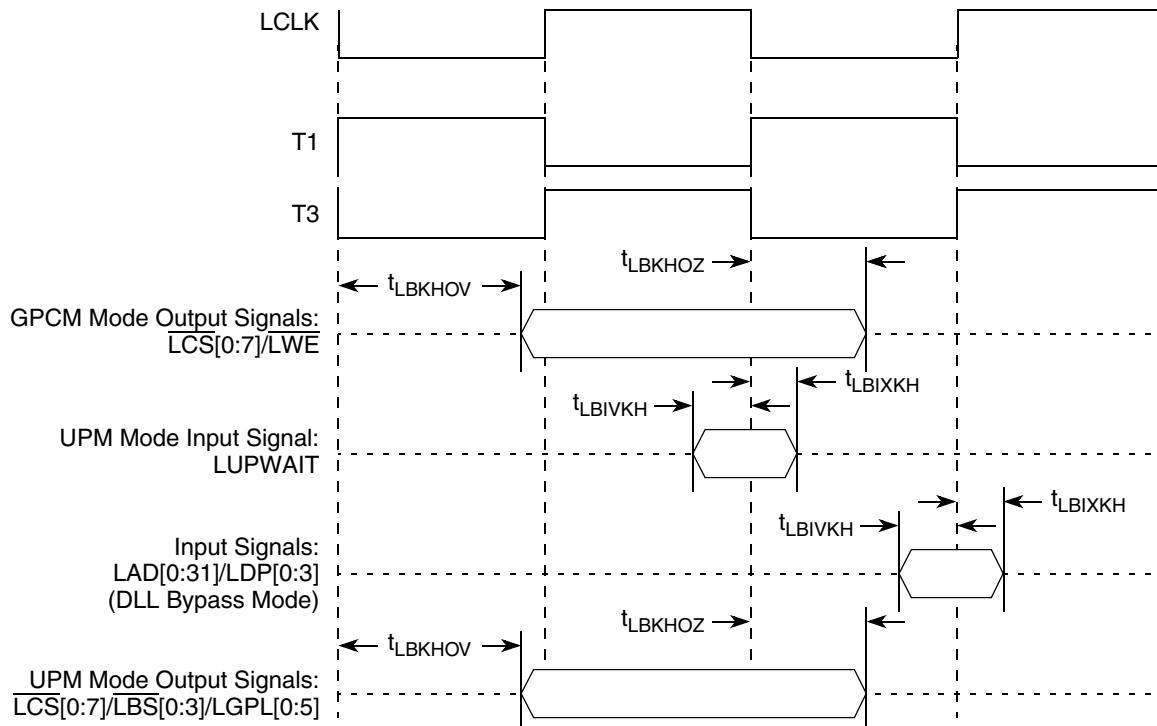
Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)
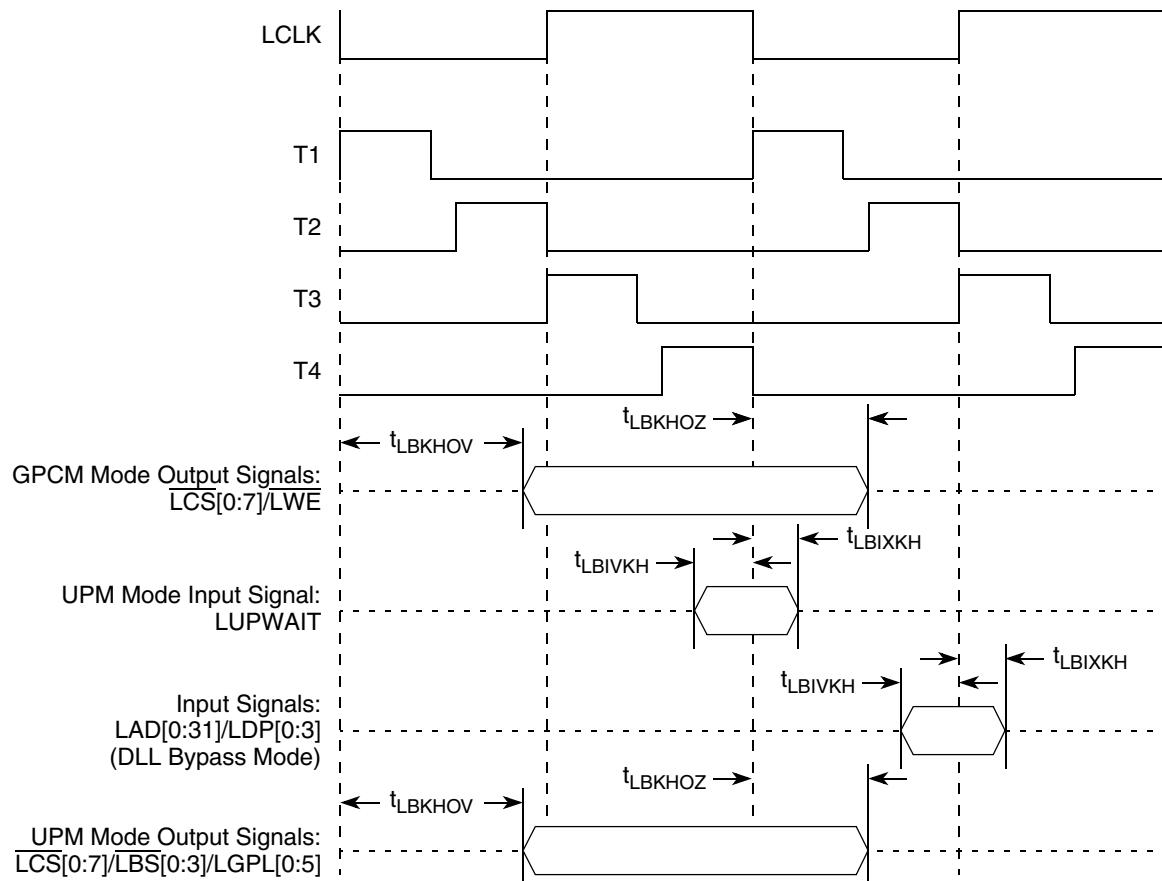
Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)
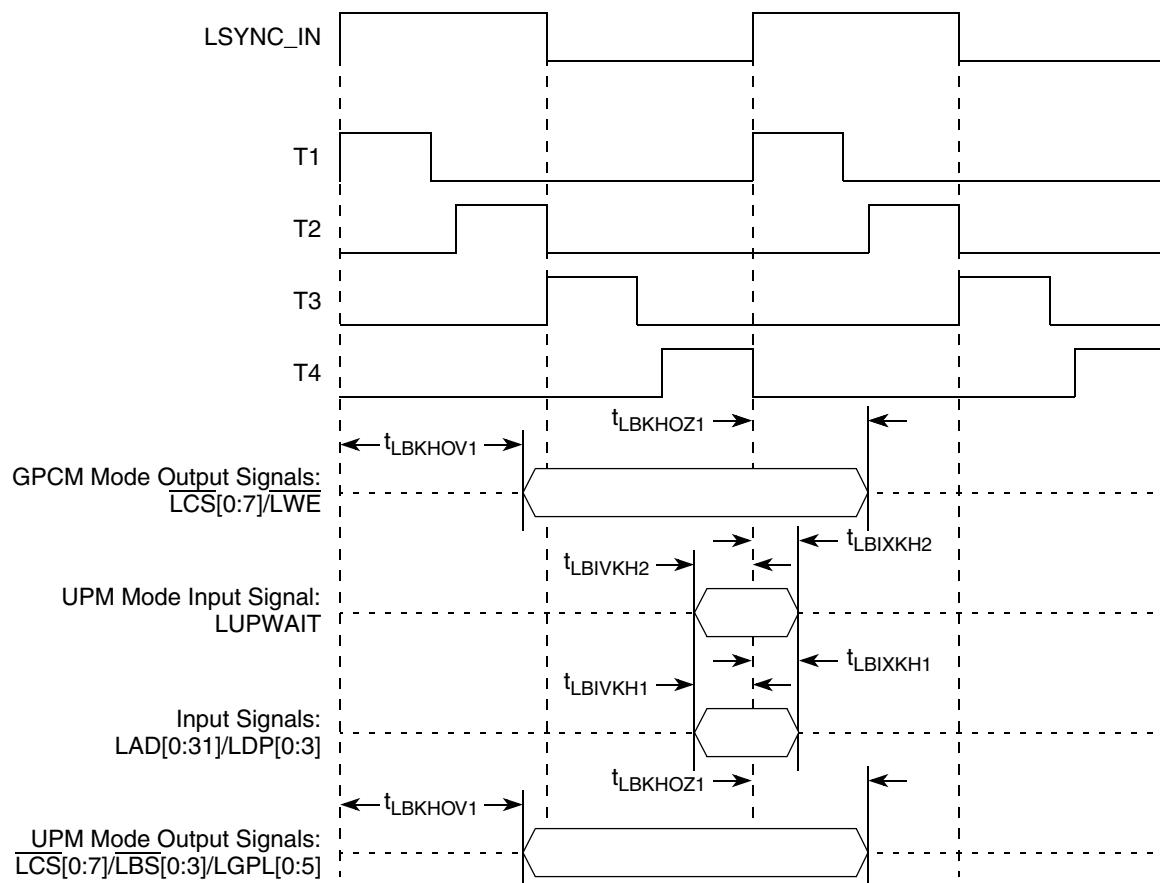
Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347EA

11.1 JTAG DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347EA.

Table 39. JTAG interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		$OV_{DD} - 0.3$	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}		−0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8347EA. Table 40 provides the JTAG AC timing specifications as defined in Figure 26 through Figure 29.

Table 40. JTAG AC Timing Specifications (Independent of CLKIN) [1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 4	ns — —		4
Input hold times: Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	10 10	ns — —		4
Valid times: Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	2 2	ns 11 11		5

Table 40. JTAG AC Timing Specifications (Independent of CLKIN) [1] (continued)

At recommended operating conditions (see Table 2).

| Parameter	Symbol [2]	Min	Max	Unit	Notes
Output hold times:				ns	5
Boundary-scan data	t_{JTKLDX}	2	—		
TDO	t_{JTKLOX}	2	—		
JTAG external clock to output high impedance:				ns	5, 6
Boundary-scan data	t_{JTKLDZ}	2	19		
TDO	t_{JTKLOZ}	2	9		

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 25). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.

4. Non-JTAG signal input timing with respect to t_{TCLK}.

5. Non-JTAG signal output timing with respect to t_{TCLK}.

6. Guaranteed by design and characterization.

Figure 25 provides the AC test load for TDO and the boundary-scan outputs of the MPC8347EA.
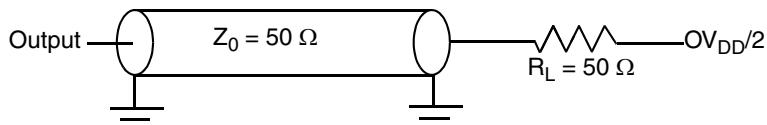
Figure 25. AC Test Load for the JTAG Interface

Figure 26 provides the JTAG clock input timing diagram.

VM = Midpoint Voltage ($OV_{DD}/2$)
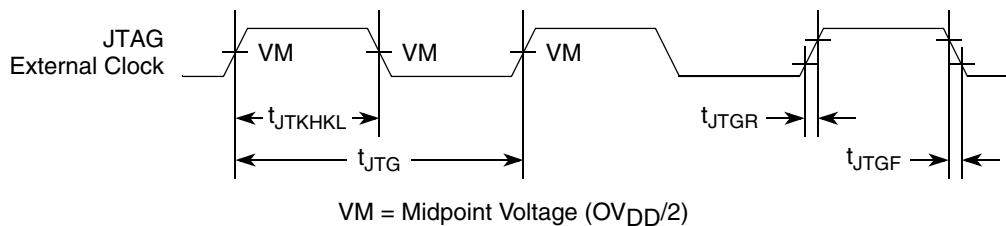
Figure 26. JTAG Clock Input Timing Diagram

Figure 27 provides the $\overline{\text{TRST}}$ timing diagram.

VM = Midpoint Voltage (OV$_{DD}$/2)
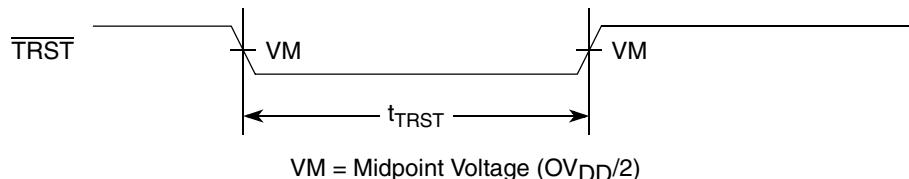
Figure 27. $\overline{\text{TRST}}$ Timing Diagram

Figure 28 provides the boundary-scan timing diagram.

VM = Midpoint Voltage (OV$_{DD}$/2)
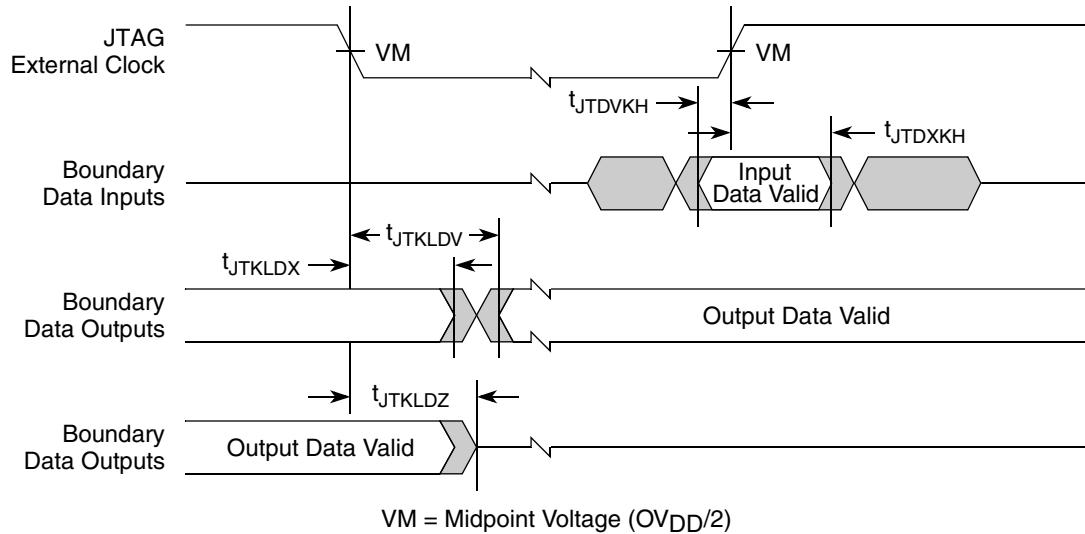
Figure 28. Boundary-Scan Timing Diagram

Figure 29 provides the test access port timing diagram.

VM = Midpoint Voltage (OV$_{DD}$/2)
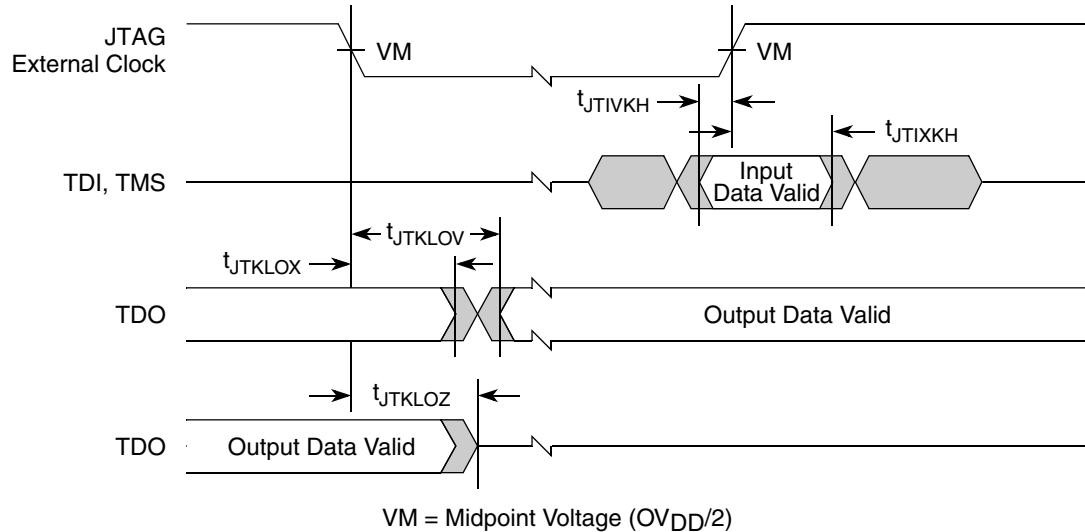
Figure 29. Test Access Port Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8347EA.

12.1 I²C DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the I²C interface of the MPC8347EA.

Table 41. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD}+ 0.3$	V	
Input low voltage level	V_{IL}	−0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	−10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. C_B = capacitance of one bus line in pF.

3. Refer to the *MPC8349E Integrated Host Processor Reference Manual* for information on the digital filter used.

4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 42 provides the AC timing parameters for the I²C interface of the MPC8347EA. Note that all values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 41).

Table 42. I²C AC Electrical Specifications

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0 [2]	— 0.9 [3]	μs

Table 42. I²C AC Electrical Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_b$ [4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1\ C_b$ [4]	300	ns
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. MPC8347EA provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.

Figure 30 provides the AC test load for the I²C.
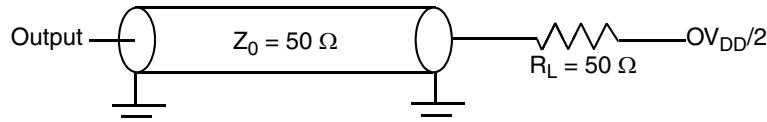
Figure 30. I²C AC Test Load

Figure 31 shows the AC timing diagram for the I²C bus.
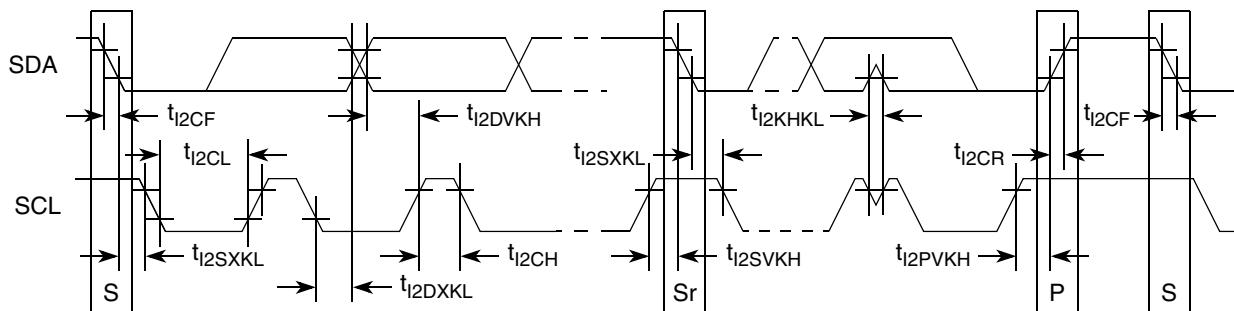
Figure 31. I²C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8347EA.

13.1 PCI DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the PCI interface of the MPC8347EA.

Table 43. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	−0.3	0.8	V
Input current	I_{IN}	V_{IN} [1] = 0 V or $V_{IN} = OV_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, $I_{OH} = -100$ μA	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, $I_{OL} = 100$ μA	—	0.2	V

Notes:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8347EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8347EA is configured as a host or agent device. Table 44 provides the PCI AC timing specifications at 66 MHz.

Table 44. PCI AC Timing Specifications at 66 MHz[6]

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from Clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to Clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.

2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.

3. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4. Input timings are measured at the pin.

6. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.

Table 45 provides the PCI AC timing specifications at 33 MHz.

Table 45. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from Clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to Clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 32 provides the AC test load for PCI.
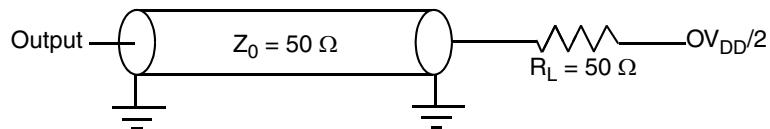
Figure 32. PCI AC Test Load

Figure 33 shows the PCI input AC timing diagram.
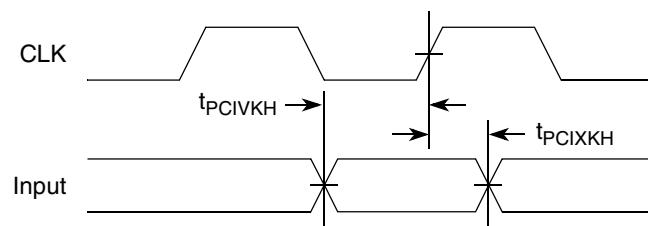
Figure 33. PCI Input AC Timing Diagram

Figure 34 shows the PCI output AC timing diagram.
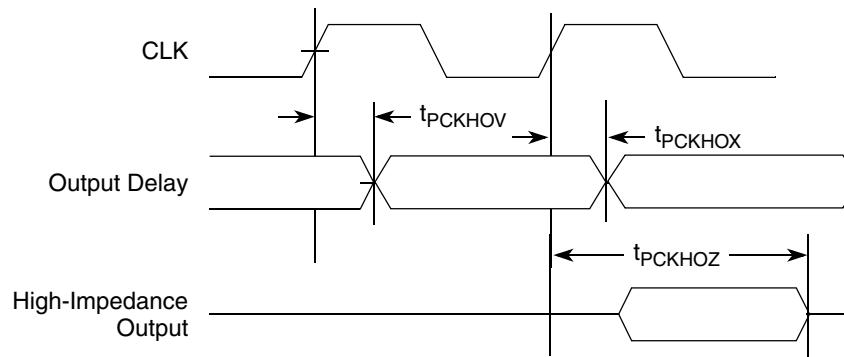
Figure 34. PCI Output AC Timing Diagram

14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timer DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8347EA timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 46. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	I_{OH} = −8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

14.2 Timer AC Timing Specifications

Table 47 provides the timer input and output AC timing specifications.

Table 47. Timers Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 48 provides the DC electrical characteristics for the MPC8347EA GPIO.

Table 48. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}		−0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	I_{OH} = −8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 49 provides the GPIO input and output AC timing specifications.

Table 49. GPIO Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 50 provides the DC electrical characteristics for the external interrupt pins.

Table 50. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}		−0.3	0.8	V
Input current	I_{IN}			±5	μA
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:

1. This table applies for pins $\overline{IRQ}$[0:7], $\overline{IRQ\_OUT}$ and $\overline{MCP\_OUT}$.
2. $\overline{IRQ\_OUT}$ and $\overline{MCP\_OUT}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 51 provides the IPIC input and output AC timing specifications.

Table 51. IPIC Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PICWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 52 provides the SPI DC electrical characteristics.

Table 52. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	$OV_{DD}+0.3$	V
Input low voltage	V_{IL}		−0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 53 provides the SPI input and output AC timing specifications.

Table 53. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}		6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—Master mode (internal clock input setup time	t_{NIIVKH}	4		ns
SPI inputs—Master mode (internal clock input hold time	t_{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.

2. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 35 provides the AC test load for the SPI.
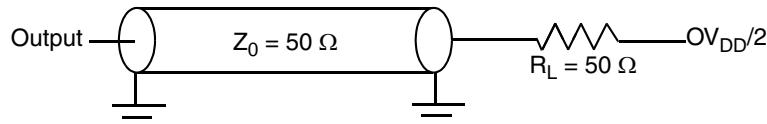
Figure 35. SPI AC Test Load

Figure 36 through Figure 37 represent the AC timings from Table 53. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 36 shows the SPI timings in slave mode (external clock).
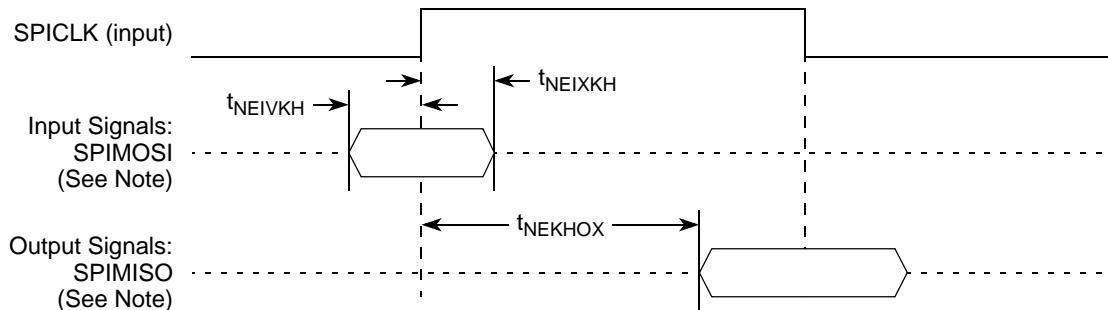
Note: The clock edge is selectable on SPI.

Figure 36. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 37 shows the SPI timings in master mode (internal clock).
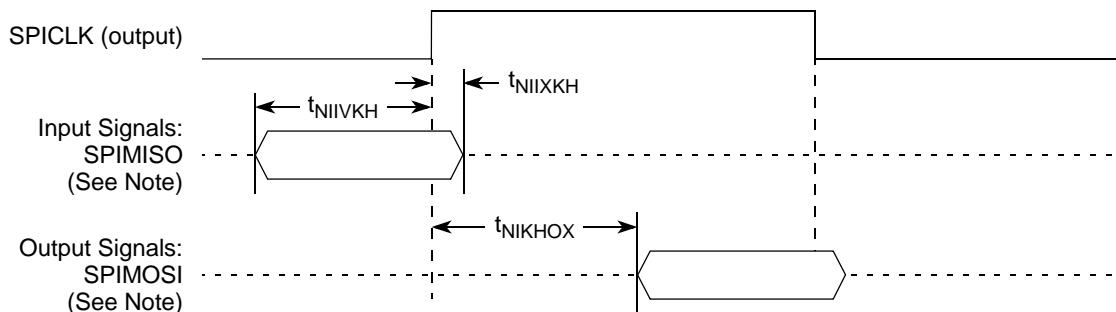
Note: The clock edge is selectable on SPI.

Figure 37. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8347EA is available in two packages a tape ball grid array (TBGA) and a plastic ball grid array (PBGA). See Section 18.1, "Package Parameters for the MPC8347EA TBGA," and Section 18.2, "Mechanical Dimensions of the MPC8347EA TBGA," and Section 18.3, "Package Parameters for the MPC8347EA PBGA" and Section 18.4, "Mechanical Dimensions of the MPC8347EA PBGA."

18.1 Package Parameters for the MPC8347EA TBGA

The package parameters are provided in the following list. The package type is 35 mm × 35 mm, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package)
	95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm

18.2   Mechanical Dimensions of the MPC8347EA TBGA

Figure 38 shows the mechanical dimensions and bottom surface nomenclature of the MPC8347EA, 672-TBGA package.
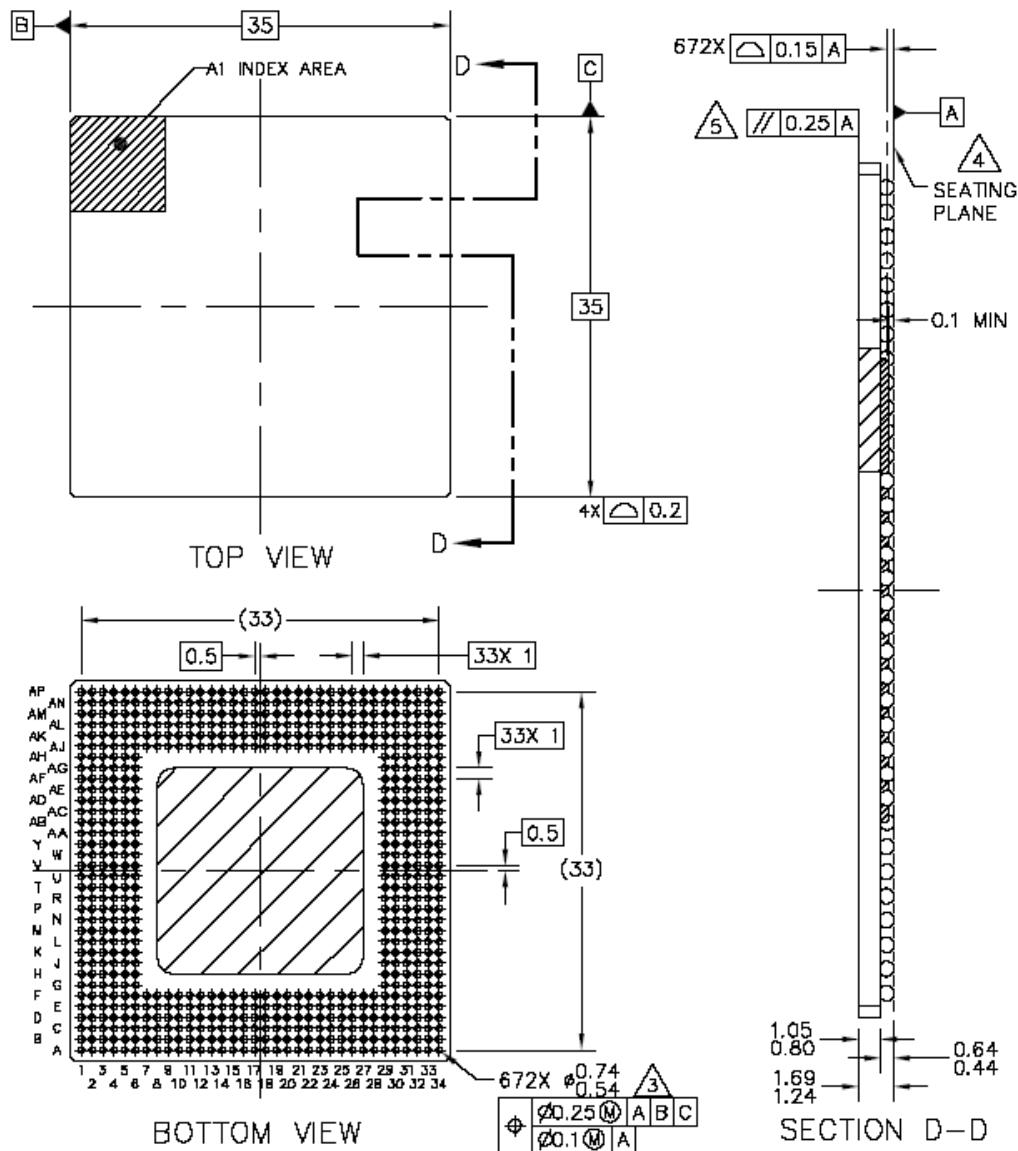
Figure 38. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8347EA TBGA

NOTES

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

18.3 Package Parameters for the MPC8347EA PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 Plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZQ package)
	95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.60 mm

18.4 Mechanical Dimensions of the MPC8347EA PBGA

Figure 39 shows the mechanical dimensions and bottom surface nomenclature of theMPC8347EA , 620-PBGA package.
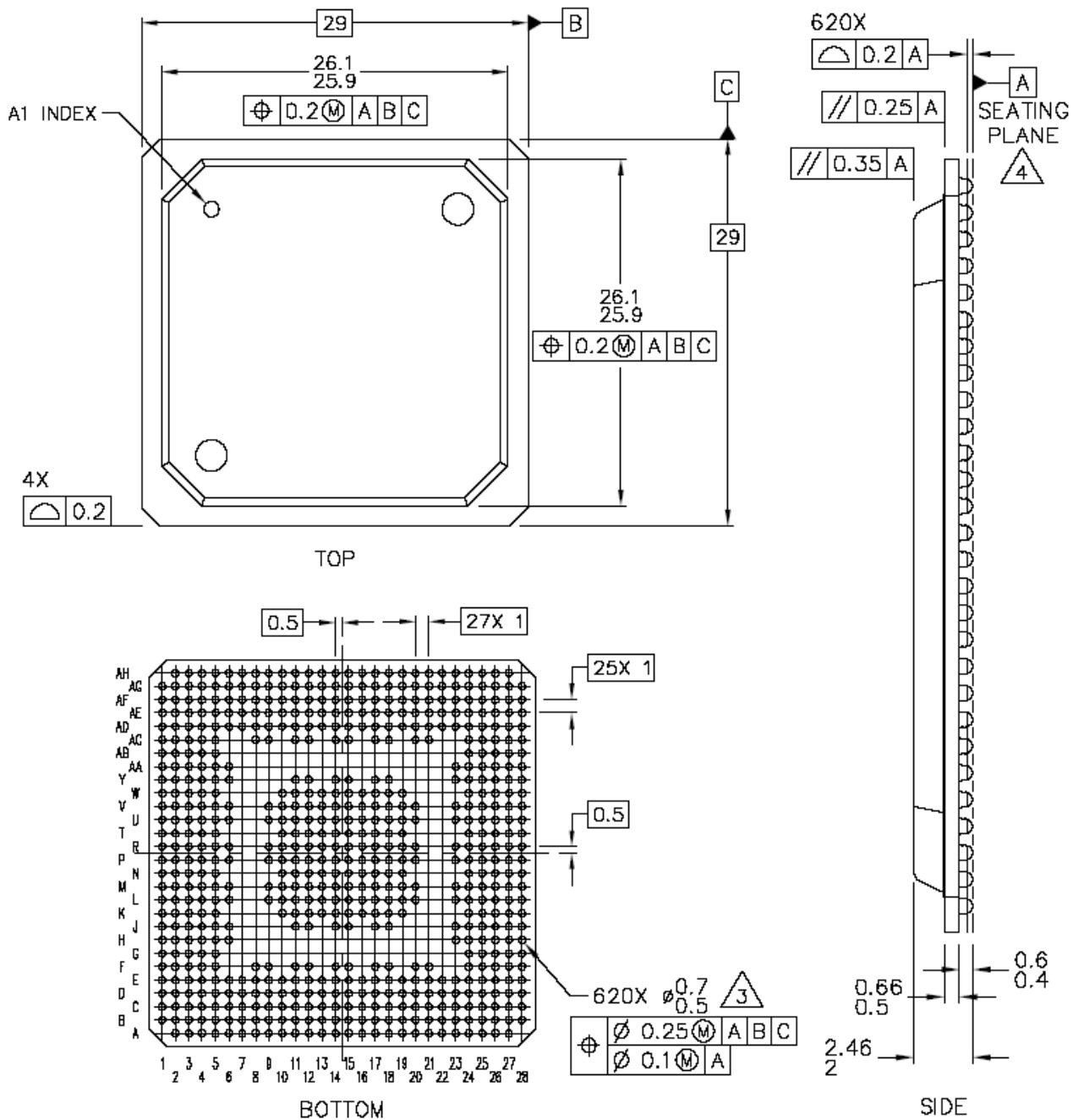

Figure 39. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8347EA PBGA

NOTE

1. All dimensions in millimeters
2. Dimensioning and tolerancing per ASME Y14. 5M-1994
3. Maximum solder ball diameter measured parallel to datum A
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

18.5 Pinout Listings

Table 51 provides the pin-out listing for the MPC8347EA, 672 TBGA package.

Table 54. MPC8347EA (TBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
$\overline{\text{PCI\_INTA}}$/$\overline{\text{IRQ\_OUT}}$	B34	O	OV$_{DD}$	2
$\overline{\text{PCI\_RESET\_OUT}}$	C33	O	OV$_{DD}$	
PCI_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV$_{DD}$	
PCI_C/$\overline{\text{BE}}$[3:0]	J30, M31, P33, T34	I/O	OV$_{DD}$	
PCI_PAR	P32	I/O	OV$_{DD}$	
$\overline{\text{PCI\_FRAME}}$	M32	I/O	OV$_{DD}$	5
$\overline{\text{PCI\_TRDY}}$	N29	I/O	OV$_{DD}$	5
$\overline{\text{PCI\_IRDY}}$	M34	I/O	OV$_{DD}$	5
$\overline{\text{PCI\_STOP}}$	N31	I/O	OV$_{DD}$	5
$\overline{\text{PCI\_DEVSEL}}$	N30	I/O	OV$_{DD}$	5
PCI_IDSEL	J31	I	OV$_{DD}$	
$\overline{\text{PCI\_SERR}}$	N34	I/O	OV$_{DD}$	5
$\overline{\text{PCI\_PERR}}$	N33	I/O	OV$_{DD}$	5
$\overline{\text{PCI\_REQ}}$[0]	D32	I/O	OV$_{DD}$	
$\overline{\text{PCI\_REQ}}$[1]/CPCI1_HS_ES	D34	I	OV$_{DD}$	
$\overline{\text{PCI\_REQ}}$[2:4]	E34, F32, G29	I	OV$_{DD}$	
$\overline{\text{PCI_GNT}}$0	C34	I/O	OV$_{DD}$	
$\overline{\text{PCI_GNT}}$1/CPCI1_HS_LED	D33	O	OV$_{DD}$	
$\overline{\text{PCI_GNT}}$2/CPCI1_HS_ENUM	E33	O	OV$_{DD}$	
$\overline{\text{PCI\_GNT}}$[3:4]	F31, F33	O	OV$_{DD}$	
M66EN	A19	I	OV$_{DD}$	

Table 54. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ[0:63]	D5, A3, C3, D3, C4, B3, C2, D4, D2, E5, G2, H6, E4, F3, G4, G3, H1, J2, L6, M6, H2, K6, L2, M4, N2, P4, R2, T4, P6, P3, R1, T2, AB5, AA3, AD6, AE4, AB4, AC2, AD3, AE6, AE3, AG4, AK5, AK4, AE2, AG6, AK3, AK2, AL2, AL1, AM5, AP5, AM2, AN1, AP4, AN5, AJ7, AN7, AM8, AJ9, AP6, AL7, AL9, AN8	I/O	GV_{DD}	
MECC[0:4]/MSRCID[0:4]	W4, W3, Y3, AA6, T1	I/O	GV_{DD}	
MECC[5]/MDVAL	U1	I/O	GV_{DD}	
MECC[6:7]	Y1, Y6	I/O	GV_{DD}	
MDM[0:8]	B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4	O	GV_{DD}	
MDQS[0:8]	B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2	I/O	GV_{DD}	
MBA[0:1]	AD1, AA5	O	GV_{DD}	
MA[0:14]	W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6	O	GV_{DD}	
$\overline{MWE}$	AF1	O	GV_{DD}	
$\overline{MRAS}$	AF4	O	GV_{DD}	
$\overline{MCAS}$	AG3	O	GV_{DD}	
$\overline{MCS}$[0:3]	AG2, AG1, AK1, AL4	O	GV_{DD}	
MCKE[0:1]	H3, G1	O	GV_{DD}	3
MCK[0:5]	U2, F4, AM3, V3, F2, AN3	O	GV_{DD}	
$\overline{MCK}$[0:5]	U3, E3, AN2, V4, E1, AM4	O	GV_{DD}	
MODT[0:3]	AH3, AJ5, AH1, AJ4	O	GV_{DD}	
MBA[2]	H4	O	GV_{DD}	
MDIC0	AB1	I/O	—	10
MDIC1	AA1	I/O	—	10
Local Bus Controller Interface				
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV_{DD}	
LDP[0]/$\overline{CKSTOP\_OUT}$	AM21	I/O	OV_{DD}	
LDP[1]/$\overline{CKSTOP\_IN}$	AP22	I/O	OV_{DD}	

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Table 54. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LDP[2]/$\overline{\text{LCS}}$[4]	AN22	I/O	OV_{DD}	
LDP[3]/$\overline{\text{LCS}}$[5]	AM22	I/O	OV_{DD}	
LA[27:31]	AK21, AP23, AN23, AP24, AK22	O	OV_{DD}	
$\overline{\text{LCS}}$[0:3]	AN24, AL23, AP25, AN25	O	OV_{DD}	
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/ $\overline{\text{LBS}}$[0:3]	AK23, AP26, AL24, AM25	O	OV_{DD}	
LBCTL	AN26	O	OV_{DD}	
LALE	AK24	O	OV_{DD}	
LGPL0/LSDA10/ cfg_reset_source0	AP27	I/O	OV_{DD}	
LGPL1/$\overline{\text{LSDWE}}$/ cfg_reset_source1	AL25	I/O	OV_{DD}	
LGPL2/ $\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	AJ24	O	OV_{DD}	
LGPL3/$\overline{\text{LSDCAS}}$/ cfg_reset_source2	AN27	I/O	OV_{DD}	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	AP28	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	AL26	I/O	OV_{DD}	
LCKE	AM27	O	OV_{DD}	
LCLK[0:2]	AN28, AK26, AP29	O	OV_{DD}	
LSYNC_OUT	AM12	O	OV_{DD}	
LSYNC_IN	AJ10	I	OV_{DD}	
General Purpose I/O Timers				
GPIO1[0]/$\overline{\text{DMA\_DREQ0}}$/ GTM1_TIN1/ GTM2_TIN2	F24	I/O	OV_{DD}	
GPIO1[1]/$\overline{\text{DMA\_DACK0}}$/ $\overline{\text{GTM1\_TGATE1}}$/ $\overline{\text{GTM2\_TGATE2}}$	E24	I/O	OV_{DD}	
GPIO1[2]/$\overline{\text{DMA\_DDONE0}}$/ $\overline{\text{GTM1\_TOUT1}}$	B25	I/O	OV_{DD}	
GPIO1[3]/$\overline{\text{DMA\_DREQ1}}$/ GTM1_TIN2/ GTM2_TIN1	D24	I/O	OV_{DD}	
GPIO1[4]/$\overline{\text{DMA\_DACK1}}$/ $\overline{\text{GTM1\_TGATE2}}$/ $\overline{\text{GTM2\_TGATE1}}$	A25	I/O	OV_{DD}	

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Table 54. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO1[5]/$\overline{\text{DMA\_DDONE1}}$/ $\overline{\text{GTM1\_TOUT2}}$/ $\overline{\text{GTM2\_TOUT1}}$	B24	I/O	OV$_{DD}$	
GPIO1[6]/$\overline{\text{DMA\_DREQ2}}$/ GTM1_TIN3/ GTM2_TIN4	A24	I/O	OV$_{DD}$	
GPIO1[7]/$\overline{\text{DMA\_DACK2}}$/ $\overline{\text{GTM1\_TGATE3}}$/ $\overline{\text{GTM2\_TGATE4}}$	D23	I/O	OV$_{DD}$	
GPIO1[8]/$\overline{\text{DMA\_DDONE2}}$/ $\overline{\text{GTM1\_TOUT3}}$	B23	I/O	OV$_{DD}$	
GPIO1[9]/$\overline{\text{DMA\_DREQ3}}$/ GTM1_TIN4/ GTM2_TIN3	A23	I/O	OV$_{DD}$	
GPIO1[10]/$\overline{\text{DMA\_DACK3}}$/ $\overline{\text{GTM1\_TGATE4}}$/ $\overline{\text{GTM2\_TGATE3}}$	F22	I/O	OV$_{DD}$	
GPIO1[11]/$\overline{\text{DMA\_DDONE3}}$/ $\overline{\text{GTM1\_TOUT4}}$/ $\overline{\text{GTM2\_TOUT3}}$	E22	I/O	OV$_{DD}$	
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	A26	I/O	OV$_{DD}$	
MPH1_D1_SER_TXD/DR_D1_SER_TXD	B26	I/O	OV$_{DD}$	
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	D25	I/O	OV$_{DD}$	
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV$_{DD}$	
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV$_{DD}$	
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV$_{DD}$	
MPH1_D6_SER_RCV/DR_D6_SER_RCV	D26	I/O	OV$_{DD}$	
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	E26	I/O	OV$_{DD}$	
MPH1_NXT/DR_SESS_VLD_NXT	D27	I	OV$_{DD}$	
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	A28	I/O	OV$_{DD}$	
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	F26	O	OV$_{DD}$	
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	E27	I	OV$_{DD}$	
MPH1_PCTL0/DR_TX_VALID_PCTL0	A29	O	OV$_{DD}$	
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	D28	O	OV$_{DD}$	

Table 54. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_CLK/DR_CLK	B29	I	OV$_{DD}$	
USB Port 0				
MPH0_D0_ENABLEN/ DR_D8_CHGVBUS	C29	I/O	OV$_{DD}$	
MPH0_D1_SER_TXD/ DR_D9_DCHGVBUS	A30	I/O	OV$_{DD}$	
MPH0_D2_VMO_SE0/ DR_D10_DPPD	E28	I/O	OV$_{DD}$	
MPH0_D3_SPEED/ DR_D11_DMMD	B30	I/O	OV$_{DD}$	
MPH0_D4_DP/ DR_D12_VBUS_VLD	C30	I/O	OV$_{DD}$	
MPH0_D5_DM/ DR_D13_SESS_END	A31	I/O	OV$_{DD}$	
MPH0_D6_SER_RCV/DR_D14	B31	I/O	OV$_{DD}$	
MPH0_D7_DRVVBUS/ DR_D15_IDPULLUP	C31	I/O	OV$_{DD}$	
MPH0_NXT/ DR_RX_ACTIVE_ID	B32	I	OV$_{DD}$	
MPH0_DIR_DPPULLUP/ DR_RESET	A32	I/O	OV$_{DD}$	
MPH0_STP_SUSPEND/ DR_TX_READY	A33	I/O	OV$_{DD}$	
MPH0_PWRFAULT/ DR_RX_VALIDH	C32	I	OV$_{DD}$	
MPH0_PCTL0/ DR_LINE_STATE0	D31	I/O	OV$_{DD}$	
MPH0_PCTL1/ DR_LINE_STATE1	E30	I/O	OV$_{DD}$	
MPH0_CLK/DR_RX_VALID	B33	I	OV$_{DD}$	
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	AN33	O	OV$_{DD}$	2
$\overline{\text{IRQ0}}$/$\overline{\text{MCP\_IN}}$/GPIO2[12]	C19	I/O	OV$_{DD}$	
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	C22, A22, D21, C21, B21	I/O	OV$_{DD}$	
$\overline{\text{IRQ}}$[6]/GPIO2[18]/ CKSTOP_OUT	A21	I/O	OV$_{DD}$	

Table 54. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ}}$[7]/GPIO2[19]/ CKSTOP_IN	C20	I/O	OV$_{DD}$	
Ethernet Management Interface				
EC_MDC	A7	O	LV$_{DD1}$	
EC_MDIO	E9	I/O	LV$_{DD1}$	2
Gigabit Reference Clock				
EC_GTX_CLK125	C8	I	LV$_{DD1}$	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	A17	I/O	OV$_{DD}$	
TSEC1_CRS/GPIO2[21]	F12	I/O	LV$_{DD1}$	
TSEC1_GTX_CLK	D10	O	LV$_{DD1}$	3
TSEC1_RX_CLK	A11	I	LV$_{DD1}$	
TSEC1_RX_DV	B11	I	LV$_{DD1}$	
TSEC1_RX_ER/GPIO2[26]	B17	I/O	OV$_{DD}$	
TSEC1_RXD[7:4]/ GPIO2[22:25]	B16, D16, E16, F16	I/O	OV$_{DD}$	
TSEC1_RXD[3:0]	E10, A8, F10, B8	I	LV$_{DD1}$	
TSEC1_TX_CLK	D17	I	OV$_{DD}$	
TSEC1_TXD[7:4]/GPIO2[27:30]	A15, B15, A14, B14	I/O	OV$_{DD}$	
TSEC1_TXD[3:0]	A10, E11, B10, A9	O	LV$_{DD1}$	
TSEC1_TX_EN	B9	O	LV$_{DD1}$	
TSEC1_TX_ER/GPIO2[31]	A16	I/O	OV$_{DD}$	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	C14	I/O	OV$_{DD}$	
TSEC2_CRS/GPIO1[22]	D6	I/O	LV$_{DD2}$	
TSEC2_GTX_CLK	A4	O	LV$_{DD2}$	
TSEC2_RX_CLK	B4	I	LV$_{DD2}$	
TSEC2_RX_DV/GPIO1[23]	E6	I/O	LV$_{DD2}$	
TSEC2_RXD[7:4]/GPIO1[26:29]	A13, B13, C13, A12	I/O	OV$_{DD}$	
TSEC2_RXD[3:0]/GPIO1[13:16]	D7, A6, E8, B7	I/O	LV$_{DD2}$	
TSEC2_RX_ER/GPIO1[25]	D14	I/O	OV$_{DD}$	
TSEC2_TXD[7]/GPIO1[31]	B12	I/O	OV$_{DD}$	

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Table 54. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TXD[6]/ DR_XCVR_TERM_SEL	C12	O	OV_{DD}	
TSEC2_TXD[5]/ DR_UTMI_OPMODE1	D12	O	OV_{DD}	
TSEC2_TXD[4]/ DR_UTMI_OPMODE0	E12	O	OV_{DD}	
TSEC2_TXD[3:0]/GPIO1[17:20]	B5, A5, F8, B6	I/O	LV_{DD2}	
TSEC2_TX_ER/GPIO1[24]	F14	I/O	OV_{DD}	
TSEC2_TX_EN/GPIO1[12]	C5	I/O	LV_{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	E14	I/O	OV_{DD}	
DUART				
UART_SOUT[1:2]/ MSRCID[0:1]/LSRCID[0:1]	AK27, AN29	O	OV_{DD}	
UART_SIN[1:2]/ MSRCID[2:3]/LSRCID[2:3]	AL28, AM29	I/O	OV_{DD}	
$\overline{UART\_CTS}$[1]/ MSRCID4/LSRCID4	AP30	I/O	OV_{DD}	
$\overline{UART\_CTS}$[2]/ MDVAL/ LDVAL	AN30	I/O	OV_{DD}	
$\overline{UART\_RTS}$[1:2]	AP31, AM30	O	OV_{DD}	
I²C interface				
IIC1_SDA	AK29	I/O	OV_{DD}	2
IIC1_SCL	AP32	I/O	OV_{DD}	2
IIC2_SDA	AN31	I/O	OV_{DD}	2
IIC2_SCL	AM31	I/O	OV_{DD}	2
SPI				
SPIMOSI/$\overline{LCS}$[6]	AN32	I/O	OV_{DD}	
SPIMISO/$\overline{LCS}$[7]	AP33	I/O	OV_{DD}	
SPICLK	AK30	I/O	OV_{DD}	
SPISEL	AL31	I	OV_{DD}	
Clocks				
PCI_CLK_OUT[0:2]	AN9, AP9, AM10	O	OV_{DD}	
PCI_CLK_OUT[3]/$\overline{LCS}$[6]	AN10	O	OV_{DD}	
PCI_CLK_OUT[4]/$\overline{LCS}$[7]	AJ11	O	OV_{DD}	

Table 54. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV$_{DD}$	
PCI_SYNC_OUT	AP11	O	OV$_{DD}$	3
RTC/PIT_CLOCK	AM32	I	OV$_{DD}$	
CLKIN	AM9	I	OV$_{DD}$	
JTAG				
TCK	E20	I	OV$_{DD}$	
TDI	F20	I	OV$_{DD}$	4
TDO	B20	O	OV$_{DD}$	3
TMS	A20	I	OV$_{DD}$	4
$\overline{\text{TRST}}$	B19	I	OV$_{DD}$	4
Test				
TEST	D22	I	OV$_{DD}$	6
TEST_SEL	AL13	I	OV$_{DD}$	7
PMC				
$\overline{\text{QUIESCE}}$	A18	O	OV$_{DD}$	
System Control				
$\overline{\text{PORESET}}$	C18	I	OV$_{DD}$	
$\overline{\text{HRESET}}$	B18	I/O	OV$_{DD}$	1
$\overline{\text{SRESET}}$	D18	I/O	OV$_{DD}$	2
Thermal Management				
THERM0	K32	I	—	9
Power and Ground Signals				
AV$_{DD}$1	L31	Power for e300 PLL (1.2 V)	AV$_{DD}$1	
AV$_{DD}$2	AP12	Power for system PLL (1.2 V)	AV$_{DD}$2	
AV$_{DD}$3	AE1	Power for DDR DLL (1.2 V)	—	
AV$_{DD}$4	AJ13	Power for LBIU DLL (1.2 V)	AV$_{DD}$4	

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Table 54. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34	—	—	
GV$_{DD}$	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O Voltage (2.5 V)	GV$_{DD}$	
LV$_{DD1}$	C9, D11	Power for Three Speed Ethernet #1 and for Ethernet Management Interface I/O (2.5V, 3.3V)	LV$_{DD1}$	
LV$_{DD2}$	C6, D9	Power for Three Speed Ethernet #2 I/O (2.5V, 3.3V)	LV$_{DD2}$	
V$_{DD}$	E19, E29, F7, F9, F11,F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for Core (1.2 V)	V$_{DD}$	
OV$_{DD}$	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV$_{DD}$	

Table 54. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF1	M3	I	DDR Reference Voltage	
MVREF2	AD2	I	DDR Reference Voltage	
No Connection				
NC	W32, AA31, AA32, AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30, AC32, AE32, AH31, AL32, AG34, AE33, AF32, AE34, AF34, AF33, AG33, AG32, AL11, AM11, AP10, Y32, Y34, Y31, Y33	—	—	

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}

2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.

3. During reset, this output is actively driven rather than three-stated.

4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.

5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.

6. This pin must always be tied to GND

7. This pin must always be pulled up to OV_{DD}

8. This pin must always be left not connected.

9. Thermal sensitive resistor.

10. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.

Table 52 provides the pin-out listing for the MPC8347EA, 620 PBGA package.

Table 55. MPC8347EA (PBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI1_INTA/IRQ_OUT	D20	O	OV_{DD}	2
PCI1_RESET_OUT	B21	O	OV_{DD}	
PCI1_AD[31:0]	E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8	I/O	OV_{DD}	
PCI1_C/BE[3:0]	A17, A14, A11, B10	I/O	OV_{DD}	

Table 55. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_PAR	D13	I/O	OV$_{DD}$	
$\overline{\text{PCI1\_FRAME}}$	B14	I/O	OV$_{DD}$	5
$\overline{\text{PCI1\_TRDY}}$	A13	I/O	OV$_{DD}$	5
$\overline{\text{PCI1\_IRDY}}$	E13	I/O	OV$_{DD}$	5
$\overline{\text{PCI1\_STOP}}$	C13	I/O	OV$_{DD}$	5
$\overline{\text{PCI1\_DEVSEL}}$	B13	I/O	OV$_{DD}$	5
PCI1_IDSEL	C17	I	OV$_{DD}$	
$\overline{\text{PCI1\_SERR}}$	C12	I/O	OV$_{DD}$	5
$\overline{\text{PCI1\_PERR}}$	B12	I/O	OV$_{DD}$	5
$\overline{\text{PCI1\_REQ}}$[0]	A21	I/O	OV$_{DD}$	
$\overline{\text{PCI1\_REQ}}$[1]/ CPCI1_HS_ES	C19	I	OV$_{DD}$	
$\overline{\text{PCI1\_REQ}}$[2:4]	C18, A19, E20	I	OV$_{DD}$	
$\overline{\text{PCI1_GNT}}$0	B20	I/O	OV$_{DD}$	
$\overline{\text{PCI1_GNT}}$1/ CPCI1_HS_LED	C20	O	OV$_{DD}$	
$\overline{\text{PCI1_GNT}}$2/ CPCI1_HS_ENUM	B19	O	OV$_{DD}$	
$\overline{\text{PCI1\_GNT}}$[3:4]	A20, E18	O	OV$_{DD}$	
M66EN	L26	I	OV$_{DD}$	
DDR SDRAM Memory Interface				
MDQ[0:63]	AC25, AD27, AD25, AH27, AE28, AD26, AD24, AF27, AF25, AF28, AH24, AG26, AE25, AG25, AH26, AH25, AG22, AH22, AE21, AD19, AE22, AF23, AE19, AG20, AG19, AD17, AE16, AF16, AF18, AG18, AH17, AH16, AG9, AD12, AG7, AE8, AD11, AH9, AH8, AF6, AF8, AE6, AF1, AE4, AG8, AH3, AG3, AG4, AH2, AD7, AB4, AB3, AG1, AD5, AC2, AC1, AC4, AA3, Y4, AA4, AB1, AB2, Y5, Y3	I/O	GV$_{DD}$	
MECC[0:4]/MSRCID[0:4]	AG13, AE14, AH12, AH10, AE15	I/O	GV$_{DD}$	
MECC[5]/MDVAL	AH14	I/O	GV$_{DD}$	
MECC[6:7]	AE13, AH11	I/O	GV$_{DD}$	
MDM[0:8]	AG28, AG24, AF20, AG17, AE9, AH5, AD1, AA2, AG12	O	GV$_{DD}$	

Table 55. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MDQS[0:8]	AE27, AE26, AE20, AH18, AG10, AF5, AC3, AA1, AH13	I/O	GV$_{DD}$	
MBA[0:1]	AF10, AF11	O	GV$_{DD}$	
MA[0:14]	AF13, AF15, AG16, AD16, AF17, AH20, AH19, AH21, AD18, AG21, AD13, AF21, AF22, AE1, AA5	O	GV$_{DD}$	
$\overline{MWE}$	AD10	O	GV$_{DD}$	
$\overline{MRAS}$	AF7	O	GV$_{DD}$	
$\overline{MCAS}$	AG6	O	GV$_{DD}$	
$\overline{MCS}$[0:3]	AE7, AH7, AH4, AF2	O	GV$_{DD}$	
MCKE[0:1]	AG23, AH23	O	GV$_{DD}$	3
MCK[0:5]	AH15, AE24, AE2, AF14, AE23, AD3	O	GV$_{DD}$	
$\overline{MCK}$[0:5]	AG15, AD23, AE3, AG14, AF24, AD2	O	GV$_{DD}$	
MODT[0:3]	AG5, AD4, AH6, AF4	O	GV$_{DD}$	
MBA[2]	AD22	O	GV$_{DD}$	
MDIC0	AG11	I/O	—	9
MDIC1	AF12	I/O	—	9
Local Bus Controller Interface				
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV$_{DD}$	
LDP[0]/$\overline{CKSTOP\_OUT}$	H1	I/O	OV$_{DD}$	
LDP[1]/$\overline{CKSTOP\_IN}$	K5	I/O	OV$_{DD}$	
LDP[2]/LCS[4]	H2	I/O	OV$_{DD}$	
LDP[3]/LCS[5]	G1	I/O	OV$_{DD}$	
LA[27:31]	J4, H3, G2, F1, G3	O	OV$_{DD}$	
$\overline{LCS}$[0:3]	J5, H4, F2, E1	O	OV$_{DD}$	
$\overline{LWE}$[0:3]/LSDDQM[0:3]/ $\overline{LBS}$[0:3]	F3, G4, D1, E2	O	OV$_{DD}$	
LBCTL	H5	O	OV$_{DD}$	
LALE	E3	O	OV$_{DD}$	
LGPL0/LSDA10/ cfg_reset_source0	F4	I/O	OV$_{DD}$	
LGPL1/$\overline{LSDWE}$/ cfg_reset_source1	D2	I/O	OV$_{DD}$	

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Table 55. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LGPL2/ $\overline{\text{LSDRAS}}$/LOE	C1	O	OV$_{DD}$	
LGPL3/$\overline{\text{LSDCAS}}$/ cfg_reset_source2	C2	I/O	OV$_{DD}$	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	C3	I/O	OV$_{DD}$	
LGPL5/cfg_clkin_div	B3	I/O	OV$_{DD}$	
LCKE	E4	O	OV$_{DD}$	
LCLK[0:2]	D4, A3, C4	O	OV$_{DD}$	
LSYNC_OUT	U3	O	OV$_{DD}$	
LSYNC_IN	Y2	I	OV$_{DD}$	
General Purpose I/O Timers				
GPIO1[0]/$\overline{\text{DMA\_DREQ0}}$/ GTM1_TIN1/ GTM2_TIN2	D27	I/O	OV$_{DD}$	
GPIO1[1]/$\overline{\text{DMA\_DACK0}}$/ $\overline{\text{GTM1\_TGATE1}}$/ $\overline{\text{GTM2\_TGATE2}}$	E26	I/O	OV$_{DD}$	
GPIO1[2]/$\overline{\text{DMA\_DDONE0}}$/ $\overline{\text{GTM1\_TOUT1}}$	D28	I/O	OV$_{DD}$	
GPIO1[3]/$\overline{\text{DMA\_DREQ1}}$/ GTM1_TIN2/ GTM2_TIN1	G25	I/O	OV$_{DD}$	
GPIO1[4]/$\overline{\text{DMA\_DACK1}}$/ $\overline{\text{GTM1\_TGATE2}}$/ $\overline{\text{GTM2\_TGATE1}}$	J24	I/O	OV$_{DD}$	
GPIO1[5]/$\overline{\text{DMA\_DDONE1}}$/ $\overline{\text{GTM1\_TOUT2}}$/ $\overline{\text{GTM2\_TOUT1}}$	F26	I/O	OV$_{DD}$	
GPIO1[6]/$\overline{\text{DMA\_DREQ2}}$/ GTM1_TIN3/ GTM2_TIN4	E27	I/O	OV$_{DD}$	
GPIO1[7]/$\overline{\text{DMA\_DACK2}}$/ $\overline{\text{GTM1\_TGATE3}}$/ $\overline{\text{GTM2\_TGATE4}}$	E28	I/O	OV$_{DD}$	
GPIO1[8]/$\overline{\text{DMA\_DDONE2}}$/ $\overline{\text{GTM1\_TOUT3}}$	H25	I/O	OV$_{DD}$	
GPIO1[9]/$\overline{\text{DMA\_DREQ3}}$/ GTM1_TIN4/ GTM2_TIN3	F27	I/O	OV$_{DD}$	

Table 55. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO1[10]/$\overline{\text{DMA\_DACK3}}$/ $\overline{\text{GTM1\_TGATE4}}$/ $\overline{\text{GTM2\_TGATE3}}$	K24	I/O	OV$_{DD}$	
GPIO1[11]/$\overline{\text{DMA\_DDONE3}}$/ $\overline{\text{GTM1\_TOUT4}}$/ $\overline{\text{GTM2\_TOUT3}}$	G26	I/O	OV$_{DD}$	
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	C28	I/O	OV$_{DD}$	
MPH1_D1_SER_TXD/DR_D1_SER_RXD	F25	I/O	OV$_{DD}$	
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	B28	I/O	OV$_{DD}$	
MPH1_D3_SPEED/DR_D3_SPEED	C27	I/O	OV$_{DD}$	
MPH1_D4_DP/DR_D4_DP	D26	I/O	OV$_{DD}$	
MPH1_D5_DM/DR_D5_DM	E25	I/O	OV$_{DD}$	
MPH1_D6_SER_RCV/DR_D6_SER_RCV	C26	I/O	OV$_{DD}$	
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	D25	I/O	OV$_{DD}$	
MPH1_NXT/DR_SESS_VLD_NXT	B26	I	OV$_{DD}$	
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	E24	I/O	OV$_{DD}$	
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	A27	O	OV$_{DD}$	
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	C25	I	OV$_{DD}$	
MPH1_PCTL0/DR_TX_VALID_PCTL0	A26	O	OV$_{DD}$	
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	B25	O	OV$_{DD}$	
MPH1_CLK/DR_CLK	A25	I	OV$_{DD}$	
USB Port 0				
MPH0_D0_ENABLEN/ DR_D8_CHGVBUS	D24	I/O	OV$_{DD}$	
MPH0_D1_SER_TXD/ DR_D9_DCHGVBUS	C24	I/O	OV$_{DD}$	
MPH0_D2_VMO_SE0/ DR_D10_DPPD	B24	I/O	OV$_{DD}$	
MPH0_D3_SPEED/ DR_D11_DMMD	A24	I/O	OV$_{DD}$	
MPH0_D4_DP/ DR_D12_VBUS_VLD	D23	I/O	OV$_{DD}$	

Table 55. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH0_D5_DM/ DR_D13_SESS_END	C23	I/O	OV$_{DD}$	
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV$_{DD}$	
MPH0_D7_DRVVBUS/ DR_D15_IDPULLUP	A23	I/O	OV$_{DD}$	
MPH0_NXT/ DR_RX_ACTIVE_ID	D22	I	OV$_{DD}$	
MPH0_DIR_DPPULLUP/ DR_RESET	C22	I/O	OV$_{DD}$	
MPH0_STP_SUSPEND/ DR_TX_READY	B22	I/O	OV$_{DD}$	
MPH0_PWRFAULT/ DR_RX_VALIDH	A22	I	OV$_{DD}$	
MPH0_PCTL0/ DR_LINE_STATE0	E21	I/O	OV$_{DD}$	
MPH0_PCTL1/ DR_LINE_STATE1	D21	I/O	OV$_{DD}$	
MPH0_CLK/DR_RX_VALID	C21	I	OV$_{DD}$	
Programmable Interrupt Controller				
MCP_OUT	E8	O	OV$_{DD}$	2
IRQ0/MCP_IN/GPIO2[12]	J28	I/O	OV$_{DD}$	
IRQ[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV$_{DD}$	
IRQ[6]/GPIO2[18]/ CKSTOP_OUT	G28	I/O	OV$_{DD}$	
IRQ[7]/GPIO2[19]/ CKSTOP_IN	J26	I/O	OV$_{DD}$	
Ethernet Management Interface				
EC_MDC	Y24	O	LV$_{DD1}$	
EC_MDIO	Y25	I/O	LV$_{DD1}$	2
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV$_{DD1}$	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV$_{DD}$	
TSEC1_CRS/GPIO2[21]	U25	I/O	LV$_{DD1}$	
TSEC1_GTX_CLK	V24	O	LV$_{DD1}$	3

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Table 55. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_CLK	U26	I	LV_{DD1}	
TSEC1_RX_DV	U24	I	LV_{DD1}	
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV_{DD}	
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV_{DD}	
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV_{DD1}	
TSEC1_TX_CLK	N25	I	OV_{DD}	
TSEC1_TXD[7:4]/GPIO2[27:30]	N28, P25, P26, P27	I/O	OV_{DD}	
TSEC1_TXD[3:0]	V28, V27, V26, W28	O	LV_{DD1}	
TSEC1_TX_EN	W27	O	LV_{DD1}	
TSEC1_TX_ER/GPIO2[31]	N24	I/O	OV_{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	P28	I/O	OV_{DD}	
TSEC2_CRS/GPIO1[22]	AC28	I/O	LV_{DD2}	
TSEC2_GTX_CLK	AC27	O	LV_{DD2}	
TSEC2_RX_CLK	AB25	I	LV_{DD2}	
TSEC2_RX_DV/GPIO1[23]	AC26	I/O	LV_{DD2}	
TSEC2_RXD[7:4]/GPIO1[26:29]	R28, T24, T25, T26	I/O	OV_{DD}	
TSEC2_RXD[3:0]/GPIO1[13:16]	AA25, AA26, AA27, AA28	I/O	LV_{DD2}	
TSEC2_RX_ER/GPIO1[25]	R25	I/O	OV_{DD}	
TSEC2_TXD[7]/GPIO1[31]	T27	I/O	OV_{DD}	
TSEC2_TXD[6]/DR_XCVR_TERM_SEL	T28	O	OV_{DD}	
TSEC2_TXD[5]/DR_UTMI_OPMODE1	U28	O	OV_{DD}	
TSEC2_TXD[4]/DR_UTMI_OPMODE0	U27	O	OV_{DD}	
TSEC2_TXD[3:0]/GPIO1[17:20]	AB26, AB27, AA24, AB28	I/O	LV_{DD2}	
TSEC2_TX_ER/GPIO1[24]	R27	I/O	OV_{DD}	
TSEC2_TX_EN/GPIO1[12]	AD28	I/O	LV_{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	R26	I/O	OV_{DD}	
DUART				
UART_SOUT[1:2]/ MSRCID[0:1]/LSRCID[0:1]	B4, A4	O	OV_{DD}	
UART_SIN[1:2]/ MSRCID[2:3]/LSRCID[2:3]	D5, C5	I/O	OV_{DD}	

Table 55. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{UART\_CTS}$[1]/ MSRCID4/LSRCID4	B5	I/O	OV$_{DD}$	
$\overline{UART\_CTS}$[2]/ MDVAL/ LDVAL	A5	I/O	OV$_{DD}$	
$\overline{UART\_RTS}$[1:2]	D6, C6	O	OV$_{DD}$	
I^{2}C interface				
IIC1_SDA	E5	I/O	OV$_{DD}$	2
IIC1_SCL	A6	I/O	OV$_{DD}$	2
IIC2_SDA	B6	I/O	OV$_{DD}$	2
IIC2_SCL	E7	I/O	OV$_{DD}$	2
SPI				
SPIMOSI/$\overline{LCS}$[6]	D7	I/O	OV$_{DD}$	
SPIMISO/$\overline{LCS}$[7]	C7	I/O	OV$_{DD}$	
SPICLK	B7	I/O	OV$_{DD}$	
SPISEL	A7	I	OV$_{DD}$	
Clocks				
PCI_CLK_OUT[0:2]	Y1, W3, W2	O	OV$_{DD}$	
PCI_CLK_OUT[3]/$\overline{LCS}$[6]	W1	O	OV$_{DD}$	
PCI_CLK_OUT[4]/$\overline{LCS}$[7]	V3	O	OV$_{DD}$	
PCI_SYNC_IN/PCI_CLOCK	U4	I	OV$_{DD}$	
PCI_SYNC_OUT	U5	O	OV$_{DD}$	3
RTC/PIT_CLOCK	E9	I	OV$_{DD}$	
CLKIN	W5	I	OV$_{DD}$	
JTAG				
TCK	H27	I	OV$_{DD}$	
TDI	H28	I	OV$_{DD}$	4
TDO	M24	O	OV$_{DD}$	3
TMS	J27	I	OV$_{DD}$	4
$\overline{TRST}$	K26	I	OV$_{DD}$	4
Test				
TEST	F28	I	OV$_{DD}$	6
TEST_SEL	T3	I	OV$_{DD}$	6

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Table 55. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PMC				
$\overline{\text{QUIESCE}}$	K27	O	OV_{DD}	
System Control				
$\overline{\text{PORESET}}$	K28	I	OV_{DD}	
$\overline{\text{HRESET}}$	M25	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	L27	I/O	OV_{DD}	2
Thermal Management				
THERM0	B15	I	—	8
Power and Ground Signals				
$AV_{DD}1$	C15	Power for e300 PLL (1.2 V)	$AV_{DD}1$	
$AV_{DD}2$	U1	Power for system PLL (1.2 V)	$AV_{DD}2$	
$AV_{DD}3$	AF9	Power for DDR DLL (1.2 V)	—	
$AV_{DD}4$	U2	Power for LBIU DLL (1.2 V)	$AV_{DD}4$	
GND	A2, B1, B2, D10, D18, E6, E14, E22, F9, F12, F15, F18, F21, F24, G5, H6, J23, L4, L6, L12, L13, L14, L15, L16, L17, M11, M12, M13, M14, M15, M16, M17, M18, M23, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, P24, R5, R11, R12, R13, R14, R15, R16, R17, R18, R23, T11, T12, T13, T14, T15, T16, T17, T18, U6, U11, U12, U13, U14, U15, U16, U17, U18, V12, V13, V14, V15, V16, V17, V23, V25, W4, Y6, AA23, AB24, AC5, AC8, AC11, AC14, AC17, AC20, AD9, AD15, AD21, AE12, AE18, AF3, AF26	—	—	
GV_{DD}	U9, V9, W10, W19, Y11, Y12, Y14, Y15, Y17, Y18, AA6, AB5, AC9, AC12, AC15, AC18, AC21, AC24, AD6, AD8, AD14, AD20, AE5, AE11, AE17, AG2, AG27	Power for DDR DRAM I/O Voltage (2.5 V)	GV_{DD}	

Table 55. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV$_{DD1}$	U20, W25	Power for Three Speed Ethernet #1 and for Ethernet Management Interface I/O (2.5V, 3.3V)	LV$_{DD1}$	
LV$_{DD2}$	V20, Y23	Power for Three Speed Ethernet #2 I/O (2.5V, 3.3V)	LV$_{DD2}$	
V$_{DD}$	J11, J12, J15, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, L10, L11, L18, L19, M10, M19, N10, N19, P9, P10, P19, R10, R19, R20, T10, T19, U10, U19, V10, V11, V18, V19, W11, W12, W13, W14, W15, W16, W17, W18	Power for Core (1.2 V)	V$_{DD}$	
OV$_{DD}$	B27, D3, D11, D19, E15, E23, F5, F8, F11, F14, F17, F20, G24, H23, H24, J6, J14, J17, J18, K4, L9, L20, L23, L25, M6, M9, M20, P5, P20, P23, R6, R9, R24, U23, V4, V6	PCI, 10/100 Ethernet, and other Standard (3.3 V)	OV$_{DD}$	
MVREF1	AF19	I	DDR Reference Voltage	
MVREF2	AE10	I	DDR Reference Voltage	
No Connection				
NC	V1, V2, V5			

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV$_{DD}$

2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV$_{DD}$.

3. During reset, this output is actively driven rather than three-stated.

4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.

5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.

6. .This pin must always be tied to GND

7. This pin must always be left not connected

8. Thermal sensitive resistor.

9. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.

19 Clocking

shows the internal distribution of the clocks.
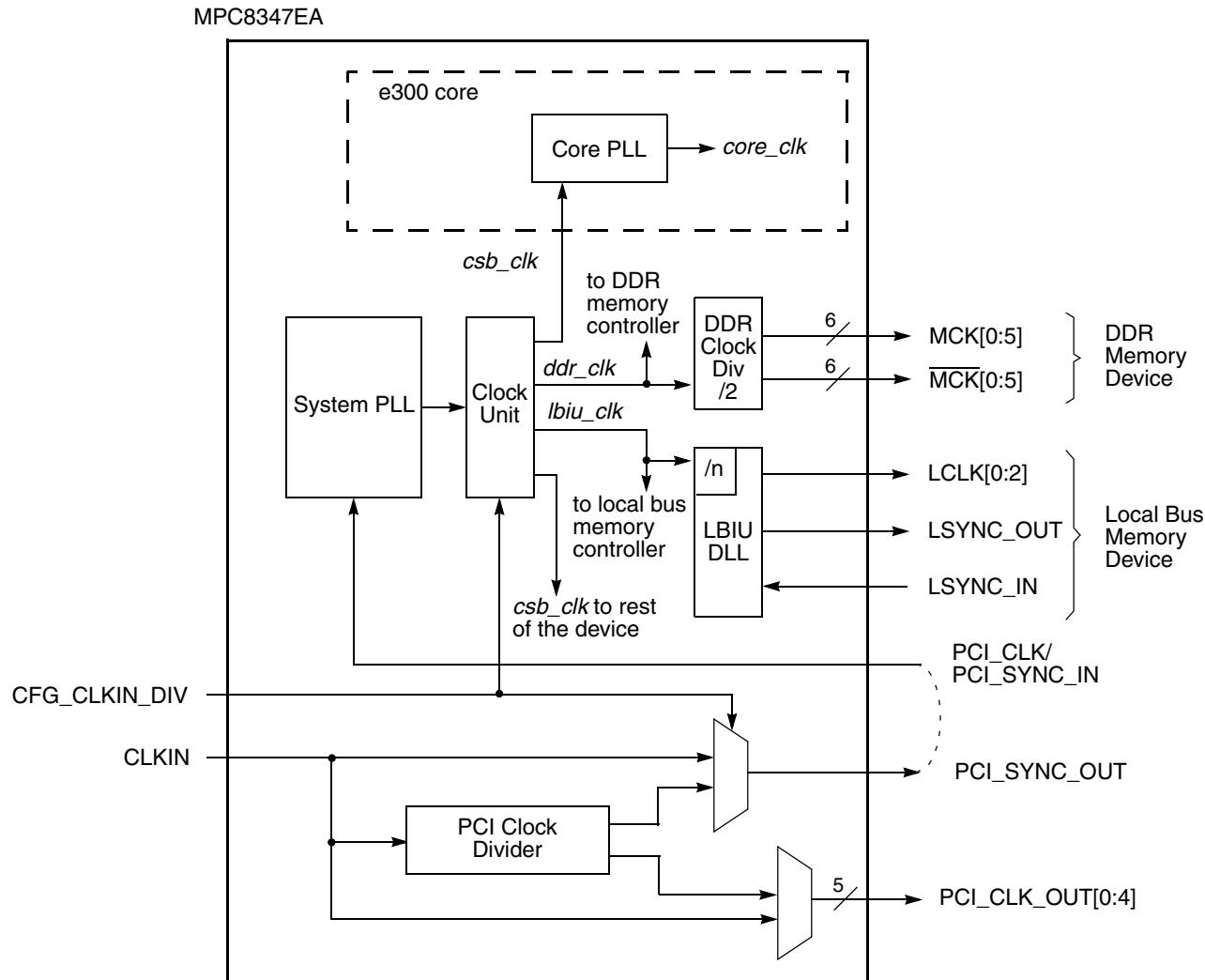
Figure 40. MPC8347EA Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8347EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8347EA to function. When the MPC8347EA is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

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As shown in Figure 40, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \text{CFG\_CLKIN\_DIV})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349EA Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

ddr_clk is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + \text{RCWL[LBIUCM]})$$

lbiu_clk is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. Table 56 specifies which units have a configurable clock frequency.

Table 56. Configurable Clock Units

Unit	Default Frequency	Options
TSEC1	*csb_clk*/3	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
TSEC2, I²C1	*csb_clk*/3	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
Security Core	*csb_clk*/3	Off, *csb_clk*, csb_clk/2, *csb_clk*/3
USB DR, USB MPH	*csb_clk*/3	Off, csb_clk, csb_clk/2, *csb_clk*/3
PCI and DMA complex	*csb_clk*	Off, *csb_clk*

Table 57 provides the operating frequencies for the MPC8347EA TBGA under recommended operating conditions (see Table 2).

Table 57. Operating Frequencies for TBGA

Characteristic [1]	533 MHz	667 MHz	Unit
e300 core frequency (*core_clk*)	266–533	266–667	MHz
Coherent system bus frequency (*csb_clk*)	100–266	100–333	MHz
DDR and DDR2 memory bus frequency (MCLK) [2]	100–200	100–200	MHz
Local bus frequency (LCLK*n*) [3]	16.67–133	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66	25–66	MHz
Security core maximum internal operating frequency	133	166	MHz
USB_DR, USB_MPH maximum internal operating frequency	133	166	MHz

[1] The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM]and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

[2] The DDR data rate is 2x the DDR memory bus frequency.

[3] The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

Table 58 provides the operating frequencies for the MPC8347EA PBGA under recommended operating conditions.

Table 58. Operating Frequencies for PBGA

Characteristic [1]	266 MHz	333 MHz	400 MHz	Unit
e300 core frequency (*core_clk*)	200–266	200–333	200–400	MHz
Coherent system bus frequency (*csb_clk*)	100–266			MHz
DDR memory bus frequency (MCLK) [2]	100–133			MHz
Local bus frequency (LCLK*n*) [3]	16.67–133			MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66			MHz
Security core maximum internal operating frequency	133			MHz
USB_DR, USB_MPH maximum internal operating frequency	133			MHz

[1] The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM]and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

[2] The DDR data rate is 2x the DDR memory bus frequency.

[3] The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

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19.1   System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 59 shows the multiplication factor encodings for the system PLL.

Table 59. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

As described in Section 19, "Clocking," The LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 60 and Table 61 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 60. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at reset [1]	SPMF	csb_clk : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				

[1] CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

[2] CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 61. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at reset [1]	SPMF	csb_clk : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
high	0010	4 : 1		100	133	266
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

[1] CFG_CLKIN_DIV doubles csb_clk if set high.

[2] CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

19.2   Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 62 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 62 should be considered as reserved.

NOTE

Core VCO frequency = Core frequency × VCO divider
VCO divider must be set properly so that the core VCO frequency is in the
range of 800–1800 MHz.

Table 62. e300 Core PLL Configuration

RCWL[COREPLL]			core_clk : csb_clk Ratio	VCO divider [1]
0–1	2–5	6		
nn	0000	n	PLL bypassed (PLL off, csb_clk clocks core directly)	PLL bypassed (PLL off, csb_clk clocks core directly)
00	0001	0	1:1	2
01	0001	0	1:1	4
10	0001	0	1:1	8
11	0001	0	1:1	8
00	0001	1	1.5:1	2
01	0001	1	1.5:1	4
10	0001	1	1.5:1	8
11	0001	1	1.5:1	8
00	0010	0	2:1	2
01	0010	0	2:1	4
10	0010	0	2:1	8
11	0010	0	2:1	8
00	0010	1	2.5:1	2
01	0010	1	2.5:1	4
10	0010	1	2.5:1	8
11	0010	1	2.5:1	8
00	0011	0	3:1	2
01	0011	0	3:1	4
10	0011	0	3:1	8
11	0011	0	3:1	8

[1] Core VCO frequency = Core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

19.3   Suggested PLL Configurations

Table 63 shows suggested PLL configurations for 33 MHz and 66 MHz input clocks.

Table 63. Suggested PLL Configurations

Ref No.[1]	RCWL		400 MHz Device			533 MHz Device			667 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
33 MHz CLKIN/PCI_CLK Options											
922	1001	0100010	—	—	—	—	—	300	33	300	300
723	0111	0100011	33	233	350	33	233	350	33	233	350
604	0110	0000100	33	200	400	33	200	400	33	200	400
624	0110	0100100	33	200	400	33	200	400	33	200	400
803	1000	0000011	33	266	400	33	266	400	33	266	400
823	1000	0100011	33	266	400	33	266	400	33	266	400
903	1001	0000011		—			—		33	300	450
923	1001	0100011		—			—		33	300	450
704	0111	0000011		—		33	233	466	33	233	466
724	0111	0100011		—		33	233	466	33	233	466
804	1000	0000100		—		33	266	533	33	266	533
705	0111	0000101		—			—		33	233	583
606	0110	0000110		—			—		33	200	600
904	1001	0000100		—			—		33	300	600
805	1000	0000101		—			—		33	266	667
A04	1010	0000100		—			—		33	333	667
66 MHz CLKIN/PCI_CLK Options											
304	0011	0000100	66	200	400	66	200	400	66	200	400
324	0011	0100100	66	200	400	66	200	400	66	200	400
403	0100	0000011	66	266	400	66	266	400	66	266	400
423	0100	0100011	66	266	400	66	266	400	66	266	400
305	0011	0000101		—		66	200	500	66	200	500
404	0100	0000100		—		66	266	533	66	266	533
306	0011	0000100		—			—		66	200	600
405	0100	0000101		—			—		66	266	667
504	0101	0000100		—			—		66	333	667

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[1] The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

[2] The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

20 Thermal

This section describes the thermal specifications of the MPC8347EA.

20.1 Thermal Characteristics

Table 64 provides the package thermal characteristics for the 672 35 × 35 mm TBGA of the MPC8347EA.

Table 64. Package Thermal Characteristics for TBGA

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (@200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	8	•C/W	1, 3
Junction-to-ambient (@ 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	•C/W	1, 3
Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	•C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	3.8	•C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.7	•C/W	5
Junction-to-package natural convection on top	ψ_{JT}	1	•C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 65 provides the package thermal characteristics for the 620 29 × 29 mm PBGA of the MPC8347EA.

Table 65. Package Thermal Characteristics for PBGA

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient natural convection on four layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-ambient (@200 ft/min) on single layer board (1s)	$R_{\theta JMA}$	17	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on four layer board (2s2p)	$R_{\theta JMA}$	12	•C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	•C/W	4
Junction-to-case thermal	$R_{\theta JC}$	5	•C/W	5

Table 65. Package Thermal Characteristics for PBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	ψ_{JT}	5	•C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3. Per JEDEC JESD51-6 with the board horizontal.

4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

   T_J = junction temperature (°C)

   T_A = ambient temperature for the package (°C)

   $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

   P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity T_J - T_A) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For

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many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3   Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4　Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 66 and Table 67 show heat sink thermal resistance for TBGA and PBGA of the MPC8347EA.

Table 66. Heat Sink and Thermal Resistance of MPC8347EA (TBGA)

Heat Sink Assuming Thermal Grease	Air Flow	35 × 35 mm TBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	10
AAVID 30 × 30 × 9.4 mm Pin Fin	1 m/s	6.5
AAVID 30 × 30 × 9.4 mm Pin Fin	2 m/s	5.6
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	8.4
AAVID 31 × 35 × 23 mm Pin Fin	1 m/s	4.7
AAVID 31 × 35 × 23 mm Pin Fin	2 m/s	4
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	5.7
Wakefield, 53 × 53 × 25 mm Pin Fin	1 m/s	3.5
Wakefield, 53 × 53 × 25 mm Pin Fin	2 m/s	2.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural Convection	6.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	4.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.8
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm Side bypass	1 m/s	3.1

Table 67. Heat Sink and Thermal Resistance of MPC8347EA (PBGA)

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	13.5
AAVID 30 × 30 × 9.4 mm Pin Fin	1 m/s	9.6
AAVID 30 × 30 × 9.4 mm Pin Fin	2 m/s	8.8
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	11.3
AAVID 31 × 35 × 23 mm Pin Fin	1 m/s	8.1
AAVID 31 × 35 × 23 mm Pin Fin	2 m/s	7.5
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	9.1
Wakefield, 53 × 53 × 25 mm Pin Fin	1 m/s	7.1
Wakefield, 53 × 53 × 25 mm Pin Fin	2 m/s	6.5
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural Convection	10.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	7.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	6.6
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm Side bypass	1 m/s	6.9

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy   603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech   408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC)   818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI)   408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics   800-522-2800
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering   603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc.   781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation   800-248-2481
Dow-Corning Electronic Materials
P.O. Box 994
Midland, MI 48686-0997
Internet: www.dowcorning.com

Shin-Etsu MicroSi, Inc.   888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company   800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

20.3   Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force).   Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

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20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

P_D = power dissipation (W)

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8347EA.

21.1 System Clocking

The MPC8347EA includes two PLLs.

1. The platform PLL (AV$_{DD}$1) generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 19.1, "System PLL Configuration."

2. The e300 Core PLL (AV$_{DD}$2) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, "Core PLL Configuration."

21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins (AV$_{DD}$1, AV$_{DD}$2 respectively). The AV$_{DD}$ level should always equal to V$_{DD}$, and preferably these voltages are derived directly from V$_{DD}$ through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 41, one to each of the five AV$_{DD}$ pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific AV$_{DD}$ pin being supplied. It should be possible to route directly from the capacitors to the AV$_{DD}$ pin, which is on the periphery of package, without the inductance of vias.

Figure 41 shows the PLL power supply filter circuit.
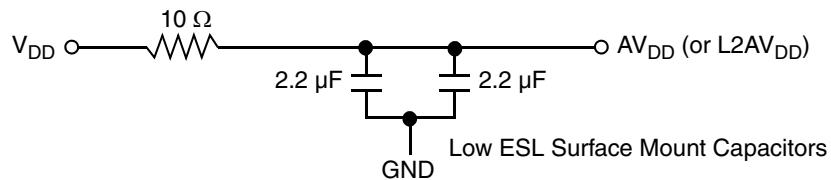
Figure 41. PLL Power Supply Filter Circuit

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8347EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8347EA system, and the MPC8347EA itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the MPC8347EA. These capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the MPC8347EA.

21.5 Output Buffer DC Impedance

The MPC8347EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^{2}C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 42). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.
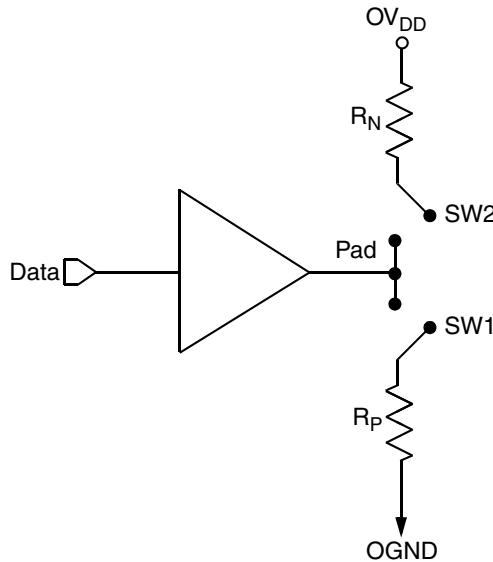
Figure 42. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 68 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 68. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (not including PCI output clocks)	PCI Output Clocks (including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

21.6 Configuration Pin Multiplexing

The MPC8347EA power-on configuration options can be set through external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see the customer-visible configuration pins). These pins are used as output only pins in normal operation.

However, while $\overline{\text{HRESET}}$ is asserted, these pins are treated as inputs, and the value on these pins is latched when $\overline{\text{PORESET}}$ deasserts. Then the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with

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the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7   Pull-Up Resistor Requirements

The MPC8347EA requires high resistance pull-up resistors (10 kΩ is recommended) on open-drain pins, including I^{2}C pins, the Ethernet Management MDIO pin, and EPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 43. Take care to ensure that these pins are maintained at a valid deasserted state under normal operating conditions because most have asynchronous behavior, and spurious assertion yields unpredictable results.

Refer to the PCI 2.3 specification for all pull-ups required for PCI.

21.8   JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std. 1149.1 specification, but it is provided on all processors that implement the PowerPC architecture. The MPC8347EA requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller may be forced to the reset state using only the TCK and TMS signals, systems typically assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical.

The PowerPC COP function allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to assert $\overline{\text{TRST}}$ independently without causing $\overline{\text{PORESET}}$. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 43 allows the COP to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ independently, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header are not used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$ so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted.

The COP header shown in Figure 43 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. It requires no more effort than adding an unpopulated footprint for a header when needed. The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). There is no standardized way to number the header, shown in Figure 43, so emulator vendors use different pin numbering schemes. Some headers are numbered top-to-bottom then left-to-right, others use left-to-right then top-to-bottom, and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 43 is common to all known emulators.

Figure 43. JTAG Interface Connection
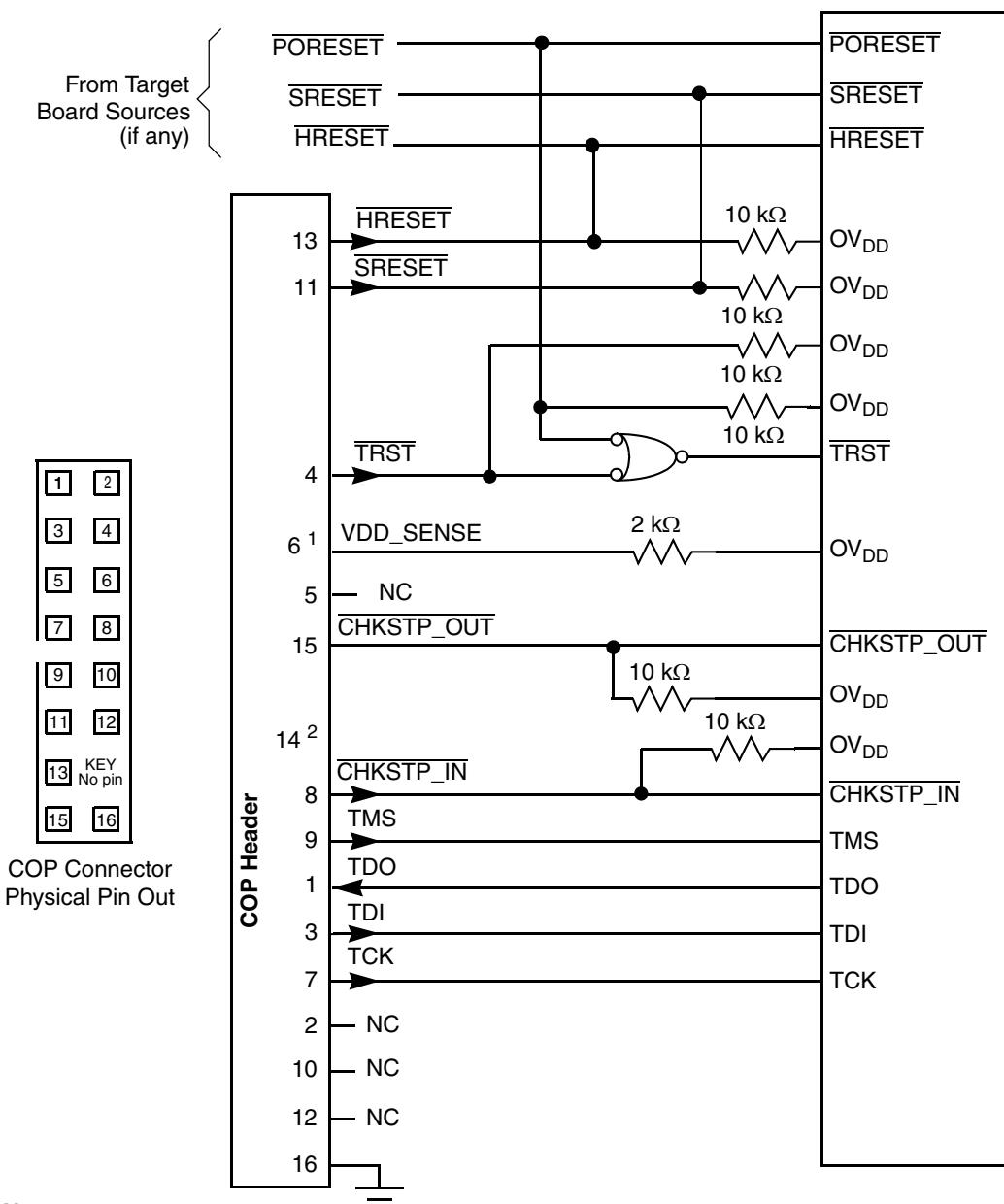
Notes:

1. Some systems require power to be fed from the application board into the debugger repeater card via the COP header. The resistor value for VDD_SENSE should be around 20Ω.

2. Key location; pin 14 is not physically present on the COP header.

22 Document Revision History

Table 66 provides a revision history of this document.

Table 69. Document Revision History

Revision	Date	Substantive Change(s)
3	11/2006	Updated note in introduction. In Table 5, "MPC8347EA Typical I/O Power Dissipation," added GVDD 1.8-V values for DDR2; added table footnote to designate rates that apply only to the TBGA package. In the features list in Section 1, "Overview," corrected DDR data rate to show: • 266 MHz for PBGA parts for all silicon revisions 400 MHz for DDR2 for TBGA parts for silicon Rev. 2 and 3In Section 23, "Ordering Information," replicated note from document introduction.
2	8/2006	Changed all references to revision 2.0 silicon to revision 3.0 silicon. Changed VIH minimum value in Table 39, "JTAG Interface DC Electrical Characteristics," to $OV_{DD} - 0.3$. In Table 63, "Suggested PLL Configurations," deleted reference-number rows 902 and 703. In Table 40, "PCI DC Electrical Characteristics," changed high-level input voltage values to min = 2 and max = OV_{DD} + 0.3; changed low-level input voltage values to min = (–0.3) and max = 0.8. In Table 44, "PCI DC Electrical Characteristics," changed high-level input voltage values to min = 2 and max = OV_{DD} + 0.3; changed low-level input voltage values to min = (–0.3) and max = 0.8. Updated DDR2 I/O power values in Table 5, "MPC8347EA Typical I/O Power Dissipation."
1	4/2006	Removed Table 20, "Timing Parameters for DDR2-400." Changed ADDR/CMD to ADDR/CMD/MODT in Table 9, "DDR and DDR2 SDRAM Output AC Timing Specifications," rows 2 and 3, and in Figure 2, "DDR SDRAM Output Timing Diagram. Changed Min and Max values for V_{IH} and VIL in Table 40,"PCI DC Electrical Characteristics." In Table 51, "MPC8347EA (TBGA) Pinout Listing," and Table 52, "MPC8347EA (PBGA) Pinout Listing," modified rows for MDICO and MDIC1 signals and added note "It is recommended that MDICO be tied to GRD using an 18 Ω resistor and MCIC1 be tied to DDR power using an 18 Ω resistor." In Table 51, "MPC8347EA (TBGA) Pinout Listing," and Table 52, "MPC8347EA (PBGA) Pinout Listing," in row AVDD3 changed power supply from "AVDD3" to "—."
0	3/2006	Initial Release

23 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked. The information in this document is accurate for revision 3.x silicon and later (in other words, for devices with part numbers ending in A or B, such as the MPC8347EA or MPC8347EB). For information on revision 1.1 silicon and earlier versions (*MPC8347E/MPC8347*), see the *PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications*

23.1 Part Numbers Fully Addressed by this Document

Table 67 shows an analysis of the Freescale part numbering nomenclature for the MPC8347EA. The individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Also the part numbering scheme includes an application modifier

to specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 70. Part Numbering Nomenclature

MPC	*nnnn*	*e*	*t*	*pp*	*aa*	*a*	*r*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature[1] Range**	**Package [2]**	**Processor Frequency [3]**	**Platform Frequency**	**Revision Level**
MPC	8347	Blank = Not included E = included	Blank = 0 to 105°C C= –40 to 105°C	ZU =TBGA VV = PB free TBGA ZQ = PBGA VR = PB Free PBGA	e300 core speed AD =266 AG = 400 AJ = 533 AL = 667	D = 266 F = 333	B = 3.1

Notes:

1. For temperature range = C, processor frequency is limited to 400 with a platform frequency of 266.

2. See Section 17, "Package and Pin Listings" for more information on available package types.

3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

Table 68 shows the SVR settings by device and package type.

Table 71. SVR Settings

Device	Package	SVR (Rev. 3.0)
MPC8347EA	TBGA	8052_0030
MPC8347A	TBGA	8053_0030
MPC8347EA	PBGA	8054_0030
MPC8347A	PBGA	8055_0030

23.2   Part Marking

Parts are marked as in the example shown in Figure 44.

MPCnnnnetppaaar

core/platform MHZ

ATWLYYWW

CCCCC

*MMMMM   YWWLAZ

TBGA/PBGA
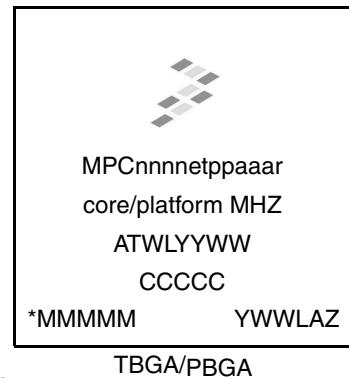
Notes:

ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 44. Freescale Part Marking for TBGA or PBGA Devices

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