

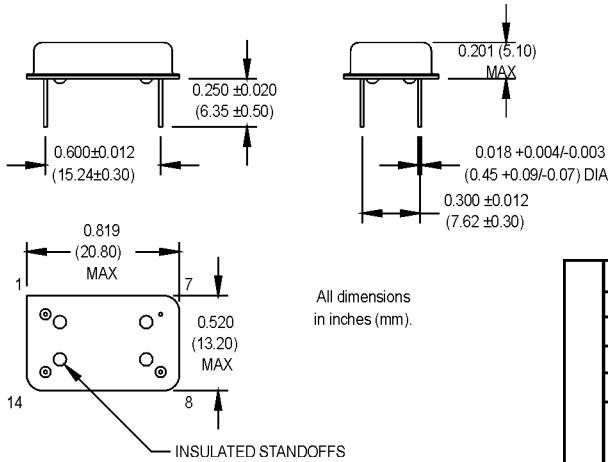
# MHO+ Series

## 14 pin DIP, 5.0 Volt, HCMOS/TTL, Clock Oscillator



### Features:

- Standard 14 DIP Package
- RoHS Compliant Version Available (-R)
- Tristate Option
- Wide Operating Temperature Range



### Pin Connections

PIN	FUNCTION
1	N/C or Tristate
7	Circuit/Case Ground
8	Output
14	+Vdd

### Available Symmetry

FREQUENCY RANGE	STD.	OPTIONS
0.732 kHz to 50 MHz	A	B, C, D
50.001 to 60 MHz	A	B, C
60.001 to 67 MHz	A	C
67.001 to 80 MHz	F,G	C

### Ordering Information

Product Series	MHO+	1	3	F	A	D	-R	00.0000	MHz
Temperature Range		1: 0°C to +70°C	2: -40°C to +85°C	3: -55°C to +105°C	4: -55°C to +125°C	5: -10°C to +85°C	6: -20°C to +70°C	7: 0°C to +85°C	
Stability		1: ±1000 ppm	2: ±500 ppm	3: ±100 ppm	4: ±50 ppm	5: ±35 ppm	6: ±25 ppm	7: +0/-200 ppm	*8: ±20 ppm
Output Type		F: Fixed	T: Tristate (1.000 to 80.000 MHz)						
Symmetry/Logic Compatibility (See Table Below)		A: 40/60 HCMOS/TTL	B: 45/55 TTL	C: 45/55 HCMOS	D: 45/55 HCMOS/TTL	F: 40/60 TTL	G: 40/60 HCMOS		
Package/Lead Configurations		D: DIP; Nickel Header					G: Gull Wing; Nickel Header		
RoHS Compliance		Blank: non-RoHS compliant part	-R: RoHS compliant part						
Frequency (customer specified)									

\*Contact factory for availability

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	.732 kHz		80	Mhz	See Note 1
Operating Temperature	T <sub>A</sub>	(See Ordering Information)				
Storage Temperature	T <sub>S</sub>	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				
Aging						
1st Year			±3		ppm	
Thereafter (per year)			±2		ppm	
Input Voltage	V <sub>dd</sub>	4.5	5.0	5.5	V	
Input Current	I <sub>dd</sub>			15	mA	.732 kHz to 2.999 MHz
				25	mA	3.000 to 25.999 MHz
				60	mA	26.000 to 80.000 MHz
Output Type						HCMOS/TTL
Load						See Note 2
				5 TTL or 50 pF		.732 kHz to 2.999 MHz
				10 TTL or 50 pF		3.000 to 67.000 MHz
				10 TTL or 15 pF		67.001 to 80.000 MHz
Symmetry (Duty Cycle)		(See Ordering Information)				
Logic "1" Level	V <sub>oh</sub>	90% V <sub>dd</sub>			V	HCMOS Load
		V <sub>dd</sub> -0.5			V	TTL Load
Logic "0" Level	V <sub>ol</sub>			10% V <sub>dd</sub>	V	HCMOS Load
				0.5	V	TTL Load
Output Current				±8	mA	0.732 kHz to 2.999 MHz
				±16	mA	3.000 to 80.000 MHz
Rise/Fall Time	T <sub>r</sub> /T <sub>f</sub>			20	ns	See Note 4
				10	ns	.732 kHz to 2.999 MHz
						3.000 to 80.000 MHz
Tristate Function		Input Logic "1" or floating; output active				
		Input Logic "0"; output to high-Z				
Start up Time			5		ms	
Random Jitter	R <sub>j</sub>		5	12	ps RMS	1-Sigma

1. Consult factory for availability of higher frequencies.
2. TTL load - See load circuit diagram #1. HCMOS load - See load circuit diagram #2.
3. Symmetry is measured at 1.4 V with TTL load, and at 50% V<sub>dd</sub> with HCMOS load.
4. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% V<sub>dd</sub> and 90% V<sub>dd</sub> with HCMOS load.

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