19-3705; Rev 0; 5/05

EVALUATION KIT AVAILABLE

Dual, Low-Voltage Linear Regulator Controllers with External MOSFETs

General Description

The MAX8737 dual high-power linear regulator controllers use external n-channel MOSFETs to generate two independent low-voltage supplies for notebook computers. The MAX8737 delivers low output voltages from 0.5V to 2.5V (±5mV no-load accuracy). The external components allow scalable current design with loads up to 5A with excellent load regulation (1%). The regulator operates from a low input voltage, which also reduces the power dissipation in the external n-channel MOSFET. The controller powers the external MOSFET gate driver from the standard 5V system supply.

The MAX8737 includes current and thermal limits to prevent damage to the linear regulator. The MAX8737 uses an external resistive divider to fold back the current limit, reducing the overall power dissipation. The MAX8737 uses an external resistive-divider in series with the current-sense input (CS_), providing foldback current-limit protection, and effectively reducing the short-circuit power dissipation.

An output undervoltage timeout is available for low-cost applications that omit the current-sense resistor. The output undervoltage (UVP) timing depends on the magnitude of the voltage at V_{OUT}. The UVP detects and shuts down the LDO if the output voltage drops out of regulation. The controller uses an adjustable reference input (REFIN_) to set the nominal output voltage ($V_{OUT\_}$), which minimizes the cost and makes the stability independent of the output voltage.

Each linear regulator features an adjustable soft-start function, and generates a delayed power-good (PGOOD) signal that signals when the linear regulator is in regulation. The MAX8737 is a low-cost solution requiring few external components and is available in a small, 4mm x 4mm, 16-pin thin QFN package.

Applications

Notebook and Desktop Computers

Point-of-Load Regulators

V_{MCH} and V_{CCP} CPU Supplies

Low-Voltage Bias Supplies

Servers

Features

- ♦ **Low-Cost Dual Linear Regulators**
- ♦ **Output Voltage Accuracy ±5mV**
- ♦ **Independent 0.5V to 2.5V Reference Inputs**
- ♦ **Foldback Current-Limit Protection**
- ♦ **Output Undervoltage-Lockout Protection**
- ♦ **Thermal Limit (Internal Sensor)**
- ♦ **1.0V to 5.5V Input Supply Voltage (External FET Drain)**
- ♦ **5V Bias Supply Voltage**
- ♦ **Independent Power-Good Open-Drain Outputs**
- ♦ **Independent Enable Inputs**
- ♦ **Soft-Shutdown Output Discharge**
- ♦ **Low Supply Current (0.5mA)**
- ♦ **5µA (max) Shutdown Supply Current**

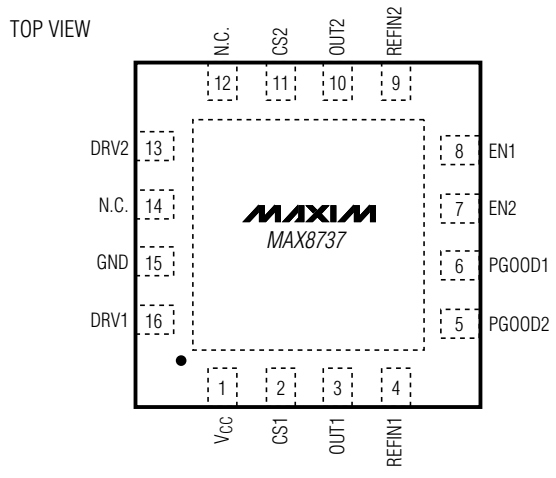
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8737ETE	-40°C to +85°C	16 Thin QFN-EP* 4mm x 4mm
MAX8737ETE+	-40°C to +85°C	16 Thin QFN-EP* 4mm x 4mm

**EP = Exposed pad.*

+Denotes lead-free packaging.

Pin Configuration



4mm x 4mm TQFN

Dual, Low-Voltage Linear Regulator Controllers with External MOSFETs

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
OUT1, OUT2 to GND .....-0.3V to +6V
REFIN1, REFIN2, PGOOD1, PGOOD2, EN1, EN2 to GND .....-0.3V to +6V
DRV1, DRV2, CS1, CS2 to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16-Pin 4mm x 4mm Thin QFN (derated 25mW/°C above +70°C) 2000mW
Operating Temperature Range
MAX8737ETE .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, EN_ = CS_ = V_{CC}, V_{REFIN} = 1.0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}		4.75		5.50	V
V_{CC} Undervoltage Lockout Threshold		Rising edge, 200mV hysteresis (typ)	4.1	4.35	4.6	V
V_{CC} Quiescent Supply Current	I_{CC}	EN1 = EN2 = V_{CC}		0.5	1	mA
V_{CC} Shutdown Supply Current		EN1 = EN2 = GND		0.1	5	µA
REFIN to OUT Offset Voltage	$V_{OUT\_}$		-5		+5	mV
OUT_ Input Bias Current	$I_{OUT\_}$		-1		+1	µA
DRIVERS						
DRV_ Output Voltage Swing (Note 1)		Output high; $V_{OUT\_}$ = $V_{REFIN\_}$ - 25mV, I_{LOAD} = 1mA	V_{CC} - 0.3	V_{CC} - 0.05		V
		Output low; $V_{OUT\_}$ = $V_{REFIN\_}$ + 25mV, I_{LOAD} = 1mA		0.03	0.3	
DRV_ Maximum Sourcing Current		$V_{OUT\_}$ = $V_{REFIN\_}$ - 25mV; V_{DRV} = 3V	6	14		mA
DRV_ Maximum Sinking Current		$V_{OUT\_}$ = $V_{REFIN\_}$ + 25mV; V_{DRV} = 3V	6	14		mA
OUT_ to DRV_ Transconductance (Large Signal)	G_{MDRV}			0.8		S
DRV_ Power-Supply Rejection Ratio		10Hz < f < 10kHz, I_{DRV} = 1mA, C_{DRV} = 10nF		-80		dB
DRV_ Soft-Start Charging Current	I_{SOFT}		40	170	400	µA
REFERENCE INPUT						
REFIN_ Voltage Range	$V_{REFIN\_}$	V_{CC} = 4.75V to 5.5V	0.5		2.5	V
REFIN_ Input Bias Current	$I_{REFIN\_}$	$V_{REFIN\_}$ = 0 to 2.5V	-100	-10	+100	nA
FAULT PROTECTION						
Thermal Shutdown Threshold	T_{SHDN}	Hysteresis = 20°C		+125		°C
Current-Limit Threshold	V_{ILIM}	$V_{CS\_}$ - $V_{OUT\_}$, T_A = 0°C to +85°C	7	10	13	mV
		$V_{CS\_}$ - $V_{OUT\_}$, T_A = +85°C	7.5	10	12.5	
CS_ Input Current			-1		+1	µA
Linear Regulator UVP Threshold (Slow)	$UVP_{(SLOW)}$	With respect to V_{REFIN}; CS_ = V_{CC}	72	80	88	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, EN_ = CS_ = V_{CC}, V_{REFIN} = 1.0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Linear Regulator UVP Threshold (Fast)	$UVP_{(FAST)}$	With respect to V_{REFIN}; CS_ = V_{CC}	54	60	66	%
Slow Short-Circuit Timer Duration	$t_{UVP(SLOW)}$	With respect to V_{REFIN}; CS_ = V_{CC}		75		µs
Fast Short-Circuit Timer Duration	$t_{UVP(FAST)}$	With respect to V_{REFIN}; CS_ = V_{CC}		5		µs
Discharge-Mode On-Resistance OUT_ Pin	R_{OUT}			10		Ω
INPUTS AND OUTPUTS						
EN_ Input Low Level					0.6	V
EN_ Input High Level		Rising edge, 200mV (typ) hysteresis	1.6			V
Enable Leakage Current			-1		+1	µA
Power-Good Trip Threshold (Lower)		With respect to error comparator threshold, hysteresis = 4% (falling edge)	-15	-12	-9	%
Power-Good Startup Delay				2		ms
Power-Good Propagation Delay	t_{PGOOD}	OUT_ forced 2% beyond PGOOD_ trip threshold		1		µs
Power-Good Output Low Voltage		I_{SINK} = 4mA			0.3	V
[illegible]	[illegible]	$V_{OUT\_}$ = 1.0V (PGOOD_ high impedance),		[illegible]		[illegible]

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, EN_ = CS_ = V_{CC}, V_{REFIN} = 1.0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}		4.75		5.50	V
V_{CC} Undervoltage Lockout Threshold		Rising edge 200mV hysteresis (typ)	4.1		4.6	V
V_{CC} Quiescent Supply Current	I_{CC}	EN1 = EN2 = V_{CC}			1.5	mA
V_{CC} Shutdown Supply Current		EN1 = EN2 = GND			5	µA
REFIN to OUT Offset Voltage	$V_{OUT\_}$		-7		+7	mV
DRIVERS						
DRV_ Output Voltage Swing (Note 1)		Output high; $V_{OUT\_}$ = $V_{REFIN\_}$ - 25mV; I_{LOAD} = 1mA	V_{CC} - 0.3			V
		Output low; $V_{OUT\_}$ = $V_{REFIN\_}$ + 25mV: I_{LOAD} = 1mA			0.3	
DRV_ Maximum Sourcing Current		$V_{OUT\_}$ = $V_{REFIN\_}$ - 25mV; V_{DRV} = 3V	3.5			mA
DRV_ Maximum Sinking Current		$V_{OUT\_}$ = $V_{REFIN\_}$ + 25mV; V_{DRV} = 3V	3.5			mA
DRV_ Soft-Start Charging Current	I_{SOFT}		40		400	µA

Dual, Low-Voltage Linear Regulator Controllers with External MOSFETs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, EN_ = CS_ = V_{CC}, V_{REFIN} = 1.0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

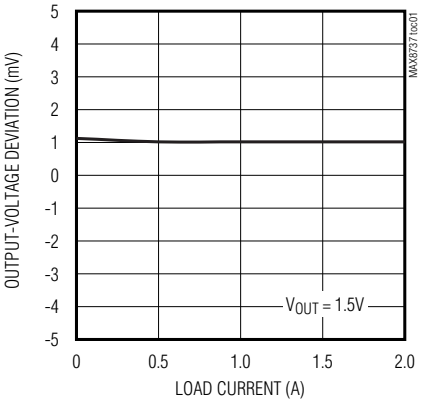
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT						
REFIN_ Voltage Range	$V_{REFIN\_}$	V_{CC} = 4.75V to 5.5V	0.5		2.5	V
FAULT PROTECTION						
Current-Limit Threshold	V_{ILIM}	$V_{CS\_}$ - $V_{OUT\_}$	6.5		13.5	mV
Linear Regulator UVP Threshold (Slow)	$UVP_{(SLOW)}$	With respect to V_{REFIN}; CS_ = V_{CC}	72		88	%
Linear Regulator UVP Threshold (Fast)	$UVP_{(FAST)}$	With respect to V_{REFIN}; CS_ = V_{CC}	54		66	%
INPUTS AND OUTPUTS						
EN_ Input Low Level					0.6	V
EN_ Input High Level			1.6			V
Power-Good Trip Threshold (Lower)		With respect to error comparator threshold, hysteresis = 4% (falling edge)	-15		-9	%
Power-Good Output Low Voltage		I_{SINK} = 4mA			0.3	V

Note 1: Low threshold n-channel MOSFET is required for 2.5V (±2%) output.
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

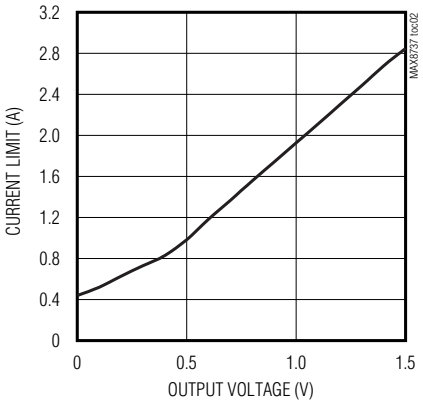
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

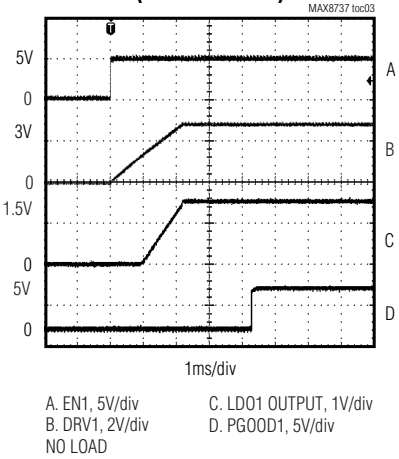
OUTPUT-VOLTAGE DEVIATION vs. LOAD CURRENT



FOLDBACK CURRENT LIMIT vs. OUTPUT VOLTAGE



SOFT-START (EN RISING EDGE)

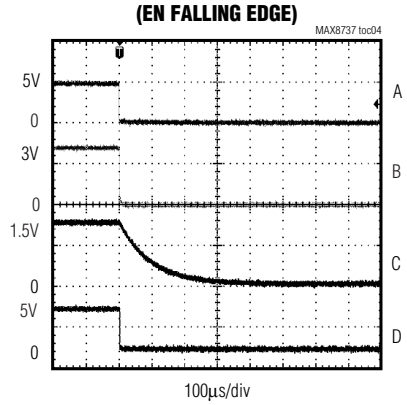


A. EN1, 5V/div
B. DRV1, 2V/div
NO LOAD
C. LDO1 OUTPUT, 1V/div
D. PGOOD1, 5V/div

Typical Operating Characteristics (continued)

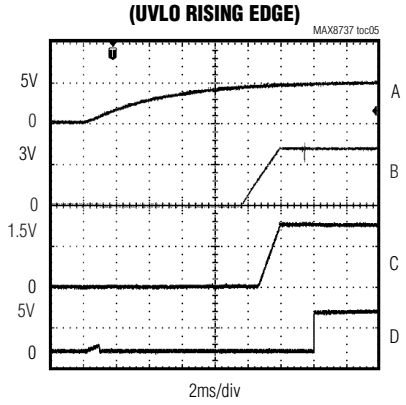
(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

SOFT-STOP (EN FALLING EDGE)



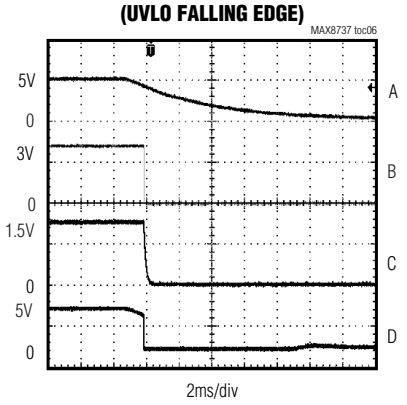
A. EN1, 5V/div
B. DRV1, 2V/div
NO LOAD
C. LDO1 OUTPUT, 1V/div
D. PGOOD1, 5V/div

SOFT-START (UVLO RISING EDGE)



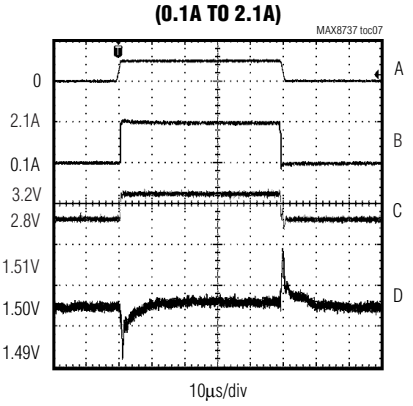
A. 5V BIAS (V_{CC}), 5V/div
B. DRV1, 2V/div
NO LOAD, EN = V_{CC}
C. LDO1 OUTPUT, 1V/div
D. PGOOD1, 5V/div

SOFT-STOP (UVLO FALLING EDGE)



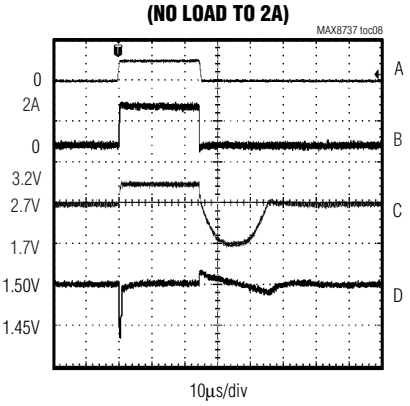
A. 5V BIAS (V_{CC}), 5V/div
B. DRV1, 2V/div
NO LOAD, EN = V_{CC}
C. LDO1 OUTPUT, 1V/div
D. PGOOD1, 5V/div

LOAD TRANSIENT (0.1A TO 2.1A)



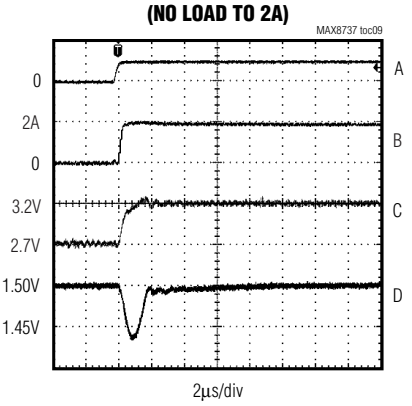
A. CONTROL SIGNAL
B. LOAD CURRENT, 2A/div
C. DRV1, 500mV/div
D. LDO1 OUTPUT VOLTAGE, 10mV/div

LOAD TRANSIENT (NO LOAD TO 2A)



A. CONTROL SIGNAL
B. LOAD CURRENT, 2A/div
C. DRV1, 1V/div
D. LDO1 OUTPUT VOLTAGE, 50mV/div

LOAD TRANSIENT (NO LOAD TO 2A)



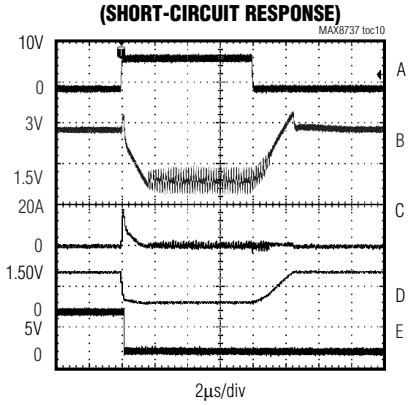
A. CONTROL SIGNAL
B. LOAD CURRENT, 2A/div
C. DRV1, 1V/div
D. LDO1 OUTPUT VOLTAGE, 50mV/div

Dual, Low-Voltage Linear Regulator Controllers with External MOSFETs

Typical Operating Characteristics (continued)

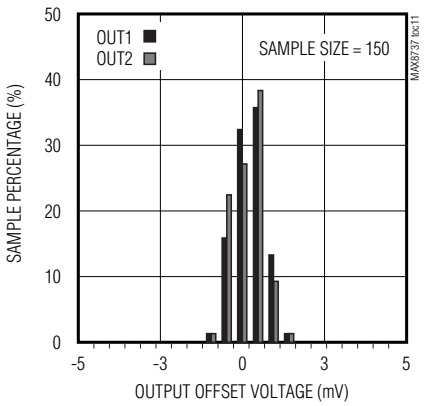
(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

FOLDBACK CURRENT LIMIT (SHORT-CIRCUIT RESPONSE)

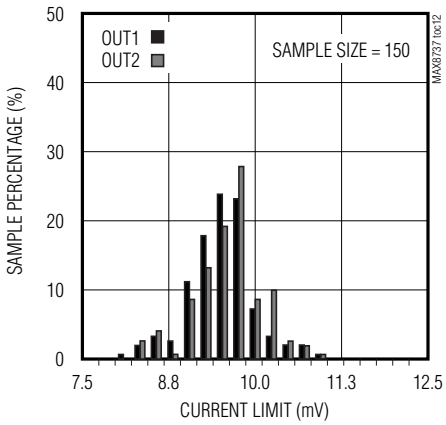


A. GATE OF FET LOAD, 10V/div
B. DRV1, 1V/div
C. MOSFET CURRENT, 20A/div
D. LD01 OUTPUT VOLTAGE, 2V/div
E. PGOOD1, 5V/div

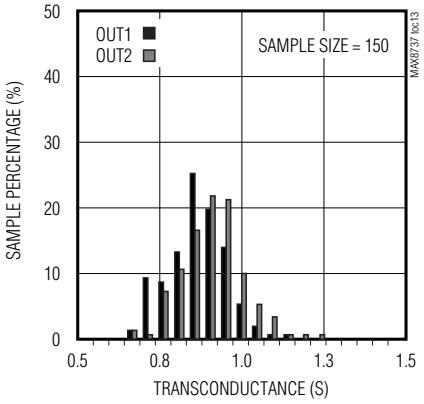
OUTPUT OFFSET VOLTAGE DISTRIBUTION



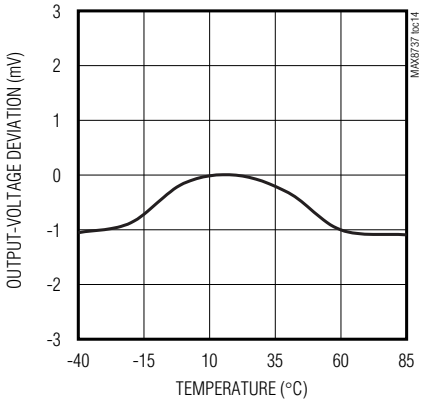
CURRENT-LIMIT THRESHOLD DISTRIBUTION



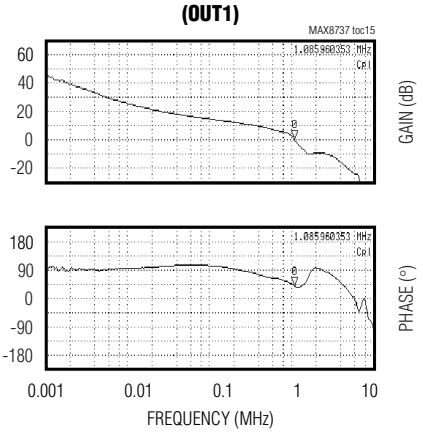
DRV TRANSCONDUCTANCE DISTRIBUTION



OUTPUT-VOLTAGE DEVIATION vs. TEMPERATURE

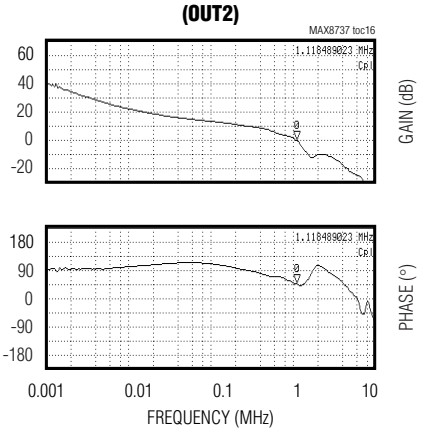


GAIN AND PHASE (OUT1)



1.5V OUTPUT, 1A LOAD, C_{OUT} = (1) 10µF 1206 16V CERAMIC

GAIN AND PHASE (OUT2)



1.05V OUTPUT, 2A LOAD, C_{OUT} = (1) 22µF 1206 6V CERAMIC

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Analog and Driver Supply Input. Connect to the system supply voltage (+5.0V). Bypass V_{CC} to analog ground with a 1µF or greater ceramic capacitor.
2	CS1	Positive Current-Sense Input for LDO1. To enable (foldback) current limit, connect CS1 to the positive terminal of the current-sense element as shown in Figure 1. The MAX8737 driver reduces the gate voltage when the 10mV (typ) current-limit threshold is exceeded. When CS1 is connected to V_{CC}, the MAX8737 disables the current-limit protection and enables the output undervoltage protection (see the *UVP Short-Circuit Protection* section).
3	OUT1	Output Feedback-Sense, Negative Current-Sense, and Discharge Input for LDO1. Connect directly to the linear regulator output. When LDO1 is disabled, OUT1 is discharged through an internal 10Ω FET to GND.
4	REFIN1	External Reference Input for LDO1. REFIN1 sets the main output regulation voltage ($V_{OUT1} = V_{REFIN1}$).
5	PGOOD2	Open-Drain Power-Good Output for LDO2. PGOOD2 is low when the output voltage is more than 12% (typ) below the normal regulation point, during soft-start, and in shutdown. Approximately 2ms (typ) after OUT2 reaches the regulation voltage (REFIN2), PGOOD2 becomes high impedance as long as the output remains in regulation.
6	PGOOD1	Open-Drain Power-Good Output for LDO1. PGOOD1 is low when the output voltage is more than 12% (typ) below the normal regulation point, during soft-start, and in shutdown. Approximately 2ms (typ) after OUT1 reaches the regulation voltage (REFIN1), PGOOD1 becomes high impedance as long as the output remains in regulation.
7	EN2	Enable Input for LDO2. Connect EN2 to Vcc for always ON. When EN2 is pulled low, the linear regulator shuts down and pulls the output to ground.
8	EN1	Enable Input for LDO1. Connect EN1 to Vcc for always ON. When EN1 is pulled low, the linear regulator shuts down and pulls the output to ground.
9	REFIN2	External Reference Input for the Secondary Regulator (LDO2). REFIN2 sets the main output regulation voltage ($V_{OUT2} = V_{REFIN2}$).
10	OUT2	Output Sense, Negative Current-Sense Input, and Discharge Input for the Secondary Regulator (LDO2). Connect directly to the linear regulator output. When the LDO2 is disabled, OUT2 is discharged through an internal 10Ω FET to GND.
11	CS2	Positive Current-Sense Input for LDO2. To enable (foldback) current limit, connect CS2 to the positive terminal of the current-sense element as shown in Figure 1. The MAX8737 driver reduces the gate voltage when the 10mV (typ) current-limit threshold is exceeded. When CS2 is connected to V_{CC}, the MAX8737 disables the current-limit protection and enables the output undervoltage protection (see the *UVP Short-Circuit Protection* section).
12, 14	N.C.	Not Internally Connected
13	DRV2	External N-Channel Gate Drive for LDO2
15	GND	Ground. **Connect the thin QFN backside pad to GND.**
16	DRV1	External N-Channel Gate Drive for LDO1
—	EP	Exposed Pad. Connect the thin QFN backside pad to GND.

Dual, Low-Voltage Linear Regulator Controllers with External MOSFETs

Detailed Description

The MAX8737 is a dual, low-dropout, external n-channel linear regulator controller for low-voltage notebook computer power supplies. The linear regulator provides a 0.5V to 2.5V (±5mV no-load) output for powering the low-voltage supplies to desktop and notebook CPU chipsets (V_{CCP} and V_{CC_MCH}). The regulator operates from low input voltage, which also reduces the power dissipation in the external n-channel MOSFET. The controller powers the external MOSFET gate driver from the standard 5V system supply.

The controller features independent enable inputs (EN_), PGOOD outputs (PGOOD_), input undervoltage lockout (UVLO), and output undervoltage protection (UVP). The controller uses an adjustable reference input (REFIN_) to set the nominal output voltage (V_{OUT}), which minimizes the cost and makes the stability independent of the output voltage. An output UVP timing depends on the magnitude of the voltage at V_{OUT}. The UVP detects and shuts down the LDO if the output voltage drops below the nominal output voltage (V_{REFIN}). Each linear regulator features an adjustable soft-start function, and generates a delayed PGOOD signal that signals when the linear regulator is in regulation. The MAX8737 uses an external resistor-divider in series with the current-sense input (CS_), providing foldback current-limit protection, and effectively reducing the short-circuit power dissipation. The MAX8737 is available in a thin QFN package to reduce the thermal impedance, and improve the thermal coupling between the controller and the external MOSFETs.

REFIN Input

The low-cost linear regulator uses an adjustable reference input (REFIN_) to set the nominal output voltage, which minimizes cost and simplifies the stability—the stability calculation is independent of V_{OUT}. The output voltage accuracy depends on the accuracy of the source generating the REFIN voltage. Multiple accurate references are typically available elsewhere in the system (such as the switching regulator providing the low-voltage input supply). If lower output accuracy is acceptable, divide down and filter another regulated output voltage supply.

To set output voltage, select R2 = 100kΩ and select R1 using the following formula:

$$R1 = \left(\frac{V_{REF}}{V_{REFIN\_}} - 1 \right) R2$$

Soft-Start

When the LDO is activated, the respective DRV_ is pulled up from GND with a typical soft-start current of 170µA. The soft-start current limits the output voltage slew rate and also limits the initial current spike through the external n-channel MOSFET. The slew rate is also limited by the compensation capacitance used at the DRV_ pin.

The maximum drain current during startup is the ratio of C_{OUT} to C_{COMP}, multiplied by the soft-start current I_{SOFT} of 170µA (typ).

Enable and Power Good

The MAX8737 has independent enable control inputs (EN1, EN2). Drive EN1 high to enable output 1. Drive EN2 high to enable output 2. When EN_ is driven low, the corresponding DRV_ and PGOOD_ pins are pulled to GND, and the output is discharged through a 10Ω switch.

There are two independent PGOOD_ outputs indicating the supply status. PGOOD_ is pulled high 2ms after the controller is enabled (EN_ is pulled high and V_{CC} exceeds its UVLO threshold), and the output is in regulation. If either output is out of regulation, the respective PGOOD_ goes low immediately. The MAX8737 pulls PGOOD_ low if the output voltage drops below the lower trip threshold of -12% (typ) or when V_{CC} is in UVLO or when EN_ is pulled low.

Soft-Stop

The MAX8737 enables a soft-stop function that discharges the output through an internal 10Ω switch when EN_ is driven low or V_{CC} is in UVLO. The discharge time of the output depends on the output capacitance, output load, and the exact resistance of the internal discharge switch. To slow down the discharge rate, add resistance in series with the OUT_ pin.

5.0V Bias Supply (Vcc)

The linear regulator operates with very low input voltages. V_{IN} may be as low as 1.2V, so a secondary 5V supply is required to provide sufficient bias to the gate drivers. Locally decouple the V_{CC} input with 1µF or greater of ceramic capacitance.

Current Limit

The MAX8737 features a current limit that monitors the voltage across the current-sense resistor, which limits $V_{CS\_}$ - $V_{OUT\_}$ to 10mV (typ). However, in case of a short-circuit condition, the power dissipation across the external FET will be extremely high. To protect the external FET, the MAX8737 uses an external resistive divider (see Figure 1) to fold back the current limit, reducing the overall power dissipation. The foldback

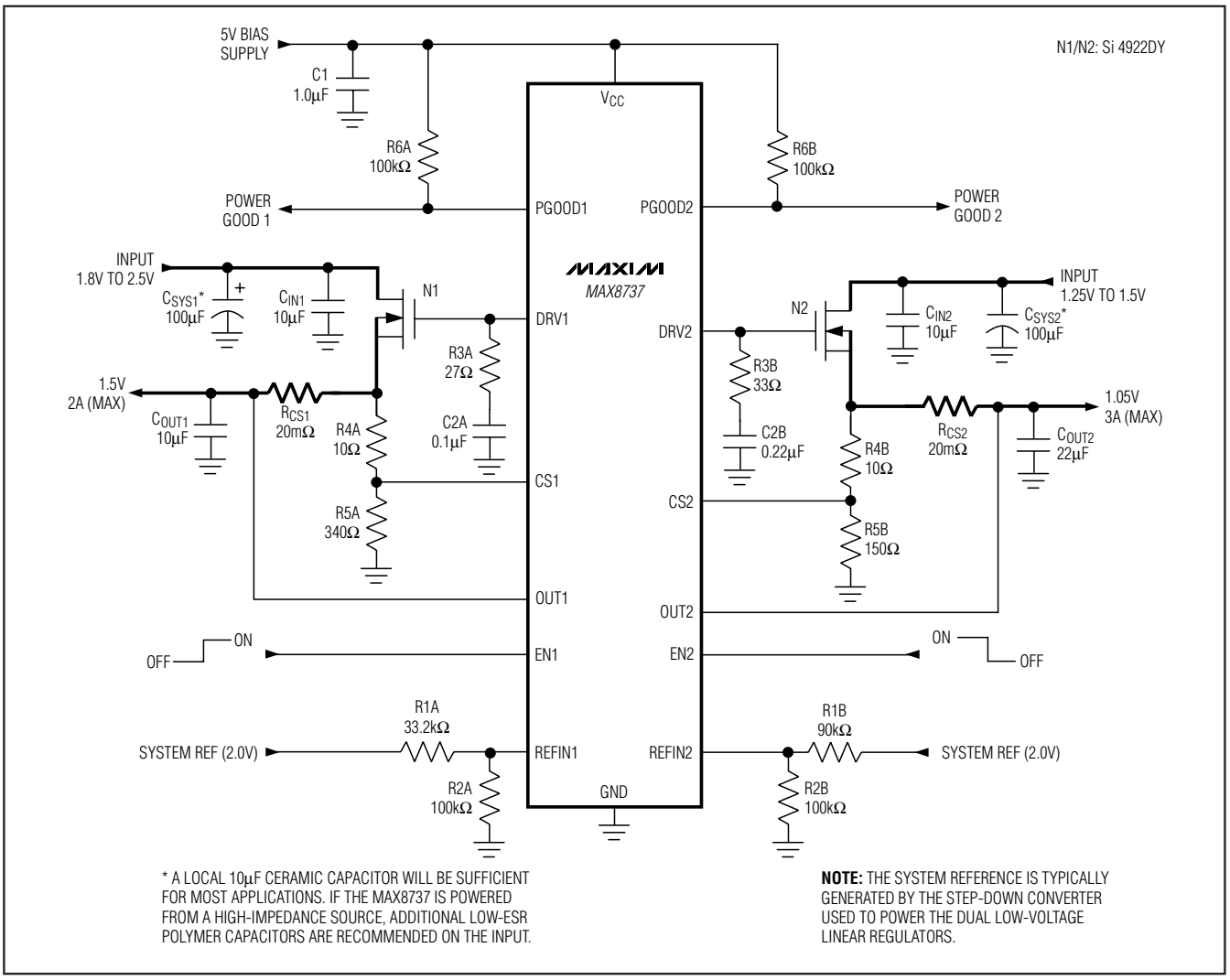


Figure 1. Typical Operating Circuit with Current Limit

resistor network is calculated using the short-circuit current (I_{SHORT}), the maximum load current (I_{MAX}), current-sense resistor (R_{CS}), the 10mV (±3mV) current-limit threshold (V_{ILIM}), and the external reference input (REFIN_). See Figure 3:

1) Pick the R_{CS} requirement for maximum short-circuit current:

$$R_{CS} = V_{ILIM} / I_{SHORT}$$

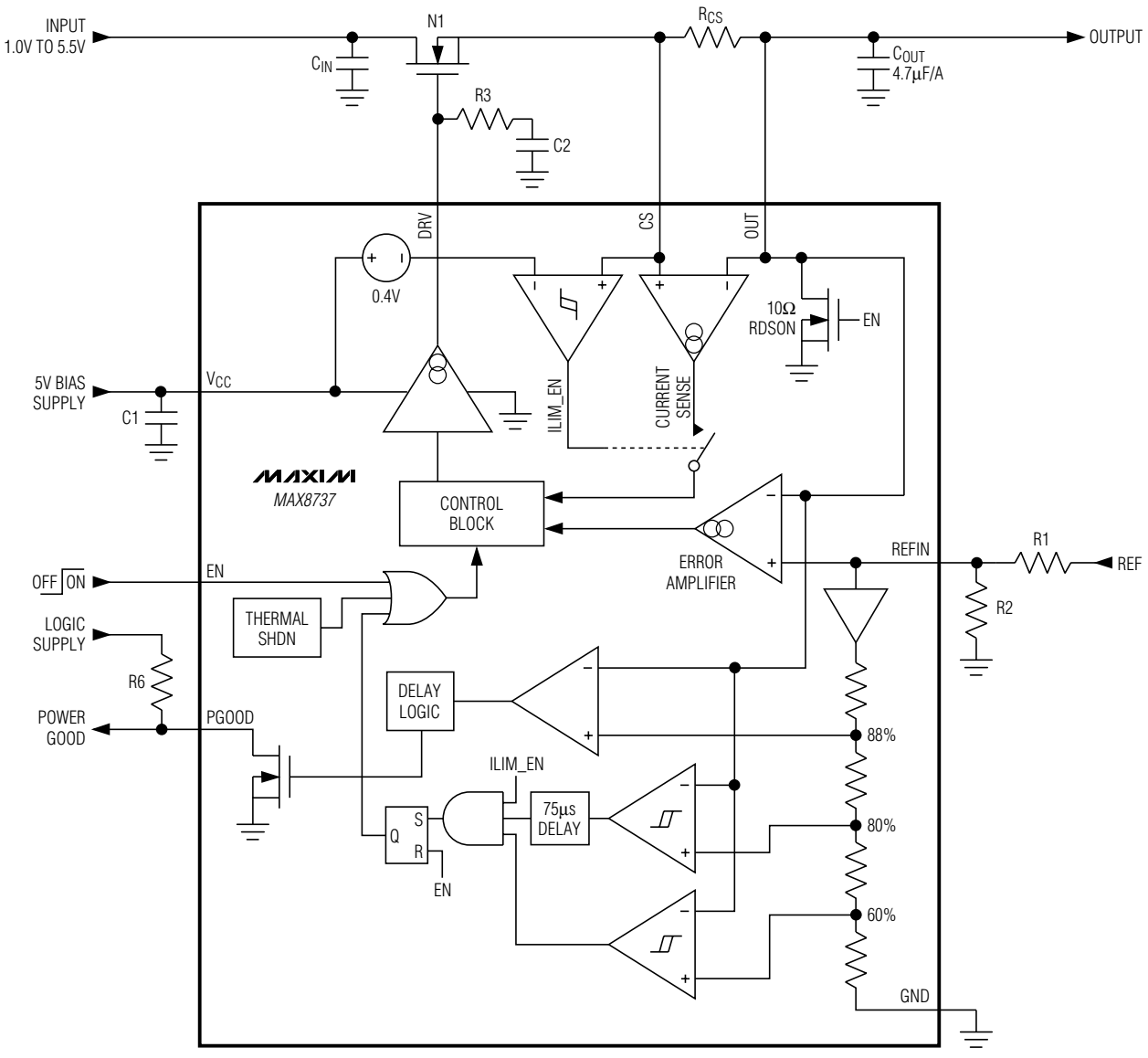
2) Select R1 = 10Ω and select R2 using the following formula:

$$R2 = \frac{(V_{REFIN} + V_{ILIM})R1}{I_{MAX}R_{CS} - V_{ILIM}}$$

UVP Short-Circuit Protection

There are two levels of short-circuit UVP available in the controller. When the current-limit protection is not used (CS_= V_{CC}), the output undervoltage timeout protection is enabled, which protects the regulator against short circuits. Output UVP timing depends on the magnitude of the output voltage drop. To clear the UVP fault latch, toggle the respective EN_ input, or cycle V_{CC} below its UVLO threshold.

Dual, Low-Voltage Linear Regulator Controllers with External MOSFETs



THE MAX8737 INCLUDES TWO LDOs AS SHOWN ABOVE.

Figure 2. Functional Diagram

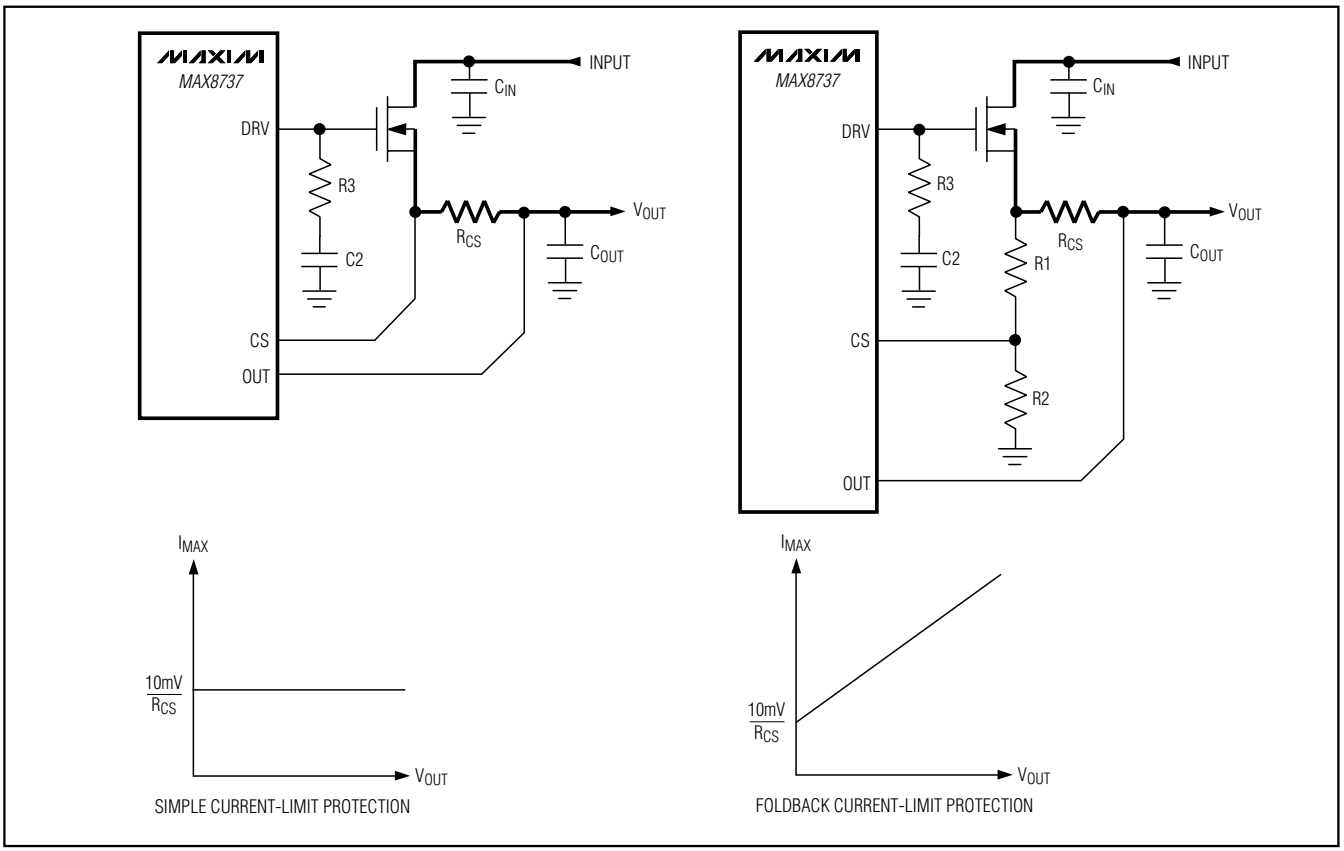


Figure 3. Current-Limit Protection

Slow UVP

If the output drops below 80% of the nominal output voltage (V_{REFIN}) for 75µs, the MAX8737 shuts down the LDO and pulls the DRV_ pin to ground. If the output voltage returns above 80% of the nominal output voltage (V_{REFIN}) within the 75µs, the controller ignores the load transient.

Fast UVP

If the output voltage drops below 60% of the nominal output voltage (V_{REFIN}) for approximately 5µs, the MAX8737 immediately shuts down and pulls the DRV_ pin to ground. If the output voltage returns above 80% of the nominal output voltage (V_{REFIN}) within the 5µs, the controller ignores the load transient.

Thermal Protection

The MAX8737 is available in a thin QFN package to reduce the thermal impedance, and improve the thermal coupling between the controller and the external MOSFETs. When the controller's junction temperature exceeds T_J = +125°C (max), a thermal sensor turns off the external pass transistor, allowing the system to cool. The thermal sensor turns the pass transistor back on once the controller's junction temperature drops by approximately 20°C.

Design Procedure

Input Capacitor Selection (C_{IN})

Typically, the MAX8737 is powered from the output of a step-down regulator, effectively providing a low-impedance source. A local 10µF ceramic capacitor at V_{IN} and a 1.0µF ceramic capacitor at V_{BIAS} should be sufficient for most applications. If the linear regulator is connected to a high-impedance input, low-ESR polymer capacitors are recommended on the input.

Output Capacitor Selection (C_{OUT})

To maintain stability and provide good transient response, the MAX8737 requires 4.7µF/A (4.7µF minimum) of low ESR ceramic capacitor at the output. The regulator remains stable with capacitances higher than the minimum. When selecting the output capacitor to

Dual, Low-Voltage Linear Regulator Controllers with External MOSFETs

provide good transient response, the capacitor's ESR should be minimized:

$$\Delta V_{OUT} = \Delta I_{OUT} \times ESR$$

where ΔI_{OUT} is the maximum peak-to-peak load current step, and ΔV_{OUT} is the transient output-voltage tolerance.

Regulator Compensation

The compensation network (R3_, C2_) is customizable and depends on load and MOSFET characteristics:

- Use of ceramic output capacitors with low R_{ESR} to ensure stability and minimize ESR voltage drop at load step
- Strength of the external n-channel MOSFET (g_M), its forward transconductance (g_{FS}), and the gate-to-source capacitance (C_{GS})
- The driver transconductance (G_{MDRV}) of the integrated circuit driver
- Load current range (including the minimum load): I_{MIN} to I_{MAX}

Recommended Procedure

Use the C_{GS}, g_{FS}, I_D from the chosen transistor data sheet and use the equation below to translate the measured g_{FS} to g_M for normal operation:

1) Determine the LDO transconductance using the MOSFET's forward transconductance (g_{FS}), and the drain current (I_D) used to test the selected MOSFET:

$$g_M = g_{FS}\sqrt{\frac{I_{MAX}}{I_D}}$$

2) Calculate the compensation resistor based on the output capacitor (C_{OUT}), the MOSFET's gate-to-source capacitance ($C_{GS} = C_{ISS} - C_{RSS}$), and the minimum driver transconductance:

$$R3 = \sqrt{\frac{C_{OUT}}{C_{GS} g_M \times 0.5S}}$$

3) Calculate the compensation capacitance using the minimum load current (I_{MIN}) and compensation resistor value calculated above:

$$C2 = \frac{2V_T C_{OUT}}{I_{MIN} G_{MDRV} (R3)^2}$$

where V_T = 25mV.

Example: The example below is used to demonstrate the stability calculation for the application circuit in Figure 1.

1) Choose V_{OUT} = 1.05V and I_{MAX} = 3A and the minimum load can be determined from the foldback current-limit resistance:

$$I_{MIN} = \frac{V_{OUT}}{R1 + R2} \approx 6mA$$

2) For the selected MOSFET (Si4922DY), C_{GS} = 2000pF at 1.5V, and g_{FS} = 30S at I_D = 8.8A:

$$g_M = 30S\sqrt{\frac{3A}{8.8A}} = 17.5S$$

3) The output capacitor must be at least 4.7µF/A. Therefore the design must use a minimum 14.1µF capacitor. The closest standard capacitor value is 22µF.

4) Based on the above operating conditions and component selection, the compensation resistor value should be:

$$R3 = \sqrt{\frac{22\mu F}{2nF \times 17.5S \times 0.5S}} = 35\Omega$$

5) Finally, select the compensation capacitor value:

$$C2 = \frac{2 \times 25mV \times 22\mu F}{6mA \times 1S \times (35\Omega)^2} = 0.15\mu F$$

External MOSFET Selection

The MAX8737 uses an n-channel MOSFET as the series pass transistor instead of a p-channel MOSFET to reduce cost. The selected MOSFET must have a gate threshold voltage (at the required max load) that meets the following criteria:

$$V_{GS\_MAX} \le V_{CC} - V_{OUT}$$

where V_{CC} is the controller bias voltage, and V_{GS_MAX} is the maximum gate voltage required to yield the on-resistance (R_{DS_ON}) specified by the manufacturer's data sheet. Make sure that input-to-output voltage meets the condition below to avoid entering dropout, where output voltage starts to decrease and any ripple on the input also passes through to the output. R_{DSON} has a positive temperature coefficient (approximately

0.5%/°C); therefore, the value of R_{DSON} at the highest operating junction temperature should be used:

$$V_{IN\_MIN} - V_{OUT\_MAX} \geq I_{MAX}(R_{DSON\_MAX} + R_{CS})$$

where V_{IN_MIN} is the minimum input voltage at the drain of the MOSFET.

MOSFET Power Dissipation

The maximum power dissipation of the MAX8737 depends on the thermal resistance of the external n-channel MOSFET package, the board layout, the temperature difference between the die and ambient air, and the rate of airflow. The power dissipated in the MOSFET is:

$$P_{DIS} = I_{OUT}(V_{IN} - V_{CSP})$$

The maximum allowable power dissipation is determined by the following formula:

$$R_{DIS(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature (+150°C), T_A is the ambient temperature, θ_{JC} is the thermal resistance from the die junction to the package case, and θ_{CA} is the thermal resistance from the case through the PC board, copper traces, and other materials to the surrounding air. Standard 8-pin SO MOSFETs are typically rated for 2W, while new power packages (PowerPAK™, DirectFET™, etc.) can achieve power dissipation ratings as high as 5W. For optimum power dissipation, use a large ground plane with good thermal contact to ground and use wide input and output traces. Extra copper on the PC board increases thermal mass and reduces the thermal resistance of the board. See Figure 4.

PC Board Layout Guidelines

Due to the high-current paths and tight output accuracy required by most applications, careful PC board layout is required. An evaluation kit (MAX8737EVKIT) is available to speed design. I**t is important to keep all traces as short as possible to minimize the high-current trace dimensions to reduce the effect of undesirable parasitic inductance.** The MOSFET dissipates a fair amount of heat due to the high currents involved, especially during large input-to-output voltage differences. To dissipate the heat generated by the MOSFET, make power traces very wide with a large amount of copper area. An efficient way to achieve good power dissipation on a surface-mount package is to lay out copper areas directly under the MOSFET package on multiple layers and connect the areas through vias. Use a ground plane to minimize impedance and inductance.

In addition to the usual high-power considerations, here are four tips to ensure high output accuracy:

- Ensure that the feedback connection to C_{OUT} is short and direct.
- Place the reference input resistors next to the REFIN_ pin.
- Place RC and CC next to the DRV_ pin.
- Ensure REFIN_ and DRV_ traces are away from noisy sources to ensure tight accuracy.

PowerPAK is a registered trademark of Vishay Siliconix.

DirectFET is a trademark of International Rectifier Corp.

Dual, Low-Voltage Linear Regulator Controllers with External MOSFETs

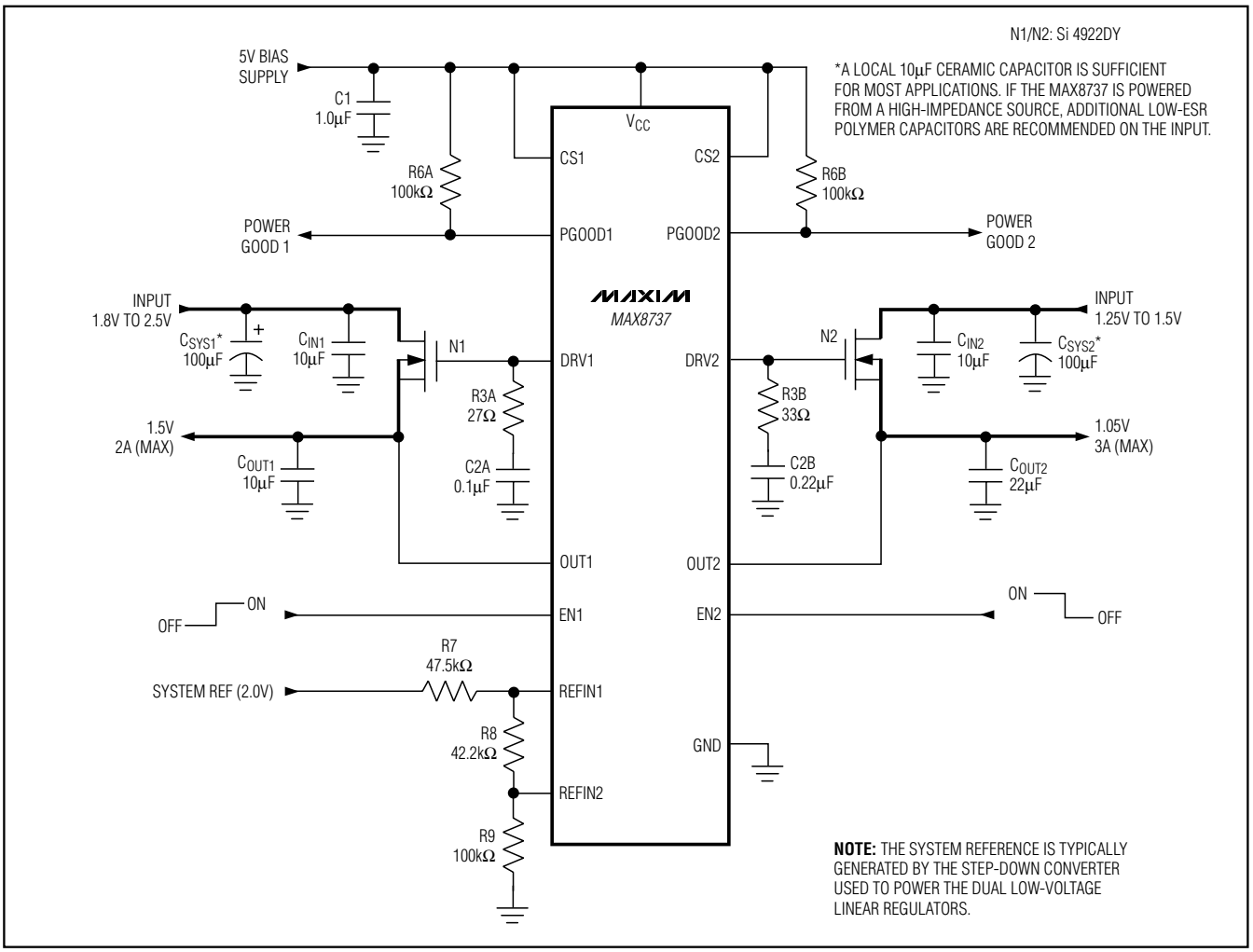


Figure 4. Typical Operating Circuit with Output Undervoltage Protection

Chip Information

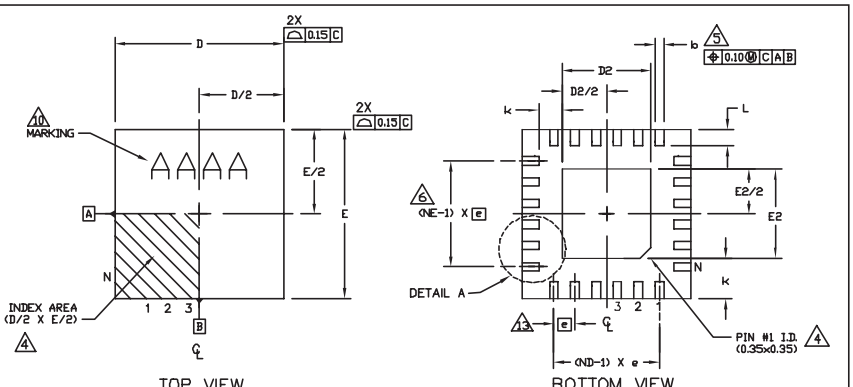
TRANSISTOR COUNT: 1562

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV. D
2/2