FAIRCHILD SEMICONDUCTOR®

December 2006

FPF1003-FPF1004
IntelliMAX™ Advanced Load Management Products

Features

- 1.2 to 5.5V Input Voltage Range
- $R_{DS(ON)}$ = 30 mΩ @ V_{IN} = 5.5V
- $R_{DS(ON)}$ = 35 mΩ @ V_{IN} = 3.3V
- ESD Protected, above 2000V HBM

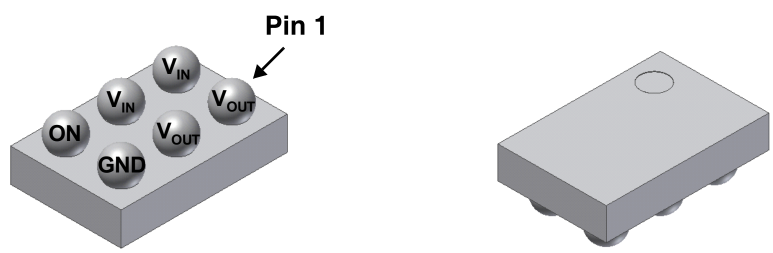
Applications

- PDAs
- Cell Phones
- GPS Devices
- MP3 Players
- Digital Cameras
- Peripheral Ports
- Hot Swap Supplies
- RoHS Compliant

General Description

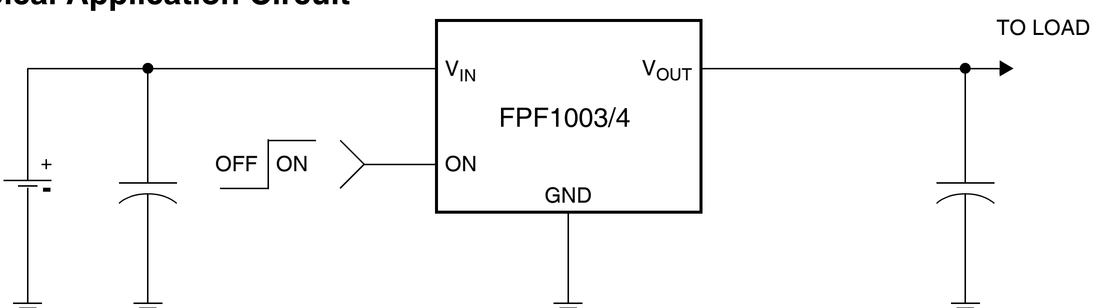
The FPF1003 & FPF1004 are low RDS P-Channel MOSFET load switches with controlled turn-on. The input voltage range operates from 1.2V to 5.5V to fulfill today's Ultra Portable Device's supply requirement. Switch control is by a logic input (ON) capable of interfacing directly with low voltage control signal. In FPF1004, 120Ω on-chip load resistor is added for output quick discharge when switch is turned off.

Both FPF1003 & FPF1004 are available in a space-saving 1.0x1.5 mm^2 chip scale package, 1.0X1.5CSP-6.



BOTTOM TOP

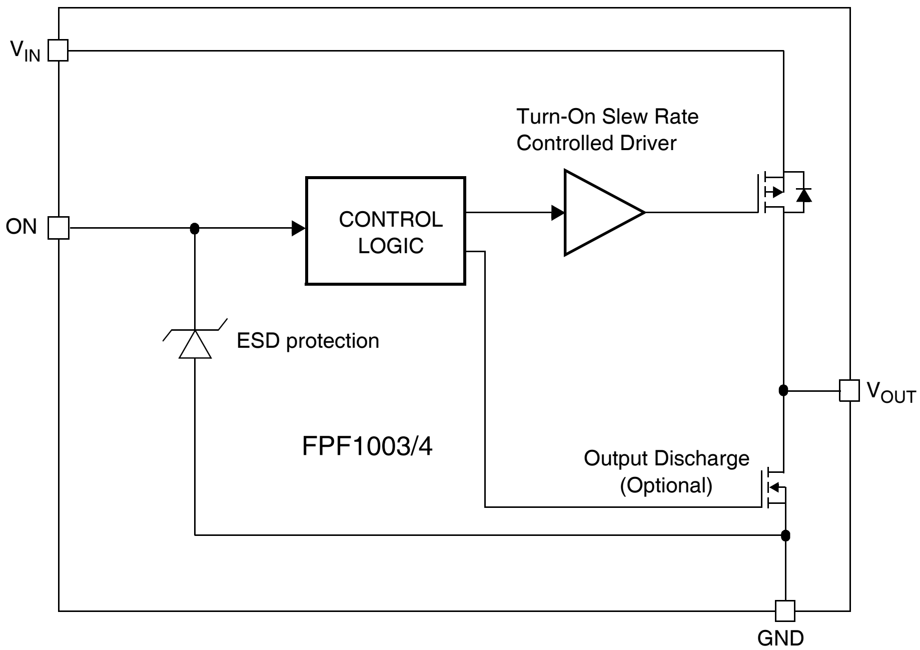
Typical Application Circuit



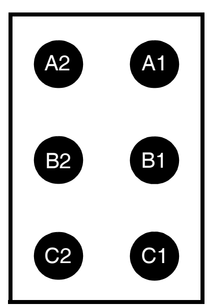
Ordering Information

Part	Switch	Input buffer	Output Discharge	ON Pin Activity	Top Mark
FPF1003	30mΩ, PMOS	Schmitt	NA	Active HI	3
FPF1004	30mΩ, PMOS	Schmitt	120Ω	Active HI	4

Functional Block Diagram



Pin Configuration



1.0 x 1.5 CSP Bottom View

Pin Description

Pin	Name	Function
A2, B2	V_{IN}	Supply Input: Input to the power switch and the supply voltage for the IC
C2	ON	ON Control Input
A1, B1	V_{OUT}	Switch Output: Output of the power switch
C1	GND	Ground

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{IN}, V_{OUT}, ON to GND		-0.3	6	V
Power Dissipation @ T_A = 25°C (Note 1)			1.2	W
Maximum Continuous Switch Current			2.0	A
Operating Temperature Range		-40	125	°C
Storage Temperature		-65	150	°C
Thermal Resistance, Junction to Ambient			85	°C/W
Electrostatic Discharge Protection	HBM	2000		V
	MM	200		V

Recommended Operating Range

Parameter	Min	Max	Unit
V_{IN}	1.2	5.5	V
Ambient Operating Temperature, T_A	-40	85	°C

Electrical Characteristics

V_{IN} = 1.2 to 5.5V, T_A = -40 to +85°C unless otherwise noted. Typical values are at V_{IN} = 3.3V and T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Basic Operation						
Operating Voltage	V_{IN}		1.2		5.5	V
Quiescent Current	I_Q	I_{OUT} = 0mA, V_{IN} = Von			1	µA
Off Supply Current	$I_{Q(off)}$	Von = GND, OUT = open			1	µA
Off Switch Current	$I_{SD(off)}$	Von = GND, V_{OUT}= 0			1	µA
On-Resistance	R_{ON}	V_{IN} = 5.5V, T_A = 25°C		20	30	mΩ
		V_{IN} = 3.3V, T_A = 25°C		25	35	
		V_{IN} = 1.5V, T_A = 25°C		50	75	
		V_{IN} = 1.2V, T_A = 25°C		95	150	
Output Pull Down Resistance	R_{PD}	V_{IN} = 3.3V, V_{ON} = 0V, T_A = 25°C, FPF1004		75	120	Ω
ON Input Logic High Voltage	V_{IH}	V_{IN} = 2.7V to 5.5V	2			V
		V_{IN} = 1.2V	0.8			
ON Input Logic Low Voltage	V_{IL}	V_{IN} = 2.7V to 5.5V			0.8	V
		V_{IN} = 1.2V			0.35	
ON Input Leakage		V_{ON} = V_{IN} or GND			1	µA
Dynamic						
Turn on delay	t_{ON}	V_{IN} = 3.3V, R_L=500Ω, C_L=0.1uF, T_A = 25°C		13		µs
Turn off delay	t_{OFF}	V_{IN} = 3.3V, R_L=500Ω, C_L=0.1uF, T_A = 25°C, FPF1003		45		µs
		V_{IN} = 3.3V, R_L=500Ω, C_L=0.1uF, R_{L_CHIP}=120Ω, T_A = 25°C, FPF1004		15		µs
V_{OUT} Rise Time	t_R	V_{IN} = 3.3V, R_L=500Ω, C_L=0.1uF, T_A = 25°C		13		µs
V_{OUT} Fall Time	t_F	V_{IN} = 3.3V, R_L=500Ω, C_L=0.1uF, T_A = 25°C, FPF1003		113		µs
		V_{IN} = 3.3V, R_L=500Ω, C_L=0.1uF, R_{L_CHIP}=120Ω, T_A = 25°C, FPF1004		10		µs

Note 1: Package power dissipation on 1square inch pad, 2 oz. copper board.

Typical Characteristics

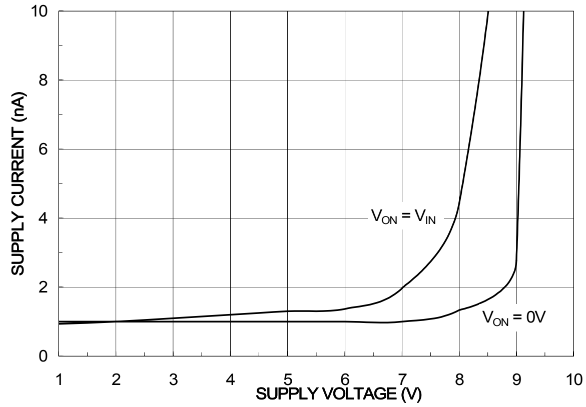


Figure 1. Quiescent Current vs. V_{IN}

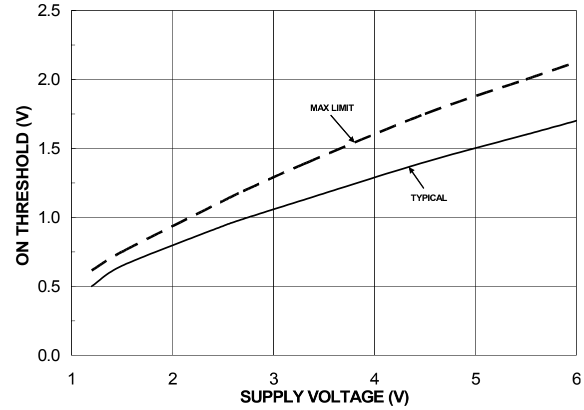


Figure 2. ON Threshold vs. V_{IN}

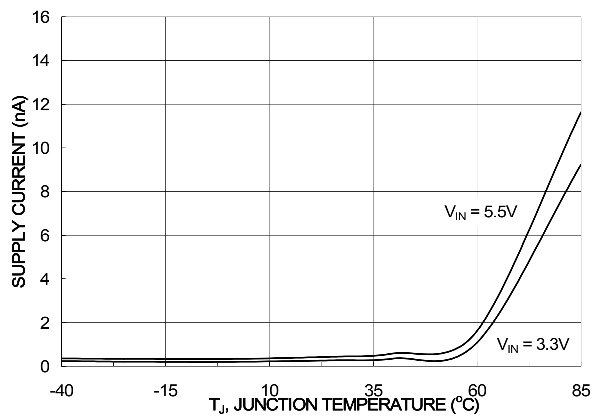


Figure 3. Quiescent Current vs. Temperature

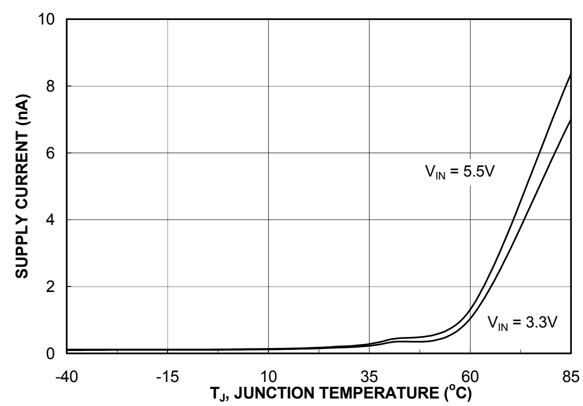


Figure 4. Quiescent Current (off) vs. Temperature

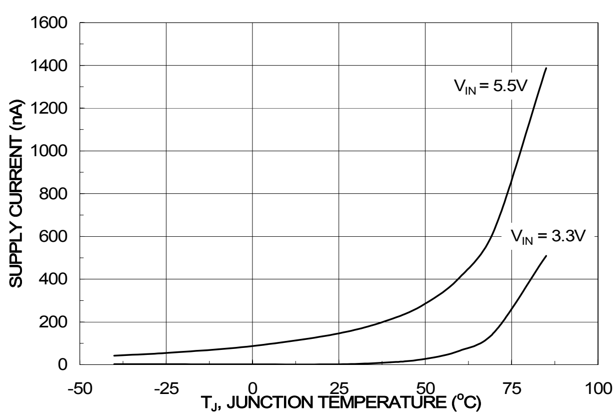


Figure 5. $I_{SWITCH-OFF}$ Current vs. Temperature

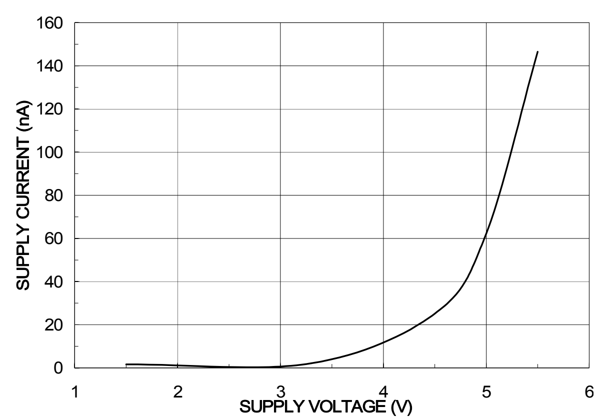


Figure 6. $I_{SWITCH-OFF}$ Current vs. V_{IN}

Typical Characteristics

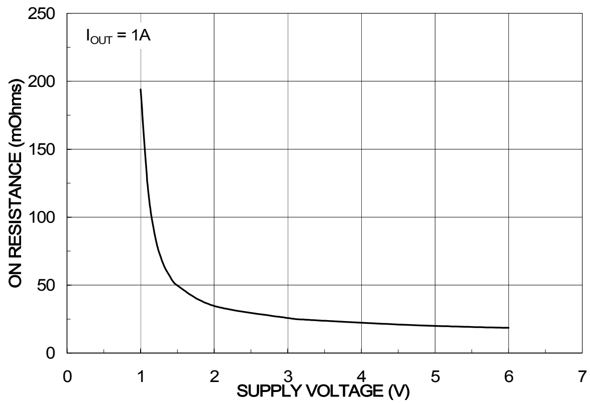


Figure 7. R_{ON} vs. V_{IN}

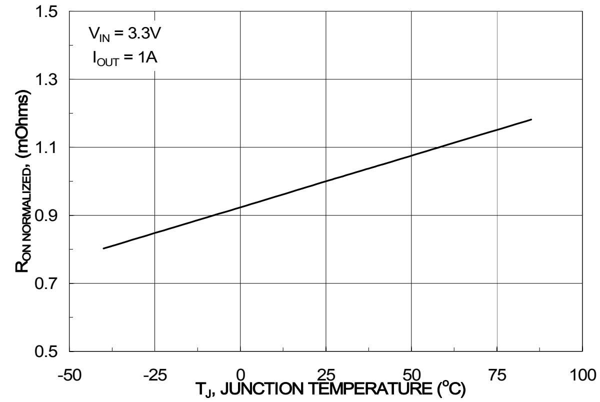


Figure 8. R_{ON} vs. Temperature

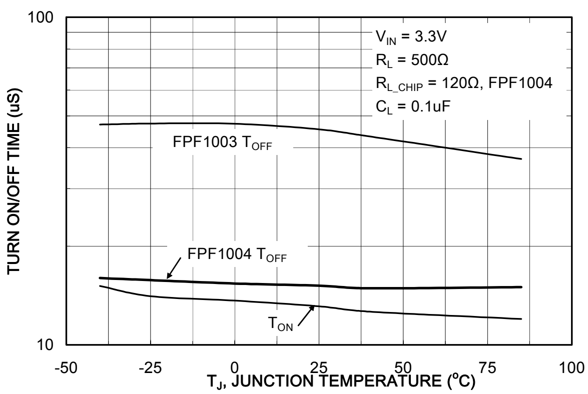


Figure 9. T_{ON}/T_{Off} vs. Temperature

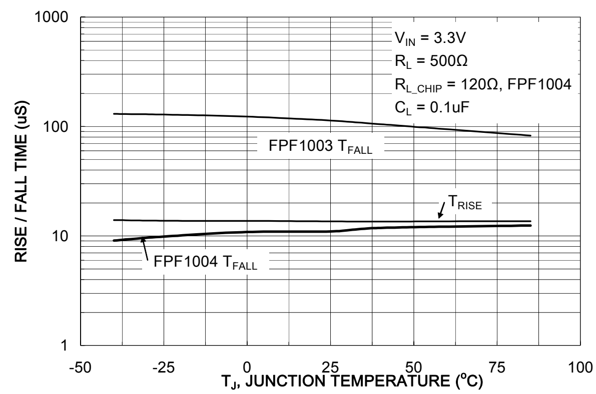


Figure 10. T_{RISE}/T_{FALL} vs. Temperature

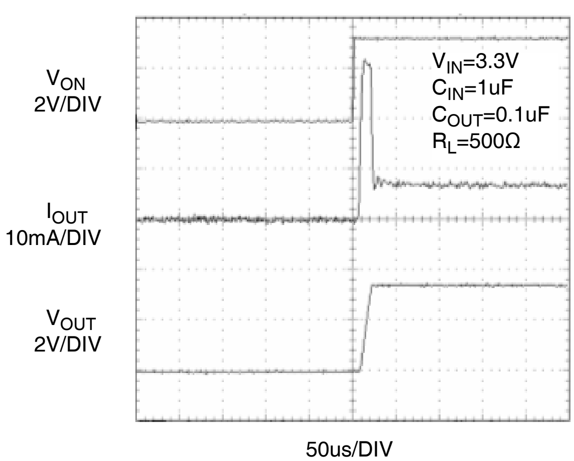


Figure 11. FPF1003 T_{ON} Response

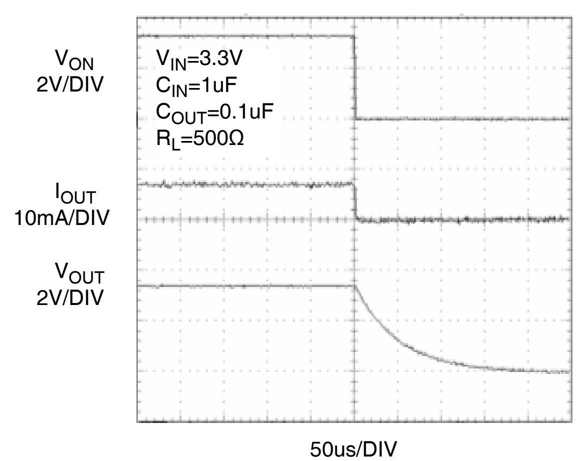


Figure 12. FPF1003 T_{OFF} Response

Typical Characteristics

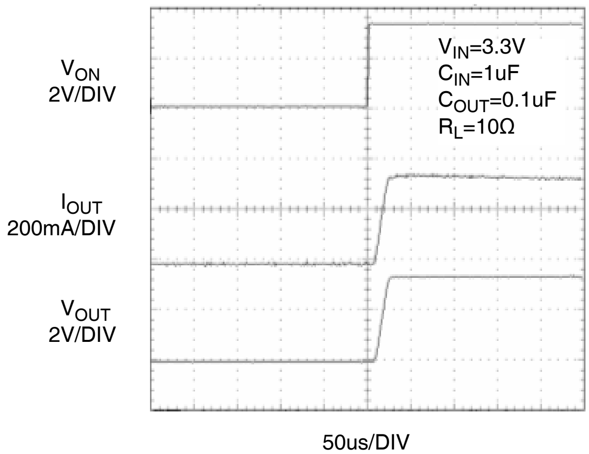


Figure 13. FPF1003 T_{ON} Response

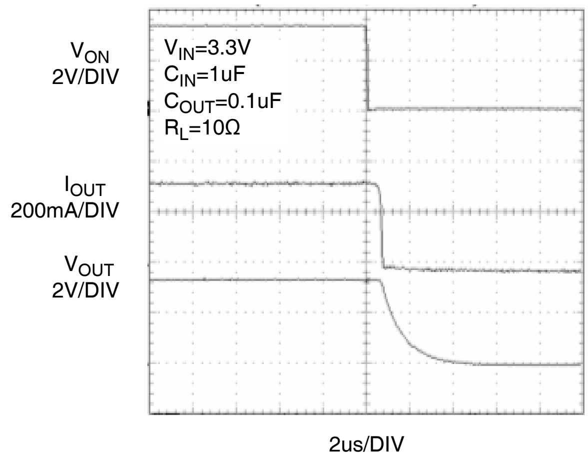


Figure 14. FPF1003 T_{OFF} Response

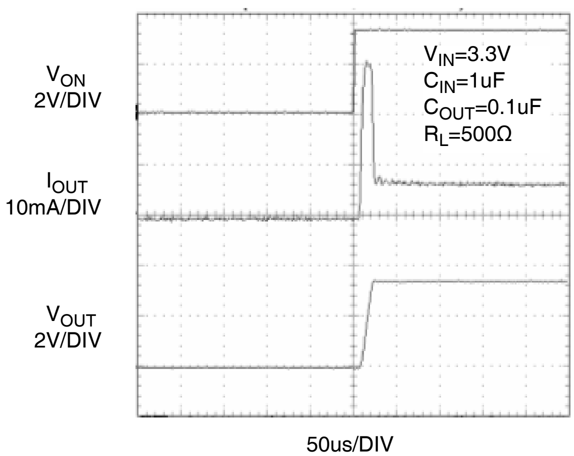


Figure 15. FPF1004 T_{ON} Response

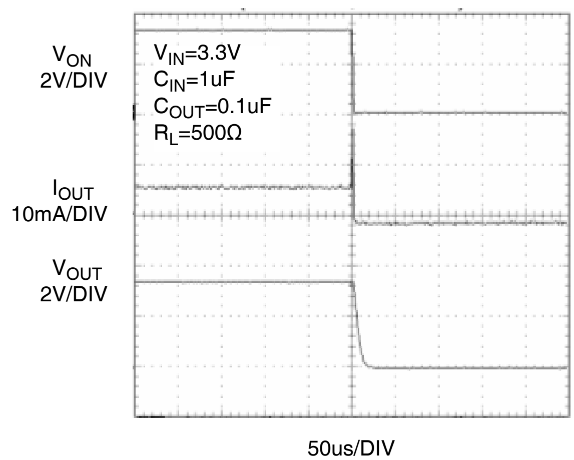


Figure 16. FPF1004 T_{OFF} Response

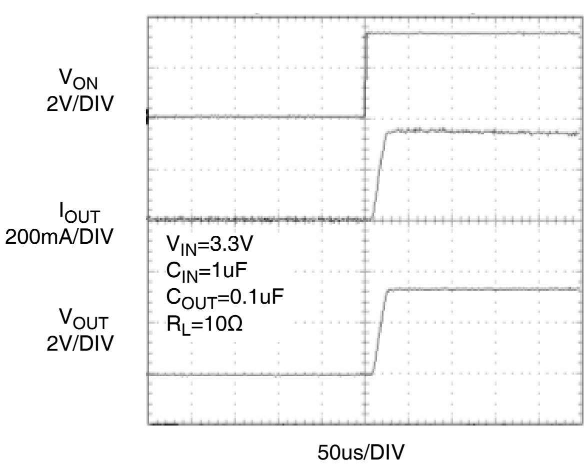


Figure 17. FPF1004 T_{ON} Response

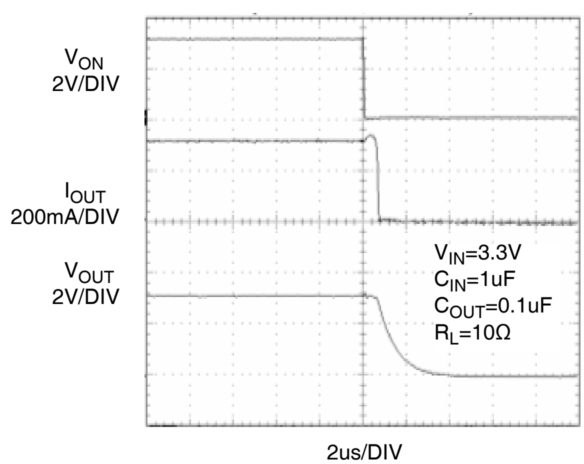


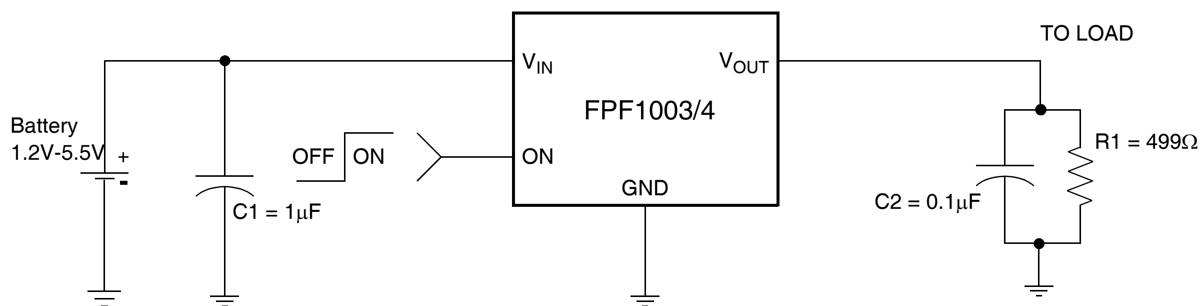
Figure 18. FPF1004 T_{OFF} Response

Description of Operation

The FPF1003 & FPF1004 are low $R_{DS(ON)}$ P-Channel load switches with controlled turn-on. The core of each device is a 30mΩ P-Channel MOSFET and a controller capable of functioning over a wide input operating range of 1.2-5.5V. Switch control is by a logic input (ON) capable of interfacing directly with low voltage control signal. In FPF1004, 120Ω on-chip load resistor is added for output quick discharge when switch is turned off.

Application Information

Typical Application



Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns-on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1μF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

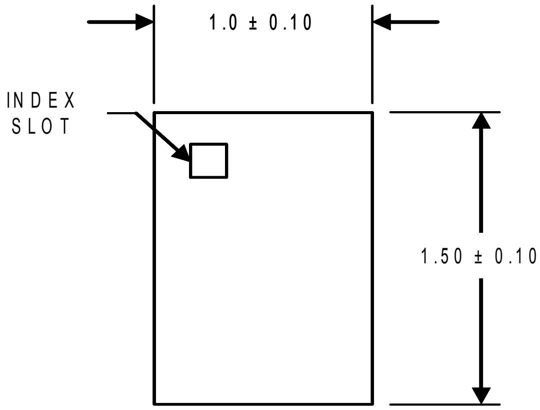
Output Capacitor

A 0.1μF capacitor, C_{OUT}, should be placed between V_{OUT} and GND. This capacitor will prevent parasitic board inductance from forcing V_{OUT} below GND when the switch turns-off. Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_{OUT} is highly recommended. A C_{OUT} greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

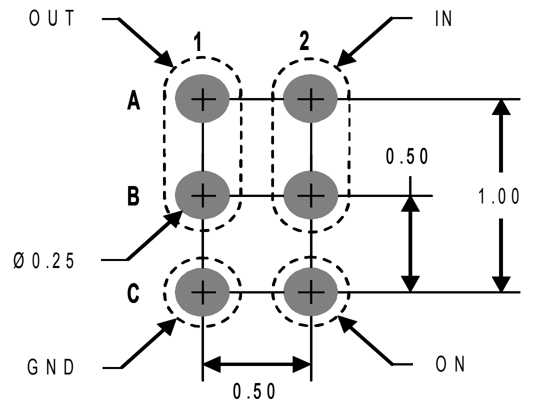
Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN}, V_{OUT} and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

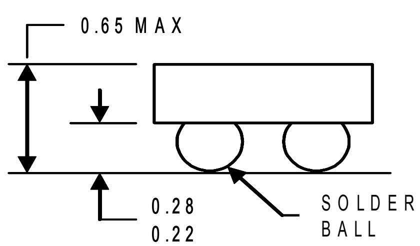
Dimensional Outline and Pad Layout



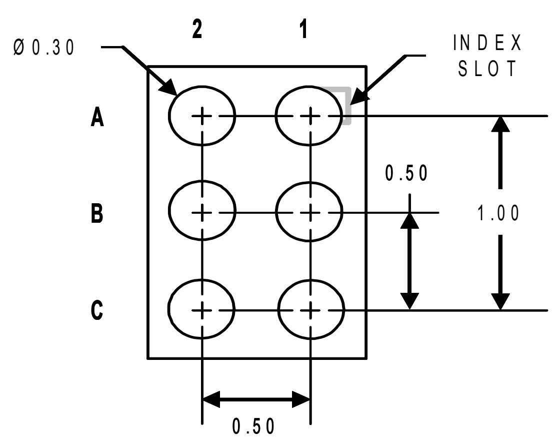
TOP VIEW



RECOMMENDED
LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A) ALL DIMENSIONS ARE IN MILLIMETERS.

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Definition of Terms

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