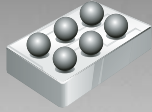


*ROHS COMPLIANT
VERSIONS
AVAILABLE



BOURNS®

Features

- Lead free versions available
- RoHS compliant (lead free version)*
- ESD protection > 25k volts
- Protects five unidirectional lines or four bidirectional lines
- Small SMT package

Applications

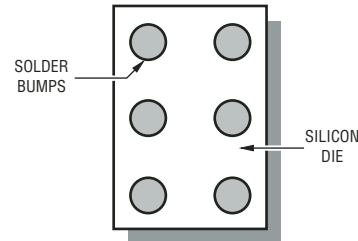
- Cell phones
- PDAs and notebooks
- Digital cameras
- MP3 players and GPS

2DAB-F6R - Integrated Passive & Active Device

General Information

The 2DAB-F6R device provides ESD protection for the I/O port of portable electronic devices such as cell phones, modems and PDAs. The device incorporates five TVS diodes which can be configured as five unidirectional lines or four bidirectional lines for interfacing to external lines.

The ESD protection provided by the component enables an I/O port to withstand a minimum ± 8 KV Contact / ± 15 KV Air Discharge per the ESD test method specified in IEC 61000-4-2. The device measures 1.00 mm x 1.50 mm and is available in a 6 bump Flip Chip package intended to be mounted directly onto an FR4 printed circuit board. The Flip Chip device meets typical thermal cycle and bend test specifications without the use of an underfill material.



Electrical & Thermal Characteristics

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)	Symbol	Minimum	Nominal	Maximum	Unit
<i>Per TVS Diode Specification</i>					
Capacitance @ 0 V 1 MHz	C	120	150	180	pF
Rated Standoff Voltage	V_{WM}		5.0		V
Breakdown Voltage @ 1 mA	V_{BR}	6.0			V
Clamping Voltage					
@ $I_p = 5$ A $t_p = 8/20$ μs	V_C			9.5	V
@ $I_{pp} = 24$ A $t_p = 8/20$ μs	V_C			11	V
Leakage Current @ 5 V	I_R		1	10	μA
ESD Protection: IEC 61000-4-2					
Contact Discharge		± 8			kV
Air Discharge		± 15			kV
Surge Protection: IEC 61000-4-5					
8/20 μs - Level 2 (Line - Gnd)		24			A
8/20 μs - Level 3 (Line - Line)		24			A
Thermal Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)					
Operating Temperature Range	T_J	-40	25	+85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55	25	+150	$^\circ\text{C}$
Peak Pulse Power ($t_p = 8/20$ μs)	P_{PP}			250	W

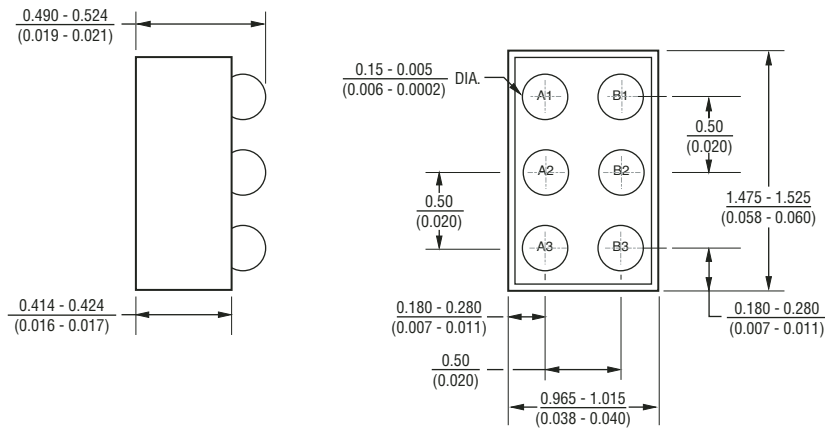
*RoHS Directive 2002/95/EC Jan 27 2003 including Annex

Specifications are subject to change without notice.

Customers should verify actual device performance in their specific applications.

Mechanical Characteristics

This is a silicon-based device and is packaged using chip scale packaging technology. Solder bumps, formed on the silicon die, provide the interconnect medium from die to PCB. The bumps are arranged on the die in a regular grid formation. The grid pitch is 0.5 mm and the dimensions for the packaged device are shown below.



DIMENSIONS = $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$

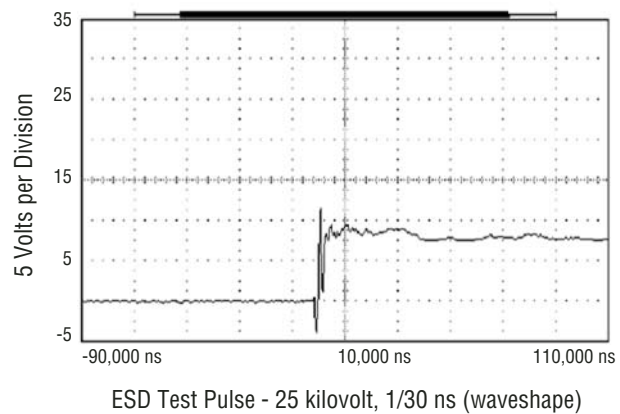
Reliability Data

Reliability data is gathered on an ongoing basis for Bourns® Integrated Passive and Active Devices.

“Package level” testing of the integrity of the solder joint is carried out on an independent Daisy-Chain test device. A 25-Pin Daisy Chain component is available from Bourns for this purpose (part number 2TAD-C25R). This is a 5 x 5 array featuring 0.5 mm pitch solder bumps. The Distance to Neutral Point (DNP) on that component is larger than that of the 2DAB-F6R and is thus deemed suitable for Thermal Cycle testing.

“Silicon level” reliability performance is based on similarity to other integrated passive CSP devices from Bourns.

Overshoot and Clamping Voltage Response



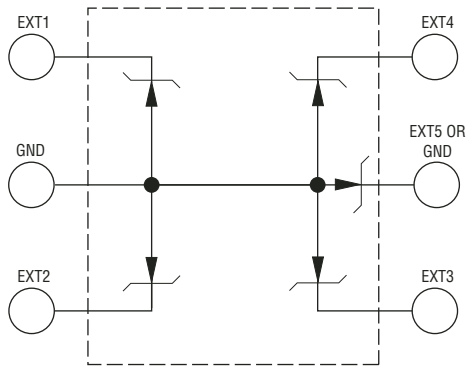
ESD Test Pulse - 25 kilovolt, 1/30 ns (waveshape)

2DAB-F6R - Integrated Passive & Active Device

BOURNS®

Block Diagram

The CSP device block diagram below includes the pin names and basic electrical connections associated with each channel.



PCB Design and SMT Processing

Please consult the "Bourns Design Guide Using CSP" for notes on PCB design and SMT Processing.

How to Order

2 DAB - F6R

Thinfilmm _____
Model _____
Flip Chip _____
No. of Solder Bumps _____
Packaging Option _____
R = Tape and Reel
Packaged 5000 pcs. / 7 " reel

Terminations _____
LF = Sn/Ag/Cu (lead free)
Blank = Sn/Pb

