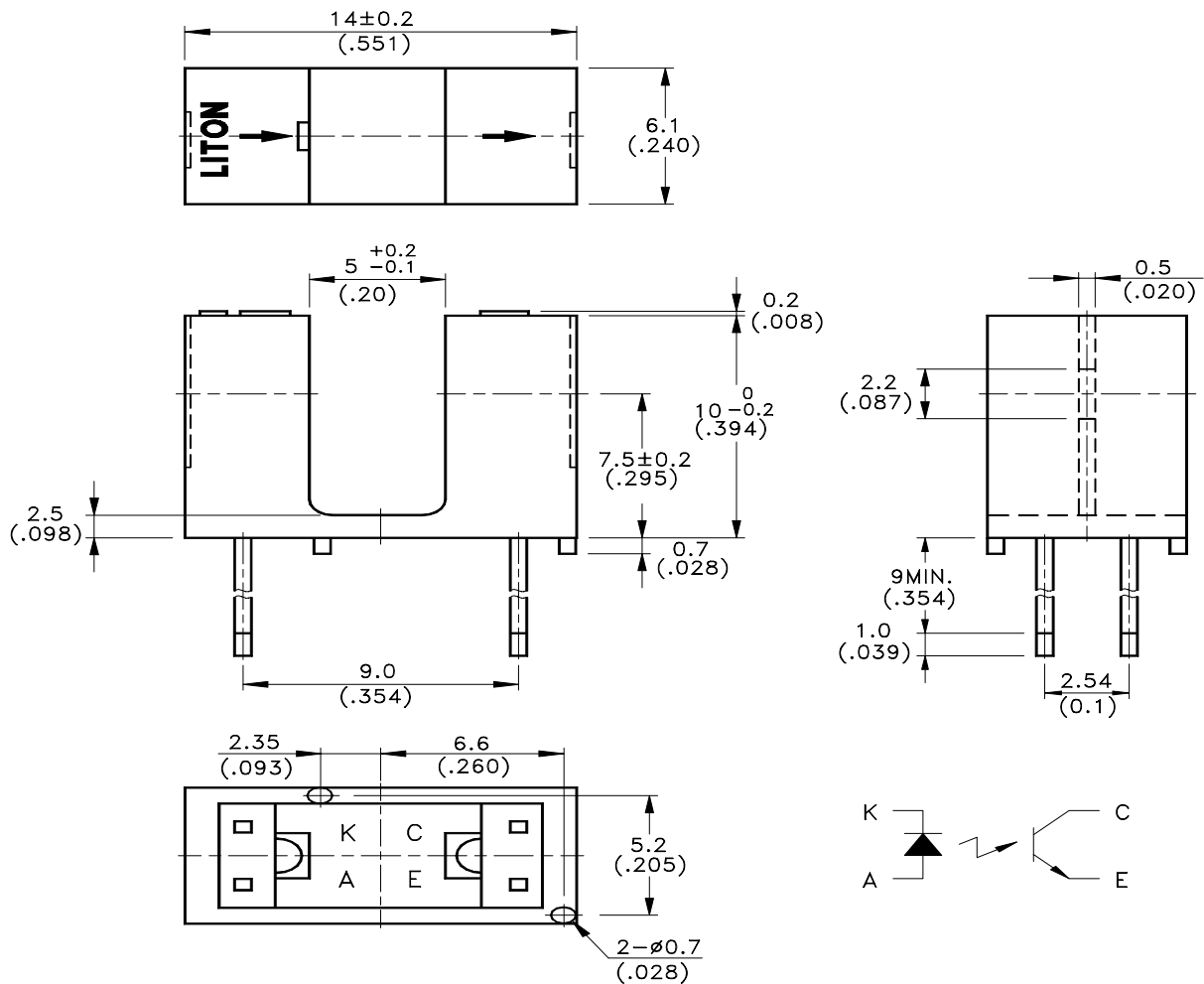


FEATURES

- * NON-CONTACT SWITCHING.
- * FOR DIRECT PC BOARD OR DUAL-IN-LINE SOCKET MOUNTING.
- * FAST SWITCHING SPEED.

PACKAGE DIMENSIONS



NOTES:

1. All dimensions are in millimeters (inches).
2. Tolerance is ± 0.25 mm(.010") unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS AT T_A=25

PARAMETER	MAXIMUM RATING	UNIT
IR Diode Continuous Forward Current	60	mA
IR Diode Reverse Voltage	5	V
Transistor Collector Current	20	mA
Transistor Power Dissipation	75	mW
IR Diode Peak Forward Current (Pulse Wide = 10 μ S, 300 pps)	1	A
Diode Power Dissipation	100	mW
Phototransistor Collector-Emitter Voltage	30	V
Phototransistor Emitter-Collector Voltage	5	V
Operating Temperature Range	-25 to + 85	
Storage Temperature Range	-40 to + 100	
Lead Soldering Temperature [1.6mm(.063") From Case]	260 for 5 Seconds	

ELECTRICAL OPTICAL CHARACTERISTICS AT TA=25

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
INPUT LED						
Forward Voltage	VF		1.2	1.6	V	IF = 20mA
Reverse Current	IR			100	μ A	VR=5V
OUTPUT PHOTOTRANSISTOR						
Collector-Emitter Breakdown Voltage	V(BR)CEO	30			V	IC=1mA
Emitter-Collector Breakdown Voltage	V(BR)ECO	5			V	IE=100 μ A
Collector-Emitter Dark Current	ICEO			100	nA	VCE=10V
COUPLER						
Collector-Emitter Saturation Voltage	VCE(SAT)			0.4	V	IC=0.25mA IF=20mA
On State Collector Current	Ic(ON)	0.6			mA	VCE=5V IF=20mA
Response Time	Rise Time	tr	3	15	μS	VCE=5V,Ic=2mA RL=100Ω
	Fall Time	tf	4	20		

TYPICAL ELECTRICAL / OPTICAL CHARACTERISTICS CURVES

(25 Ambient Temperature Unless Otherwise Noted)

Fig.1 Power Dissipation vs. Ambient Temperature

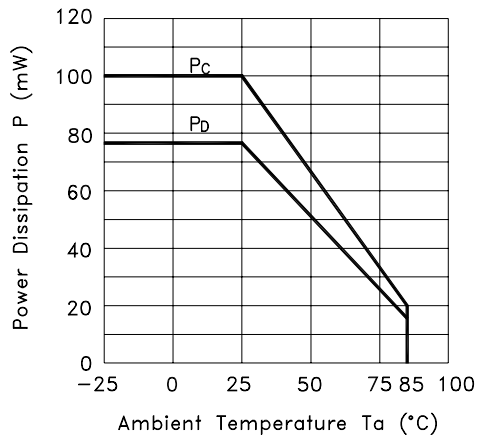


Fig.2 Forward Current vs. Forward Voltage

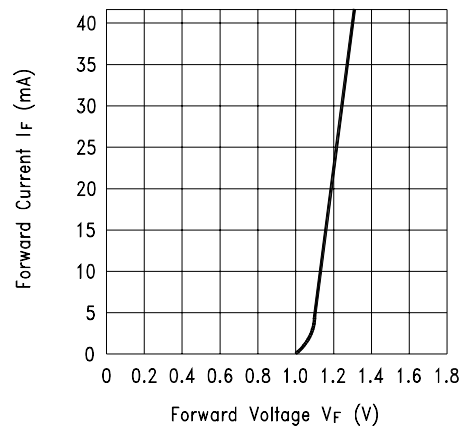


Fig.3 Collector Current vs. Forward Voltage

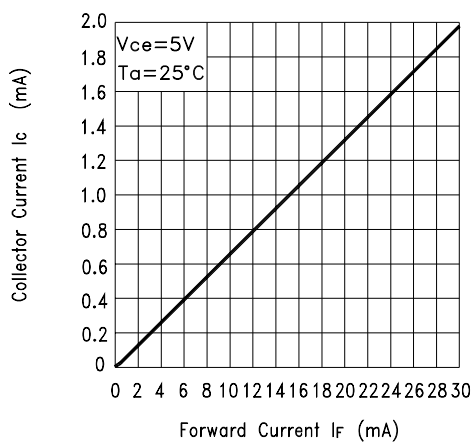
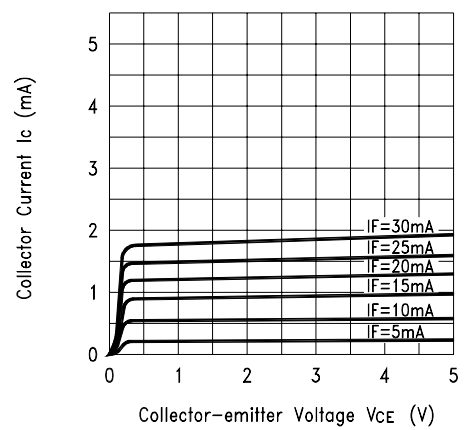


Fig.4 Collector Current vs. Collector-emitter Voltage



TYPICAL ELECTRICAL / OPTICAL CHARACTERISTICS CURVES

(25 Ambient Temperature Unless Otherwise Noted)

Fig.5 Collector Current vs. Ambient Temperature

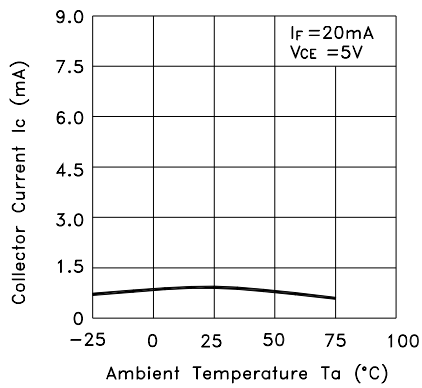


Fig.6 Collector-emitter Saturation Voltage vs. Ambient Temperature

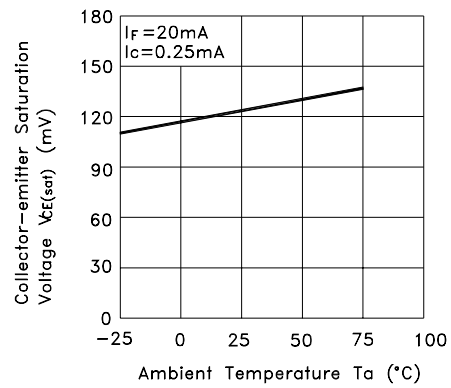
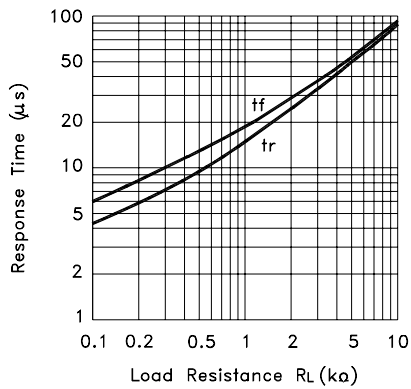


Fig.7 Response Time vs. Load Resistance



Test Circuit for Response Time

