

## 512Kx32 SRAM / FLASH MODULE

### FEATURES

- Access Times of 25ns (SRAM) and 70, 90ns (FLASH)
- Packaging
  - 66 pin, PGA Type, 1.385" square HIP, Hermetic Ceramic HIP (Package 402)
  - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880") square (Package 509) 4.57mm (0.180") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Figure 2). Package to be developed.
- 512Kx32 SRAM
- 512Kx32 5V Flash
- Organized as 512Kx32 of SRAM and 512Kx32 of Flash Memory with common Data Bus
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs

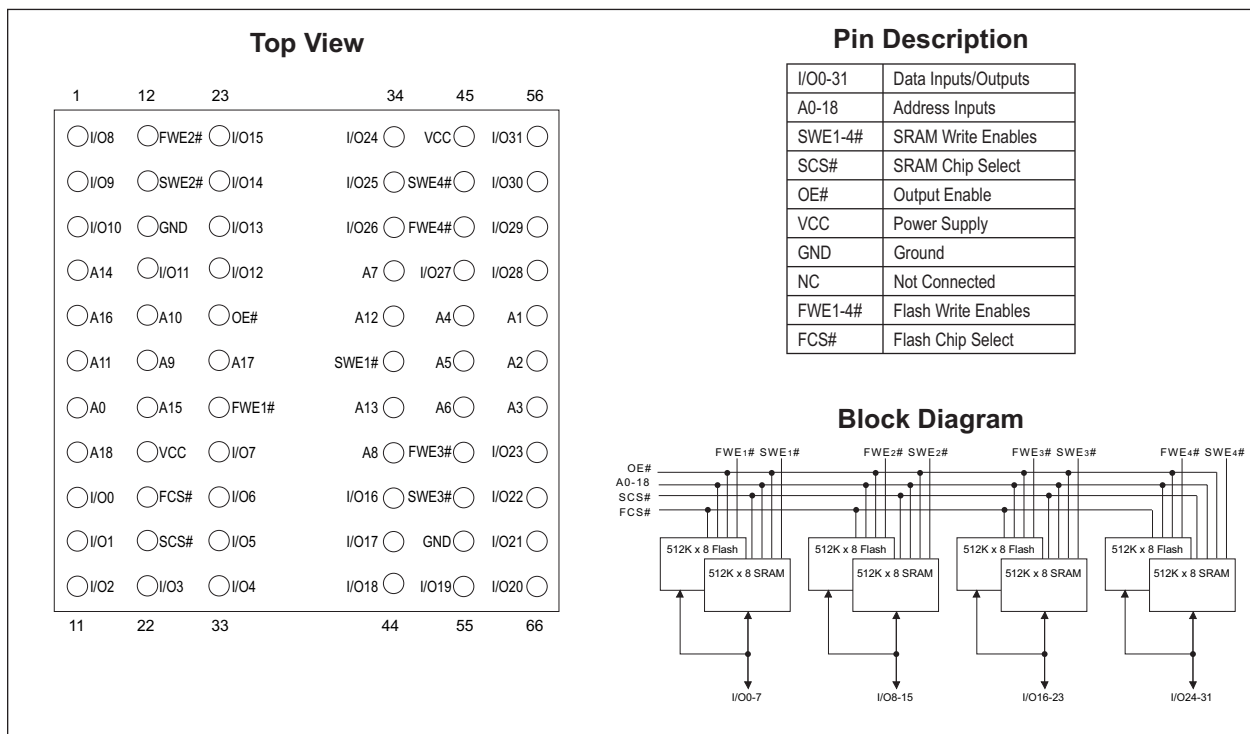
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 13 grams typical

### FLASH MEMORY FEATURES

- 100,000 Erase/Program Cycles
- Sector Architecture
  - 8 equal size sectors of 64KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection
- Page Program Operation and Internal Program Control Time.

\* This product is subject to change without notice.  
 Note: Programming information available upon request.

**Figure 1 – PIN CONFIGURATION FOR WSF512K32-29H2X**



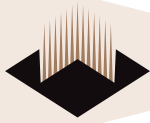
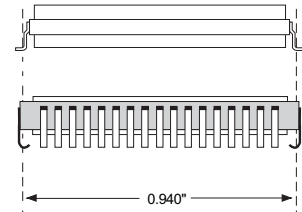
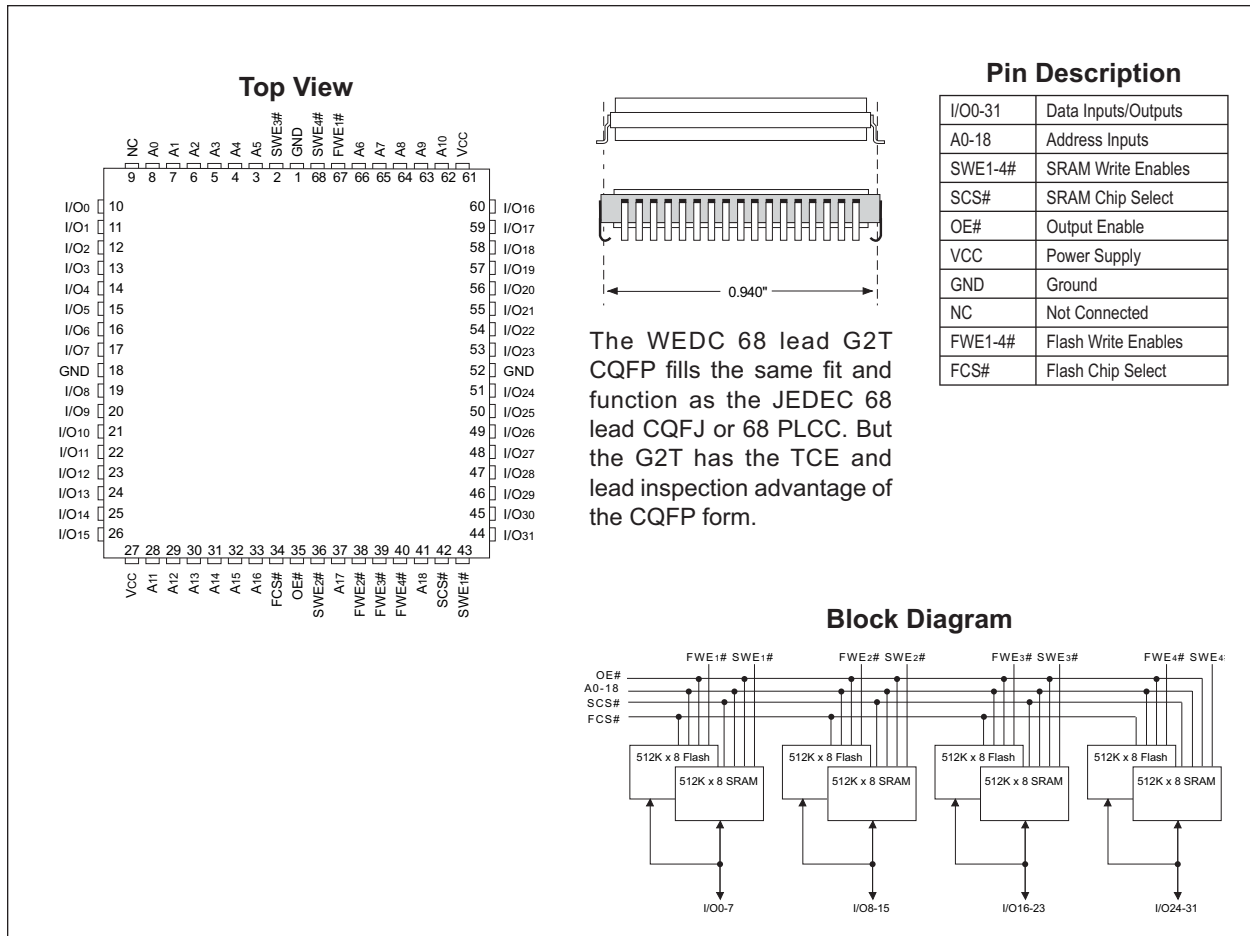
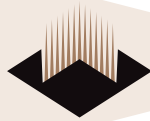


FIGURE 2 – PIN CONFIGURATION FOR WSF512K32-29G2TX



The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	7.0	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

Parameter	
Flash Data Retention	20 years
Flash Endurance (write/erase cycles)	100,000

**NOTE:**

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V

**SRAM TRUTH TABLE**

SCS#	OE#	SWE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

**NOTE:**

- FCS# must remain high when SCS# is low.

**CAPACITANCE**

T<sub>a</sub> = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	80	pF
F/S WE <sub>1-4</sub> # capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	30	pF
F/S CS# capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF
D <sub>0-31</sub> capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	30	pF
A <sub>0-18</sub> capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	80	pF

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	µA
Output Leakage Current	I <sub>LO</sub>	SCS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	µA
SRAM Operating Supply Current x 32 Mode	I <sub>CCx32</sub>	SCS# = V <sub>IL</sub> , OE# = FCS# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		550	mA
Standby Current	I <sub>SB</sub>	FCS# = SCS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		90	mA
SRAM Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 6mA, V <sub>CC</sub> = 4.5		0.4	V
SRAM Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4		V
Flash V <sub>CC</sub> Active Current for Read (1)	I <sub>CC1</sub>	FCS# = V <sub>IL</sub> , OE# = SCS# = V <sub>IH</sub>		250	mA
Flash V <sub>CC</sub> Active Current for Program or Erase (2)	I <sub>CC2</sub>	FCS# = V <sub>IL</sub> , OE# = SCS# = V <sub>IH</sub>		300	mA
Flash Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA, V <sub>CC</sub> = 4.5		0.45	V
Flash Output High Voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5	0.85 x V <sub>CC</sub>		V
Flash Output High Voltage	V <sub>OH2</sub>	I <sub>OH</sub> = -100 µA, V <sub>CC</sub> = 4.5	V <sub>CC</sub> - 0.4		V
Flash Low V <sub>CC</sub> Lock Out Voltage	V <sub>LKO</sub>		3.2	4.2	V

**NOTES:**

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2mA/MHz, with OE# at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V



**SRAM AC CHARACTERISTICS**

$V_{CC} = 5.0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter Read Cycle	Symbol	-25		Units
		Min	Max	
Read Cycle Time	$t_{RC}$	25		ns
Address Access Time	$t_{AA}$		25	ns
Output Hold from Address Change	$t_{OH}$	0		ns
Chip Select Access Time	$t_{ACS}$		25	ns
Output Enable to Output Valid	$t_{OE}$		15	ns
Chip Select to Output in Low Z	$t_{CLZ}^1$	3		ns
Output Enable to Output in Low Z	$t_{OLZ}^1$	0		ns
Chip Disable to Output in High Z	$t_{CHZ}^1$		12	ns
Output Disable to Output in High Z	$t_{OHZ}^1$		12	ns

1. This parameter is guaranteed by design but not tested.

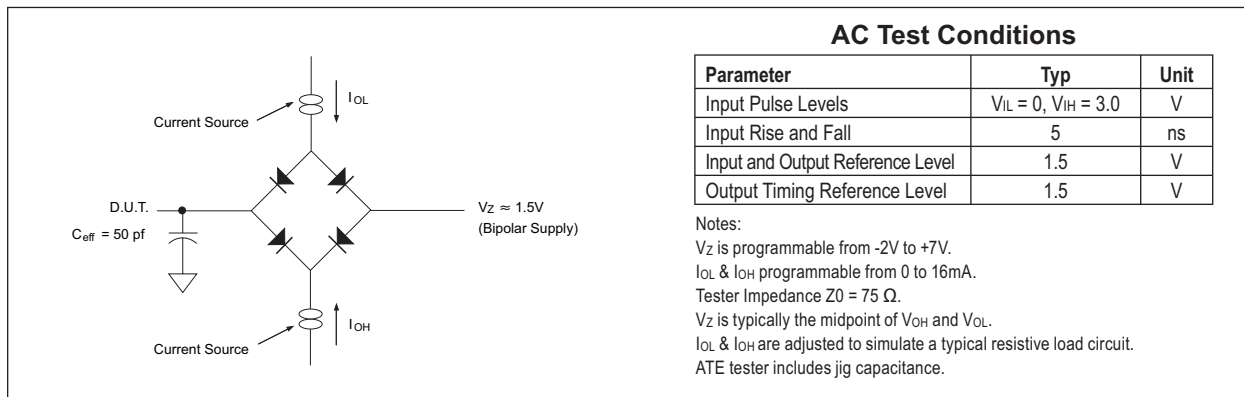
**SRAM AC CHARACTERISTICS**

$V_{CC} = 5.0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter Write Cycle	Symbol	-25		Units
		Min	Max	
Write Cycle Time	$t_{WC}$	25		ns
Chip Select to End of Write	$t_{CW}$	20		ns
Address Valid to End of Write	$t_{AW}$	20		ns
Data Valid to End of Write	$t_{DW}$	15		ns
Write Pulse Width	$t_{WP}$	20		ns
Address Setup Time	$t_{AS}$	3		ns
Address Hold Time	$t_{AH}$	0		ns
Output Active from End of Write	$t_{OW}^1$	3		ns
Write Enable to Output in High Z	$t_{WHZ}^1$		15	ns
Data Hold from Write Time	$t_{DH}$	0		ns

1. This parameter is guaranteed by design but not tested.

**FIGURE 3 AC TEST CIRCUIT**



**AC Test Conditions**

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:  
 $V_Z$  is programmable from -2V to +7V.  
 $I_{OL}$  &  $I_{OH}$  programmable from 0 to 16mA.  
 Tester Impedance  $Z_0 = 75 \Omega$ .  
 $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .  
 $I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.  
 ATE tester includes jig capacitance.



FIGURE 4 – SRAM TIMING WAVEFORM - READ CYCLE

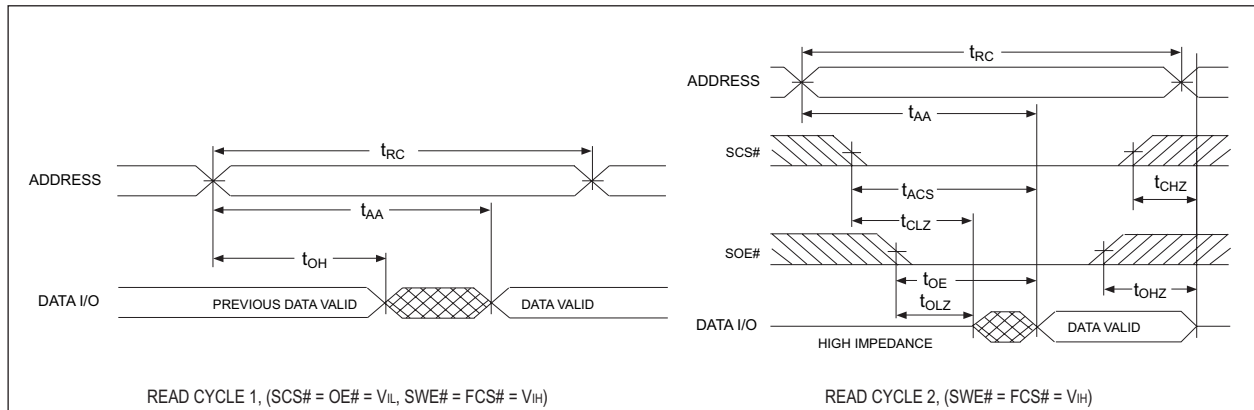


FIGURE 5 – SRAM WRITE CYCLE - SWE# CONTROLLED

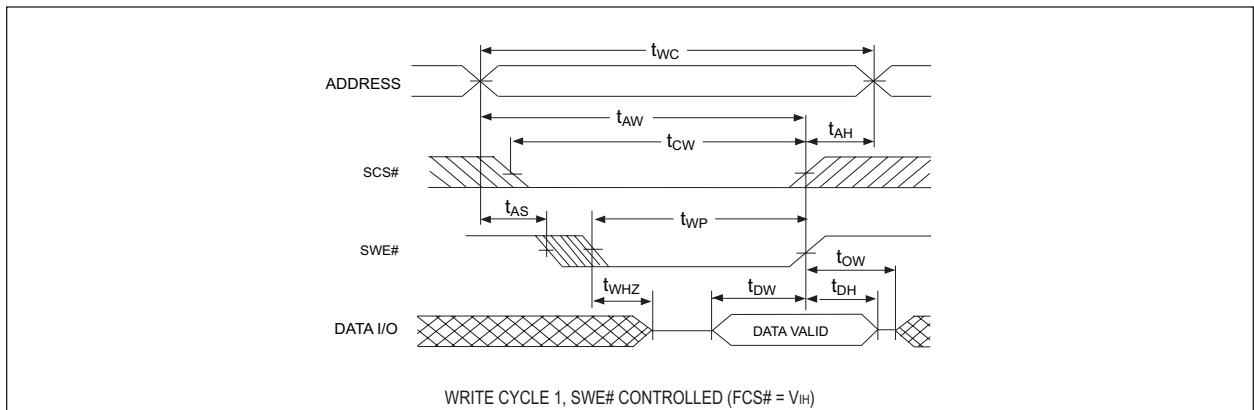
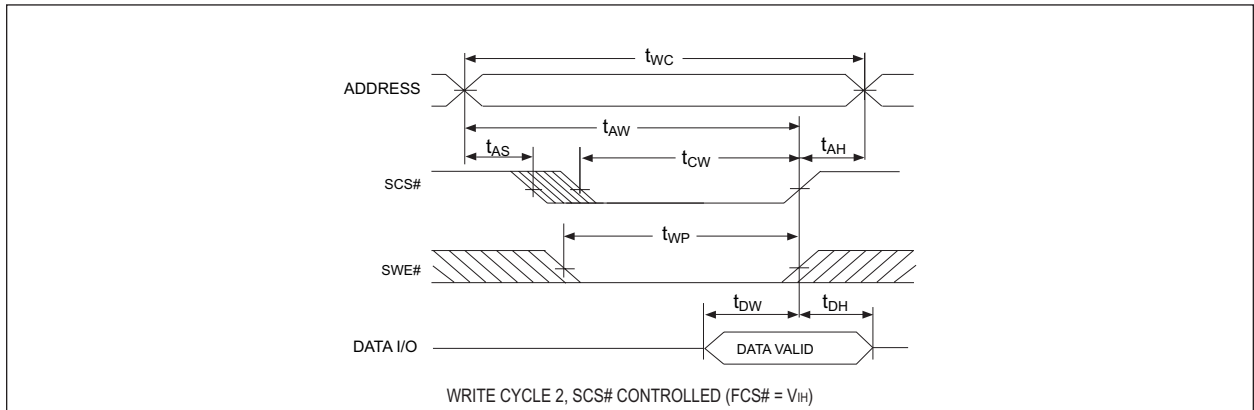


FIGURE 6 – SRAM WRITE CYCLE - SCS# CONTROLLED





**FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FWE# CONTROLLED**

V<sub>CC</sub> = 5.0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-70		-90		Unit
			Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	70		90		ns
Chip Select Setup Time	t <sub>ELWL</sub>	t <sub>CS</sub>	0		0		ns
Write Enable Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	45		45		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		0		ns
Data Setup Time	t <sub>DVWH</sub>	t <sub>DS</sub>	45		45		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		0		ns
Address Hold Time	t <sub>WLAX</sub>	t <sub>AH</sub>	45		45		ns
Write Enable Pulse Width High	t <sub>WHWL</sub>	t <sub>WPH</sub>	20		20		ns
Duration of Byte Programming Operation (1)	t <sub>WHWH1</sub>			300		300	μs
Chip and Sector Erase Time (2)	t <sub>WHWH2</sub>			15		15	sec
Read Recovery Time Before Write	t <sub>GHWL</sub>		0		0		μs
VCC Set-up Time		t <sub>VCS</sub>	50		50		μs
Chip Programming Time				11		11	sec
Output Enable Setup Time		t <sub>OES</sub>	0		0		ns
Output Enable Hold Time (4)		t <sub>OEH</sub>	10		10		ns
Chip Erase Time (3)				64		64	sec

**NOTES:**

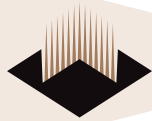
1. Typical value for t<sub>WHWH1</sub> is 7ns.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 8sec.
4. For Toggle and Data# Polling.

**FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS**

V<sub>CC</sub> = 5.0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-70		-90		Unit
			Min	Max	Min	Max	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	70		90		ns
Address Access Time	t <sub>AVQV</sub>	t <sub>ACC</sub>		70		90	ns
Chip Select Access Time	t <sub>ELQV</sub>	t <sub>CE</sub>		70		90	ns
OE# to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		35		35	ns
Chip Select to Output High Z (1)	t <sub>EHQZ</sub>	t <sub>DF</sub>		20		20	ns
OE# High to Output High Z (1)	t <sub>GHQZ</sub>	t <sub>DF</sub>		20		20	ns
Output Hold from Address, FCS# or OE# Change, whichever is first	t <sub>AXQX</sub>	t <sub>OH</sub>	0		0		ns

1. Guaranteed by design, not tested.



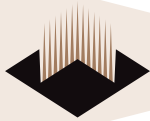
**FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FCS# CONTROLLED**

$V_{CC} = 5.0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

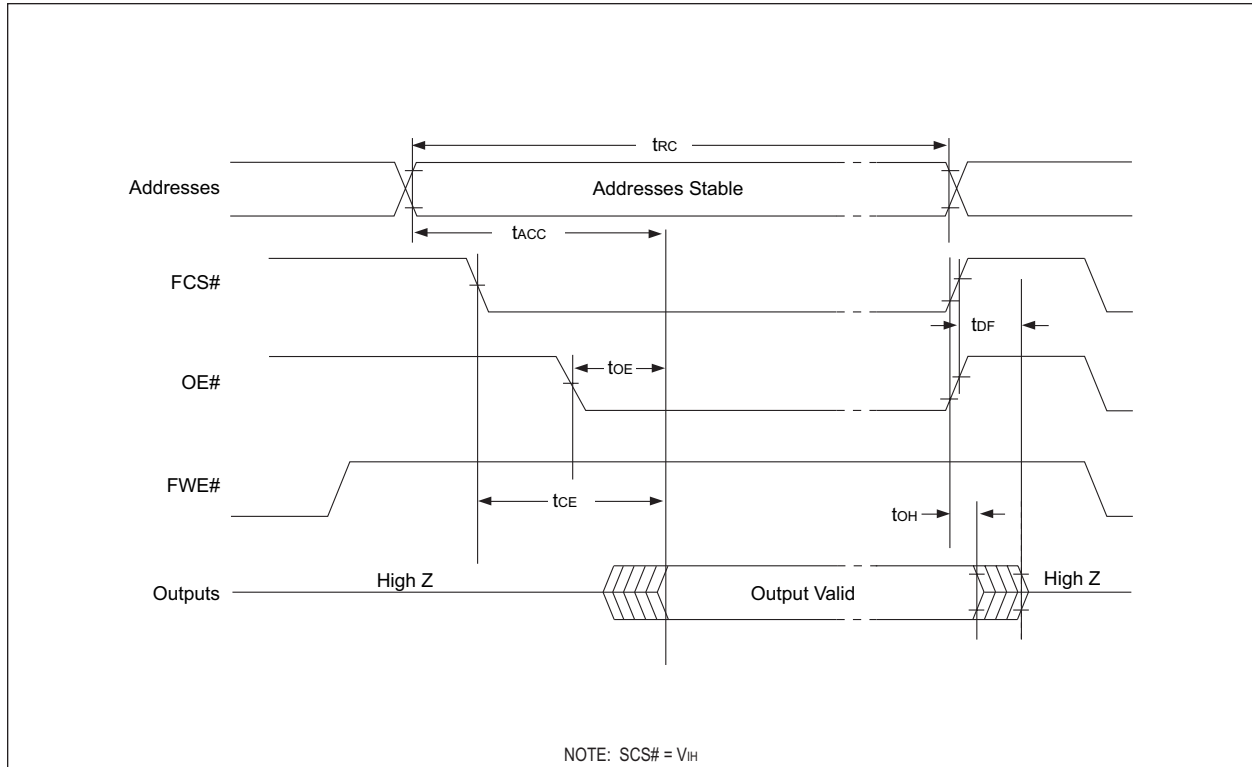
Parameter	Symbol		-70		-90		Unit
			Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	70		90		ns
FWE# Setup Time	t <sub>WLEL</sub>	t <sub>WS</sub>	0		0		ns
FCS# Pulse Width	t <sub>ELEH</sub>	t <sub>CP</sub>	45		45		ns
Address Setup Time	t <sub>AVEL</sub>	t <sub>AS</sub>	0		0		ns
Data Setup Time	t <sub>DVEH</sub>	t <sub>DS</sub>	45		45		ns
Data Hold Time	t <sub>EHDH</sub>	t <sub>DH</sub>	0		0		ns
Address Hold Time	t <sub>ELAX</sub>	t <sub>AH</sub>	45		45		ns
FCS# Pulse Width High	t <sub>EHEL</sub>	t <sub>CPH</sub>	20		20		ns
Duration of Programming Operation (1)	t <sub>WHWH1</sub>			300		300	μs
Sector Erase Time (2)	t <sub>WHWH2</sub>			15		15	sec
Read Recovery Time	t <sub>GHEL</sub>		0		0		ns
Chip Programming Time				11			sec
Chip Erase Time (3)				64			sec

**NOTES:**

1. Typical value for t<sub>WHWH1</sub> is 7ns.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 8sec.



**FIGURE 7 – AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS**





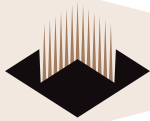


FIGURE 8 – WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY FWE# CONTROLLED

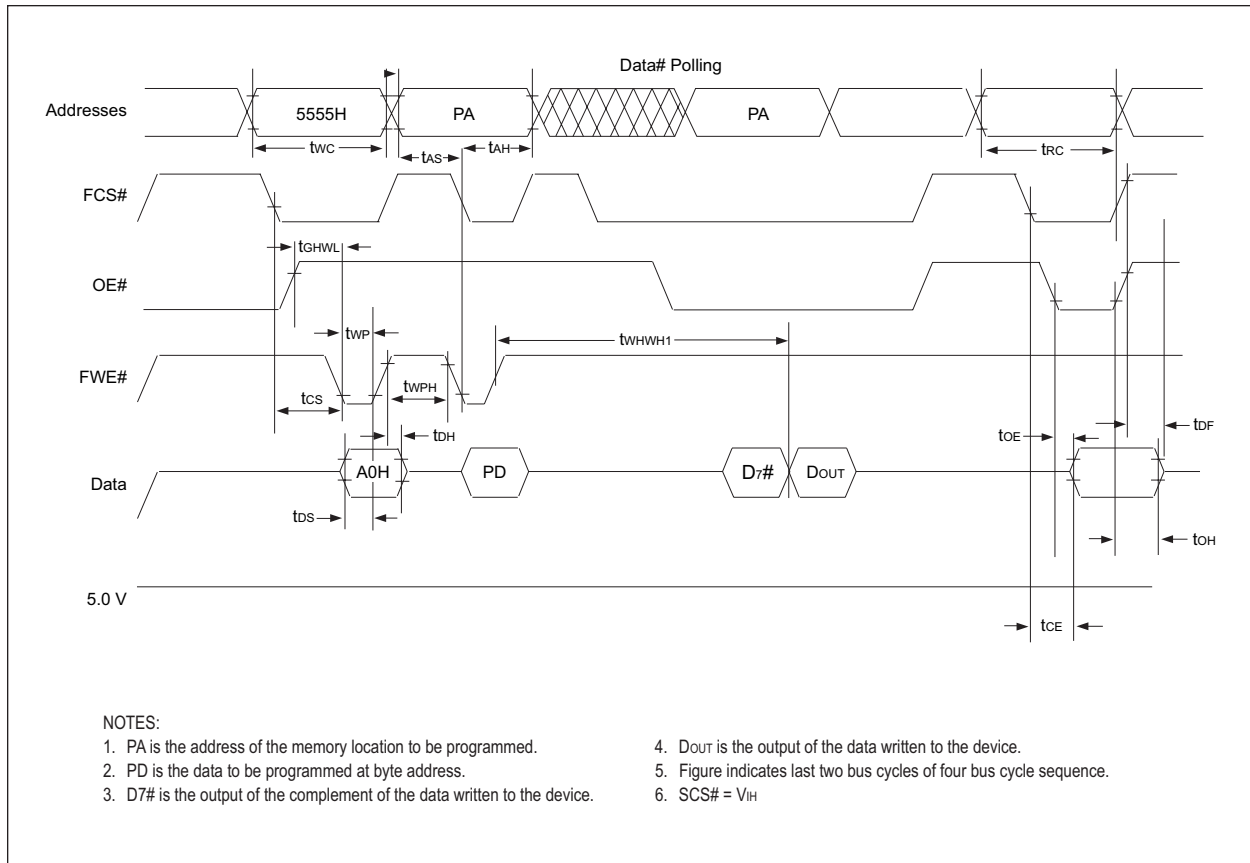
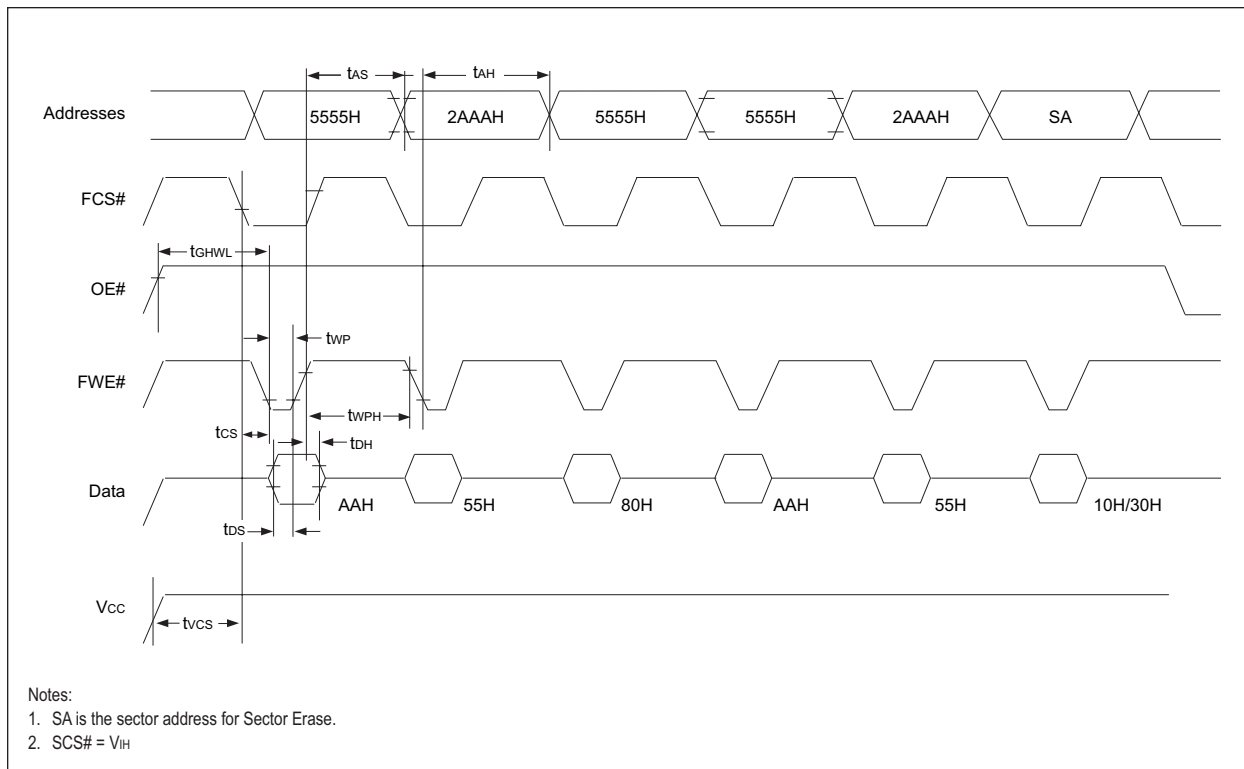




FIGURE 9 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY



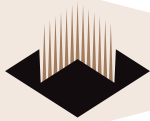


FIGURE 10 AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS FOR FLASH MEMORY

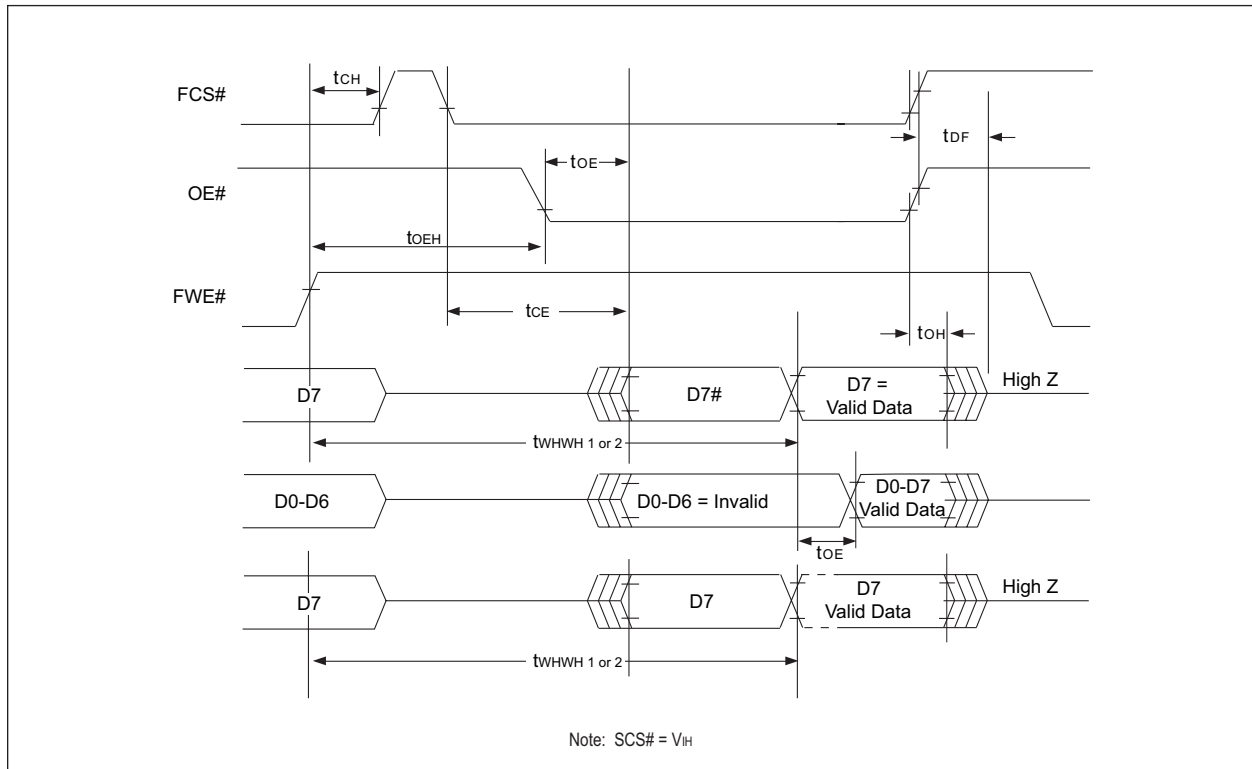
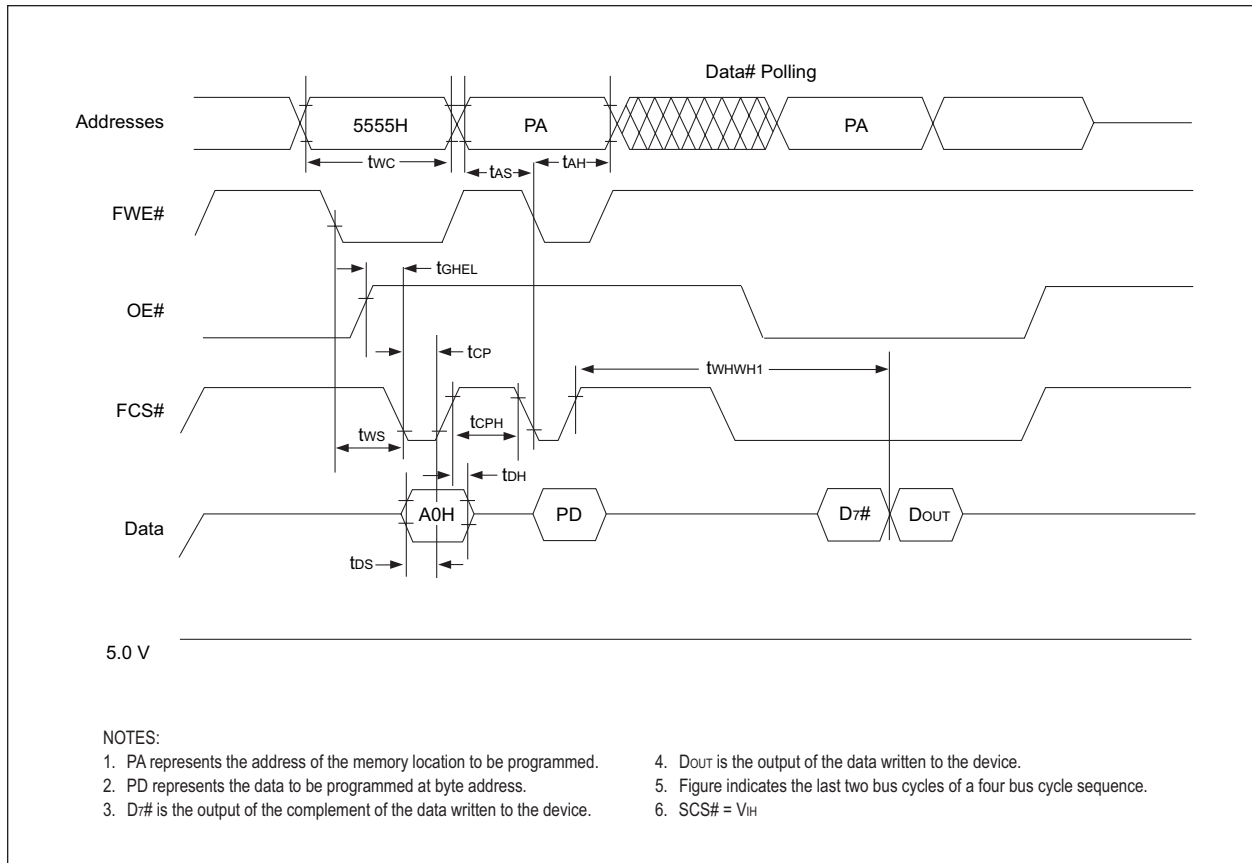


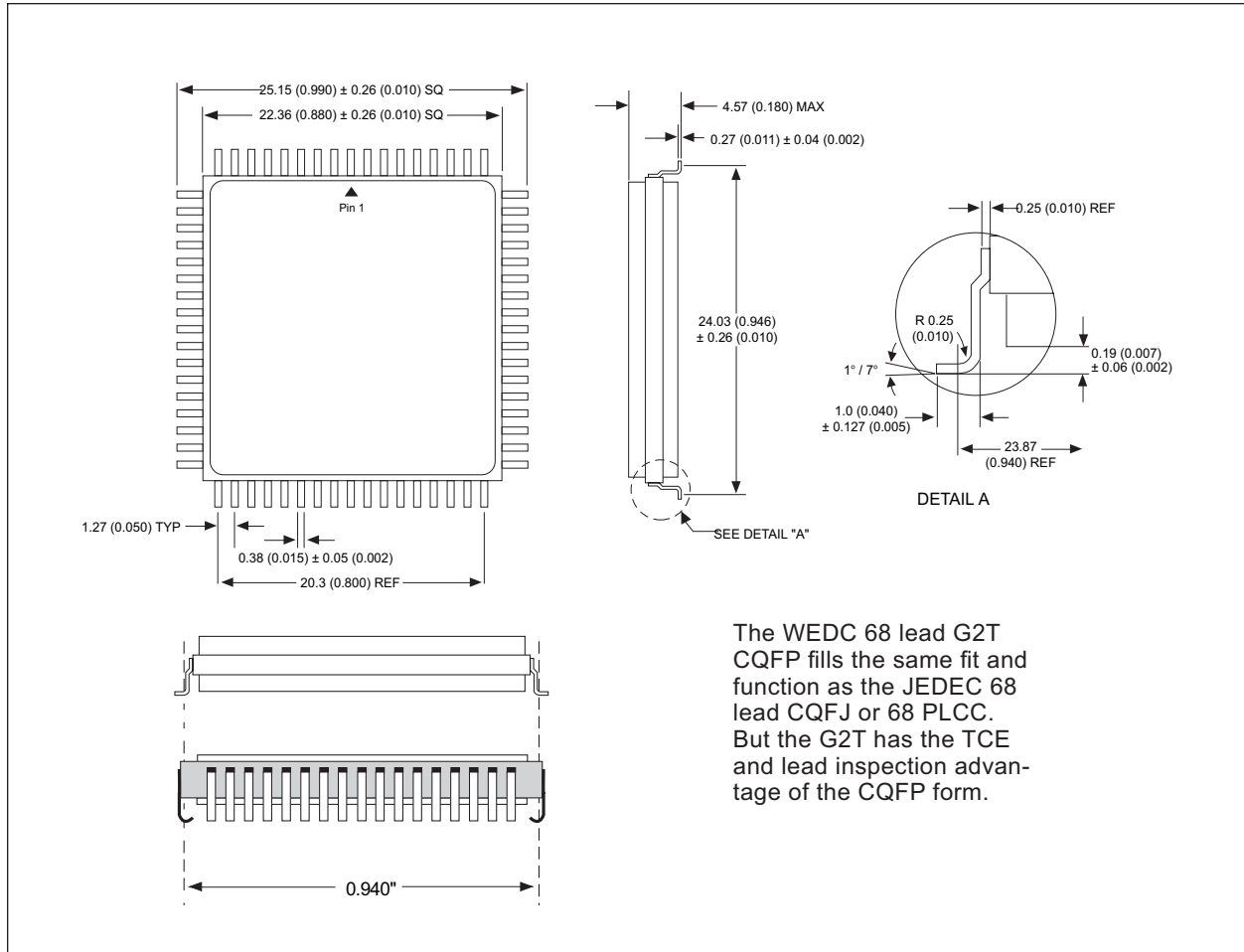


FIGURE 11 – WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY, CS# CONTROLLED





PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)

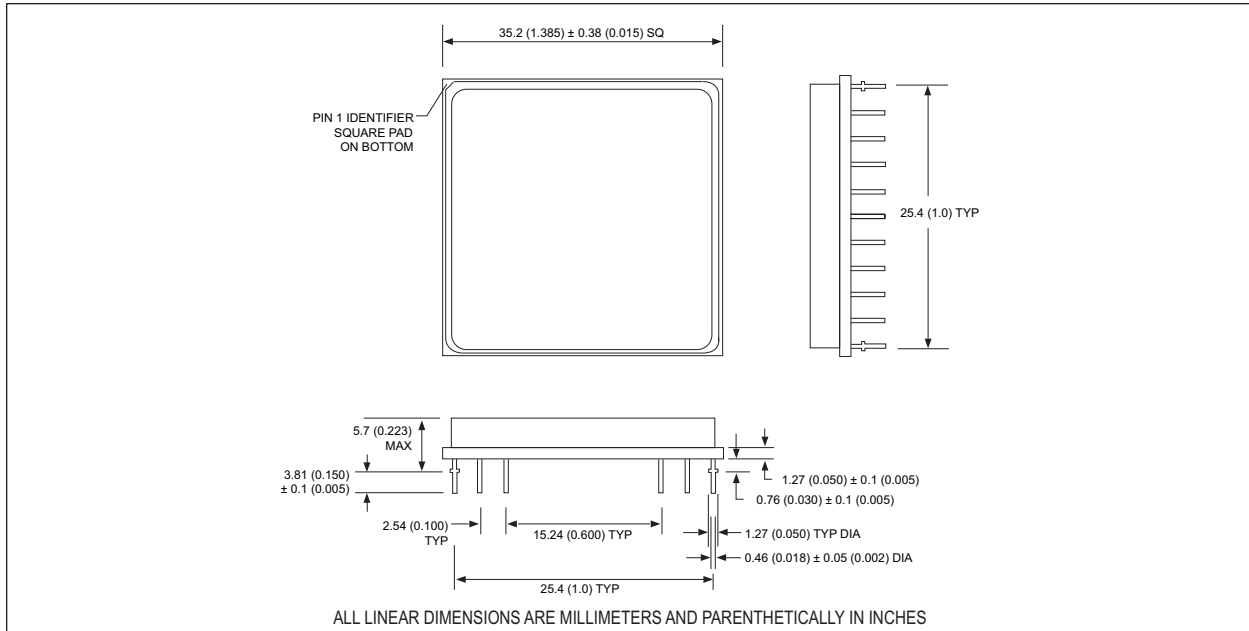


The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)**



**ORDERING INFORMATION**

