8Meg x 16
128-MBIT DDR SDRAM

PRELIMINARY INFORMATION
APRIL 2006

FEATURES

- Clock Frequency: 166, 133 MHz
- Power supply (V_{DD} and V_{DDQ}): 2.5V
- SSTL 2 interface
- Four internal banks to hide row Pre-charge and Active operations
- Commands and addresses register on positive clock edges (CK)
- Bi-directional Data Strobe signal for data capture
- Differential clock inputs (CK and $\overline{CK}$) for two data accesses per clock cycle
- Data Mask feature for Writes supported
- DLL aligns data I/O and Data Strobe transitions with clock inputs
- Half-strength and Matched drive strength options
- Programmable burst length for Read and Write operations
- Programmable CAS Latency (2, 2.5 clocks)
- Programmable burst sequence: sequential or interleaved
- Burst concatenation and truncation supported for maximum data throughput
- Auto Pre-charge option for each Read or Write burst
- 4096 refresh cycles every 64ms
- Auto Refresh and Self Refresh Modes
- Pre-charge Power Down and Active Power Down Modes
- Lead-free Availability

DEVICE OVERVIEW

ISSI's 128-Mbit DDR SDRAM achieves high-speed data transfer using pipeline architecture and two data word accesses per clock cycle. The 134,217,728-bit memory array is internally organized as four banks of 32M-bit to allow concurrent operations. The pipeline allows Read and Write burst accesses to be virtually continuous, with the option to concatenate or truncate the bursts. The programmable features of burst length, burst sequence and CAS latency enable further advantages. The device is available in 16-bit data word size. Input data is registered on the I/O pins on both edges of Data Strobe signal(s), while output data is referenced to both edges of Data Strobe and both edges of CK. Commands are registered on the positive edges of CK. Auto Refresh, Active Power Down, and Pre-charge Power Down modes are enabled by using clock enable (CKE) and other inputs in an industry-standard sequence. All input and output voltage levels are compatible with SSTL 2.

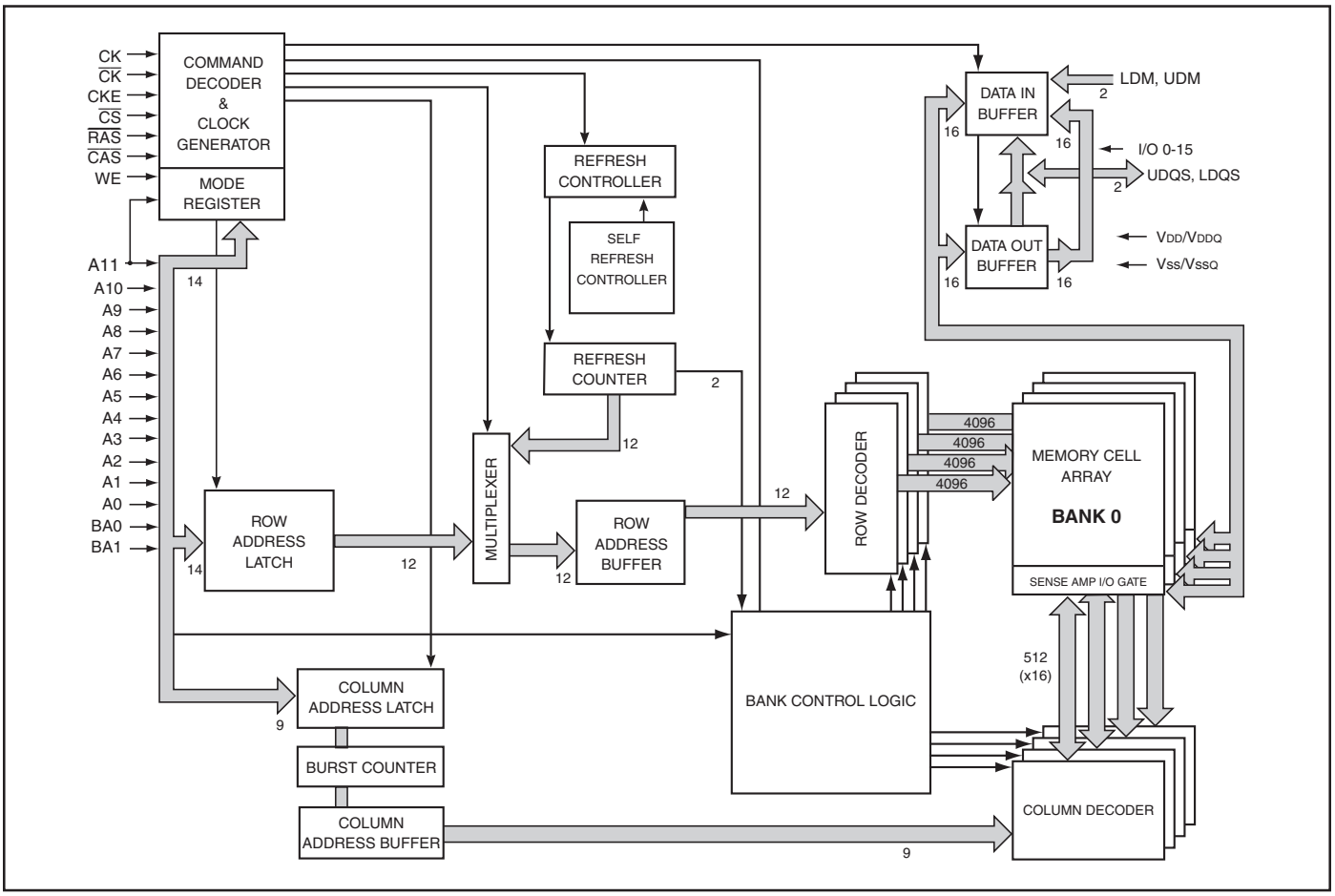
IS43R16800A-6

1M x16x8 Banks
V_{DD}: 2.5V
V_{DDQ}: 2.5V
66-pin TSOP-II

KEY TIMING PARAMETERS

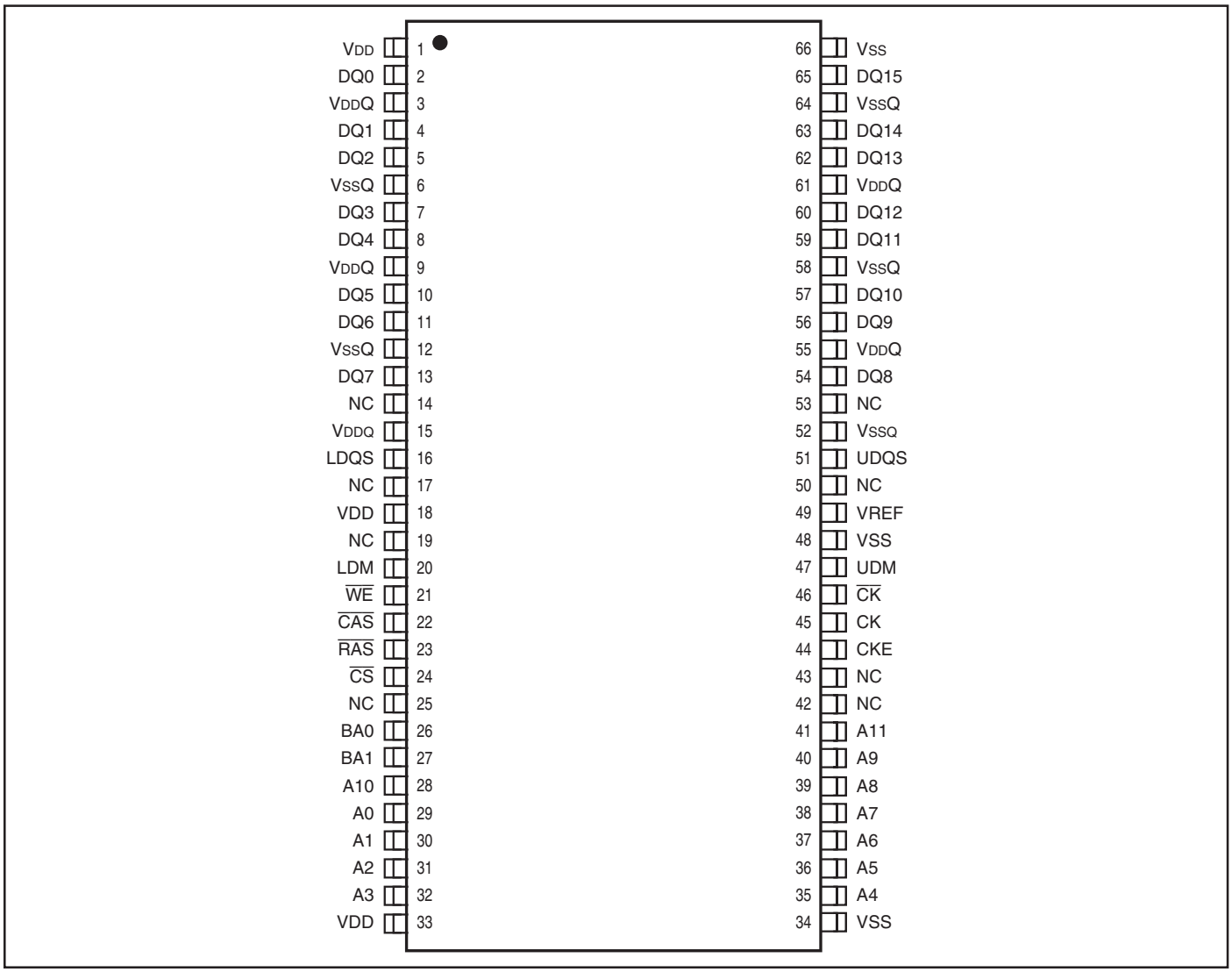
Parameter	-6	Unit
	DDR333	
Clock Cycle Time		
$\overline{CAS}$ Latency = 3	—	ns
$\overline{CAS}$ Latency = 2.5	6	ns
$\overline{CAS}$ Latency = 2	7.5	ns
Clock Frequency		
$\overline{CAS}$ Latency = 3	—	MHz
$\overline{CAS}$ Latency = 2.5	166	MHz
$\overline{CAS}$ Latency = 2	133	MHz

FUNCTIONAL BLOCK DIAGRAM (x16)



PIN CONFIGURATIONS

66 pin TSOP - Type II for x16



PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ15	Data I/O
CK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
LDM, UDM	x16 Input/Output Mask
LDQS, UDQS	Data Strobe
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN FUNCTIONS

Symbol	Type	Function (In Detail)
A0-A11	Input Pin	Address inputs are sampled during several commands. During an Active command, A0-A11 select a row to open. During a Read or Write command, A0-A8 select a starting column for a burst. During a Pre-charge command, A10 determines whether all banks are to be pre-charged, or a single bank. During a Load Mode Register command, the address inputs select an operating mode.
BA0, BA1	Input Pin	Bank Address inputs are used to select a bank during Active, Pre-charge, Read, or Write commands. During a Load Mode Register command, BA0 and BA1 are used to select between the Base or Extended Mode Register
$\overline{CAS}$	Input Pin	$\overline{CAS}$ is Column Access Strobe, which is an input to the device command along with $\overline{RAS}$ and $\overline{WE}$. See "Command Truth Table" for details.
CKE	Input Pin	Clock Enable: CKE High activates and CKE Low de-activates internal clock signals and input/output buffers. When CKE goes Low, it can allow Self Refresh, Pre-charge Power Down, and Active Power Down. CKE must be High during entire Read and Write accesses. Input buffers except CK, $\overline{CK}$, and CKE are disabled during Power Down. CKE uses an SSTL 2 input, but will detect a LVCMOS Low level after VDD is applied.
CK, $\overline{CK}$	Input Pin	All address and command inputs are sampled on the rising edge of the clock input CK and the falling edge of the differential clock input $\overline{CK}$. Output data is referenced from the crossings of CK and $\overline{CK}$.
$\overline{CS}$	Input Pin	The Chip Select input enables the Command Decoding block of the device. When $\overline{CS}$ is disabled, a NOP occurs. See "Command Truth Table" for details. Multiple DDR SDRAM devices can be managed with $\overline{CS}$.
LDM, UDM	Input Pin	These are the Data Mask inputs. During a Write operation, the Data Mask input allows masking of the data bus. DM is sampled on each edge of DQS. There are two Data Mask input pins for the x16 DDR SDRAM. Each input applies to DQ0-DQ7, or DQ8-DQ15.
LDQS, UDQS	Input/Output Pin	These are the Data Strobe inputs. The Data Strobe is used for data capture. During a Read operation, the DQS output signal from the device is edge-aligned with valid data on the data bus. During a Write operation, the DQS input should be issued to the DDR SDRAM device when the input values on DQ inputs are stable. There are two Data Strobe pins for the x16 DDR SDRAM. Each of the two Data Strobe pins applies to DQ0-DQ7, or DQ8-DQ15.
DQ0-DQ15	Input/Output Pin	The pins DQ0 to DQ15 represent the data bus. For Write operations, the data bus is sampled on Data Strobe. For Read operations, the data bus is sampled on the crossings of CK and $\overline{CK}$.
NC	—	No Connect: This pin should be left floating. These pins could be used for 256Mbit or higher density DDR SDRAM.
$\overline{RAS}$	Input Pin	$\overline{RAS}$ is Row Access Strobe, which is an input to the device command along with $\overline{CAS}$ and $\overline{WE}$. See "Command Truth Table" for details.
$\overline{WE}$	Input Pin	$\overline{WE}$ is Write Enable, which is an input to the device command along with $\overline{RAS}$ and $\overline{CAS}$. See "Command Truth Table" for details.
VDDQ	Power Supply Pin	VDDQ is the output buffer power supply.
VDD	Power Supply Pin	VDD is the device power supply.
VREF	Power Supply Pin	VREF is the reference voltage for SSTL 2.
VSSQ	Power Supply Pin	VSSQ is the output buffer ground.
VSS	Power Supply Pin	VSS is the device ground.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
$V_{DD\,MAX}$	Maximum Supply Voltage		–1.0 to +3.6	V
V_{DDQMAX}	Maximum Supply Voltage for Output Buffer		–1.0 to +3.6	V
V_{IN}, V_{REF}	Input Voltage, Reference Voltage		–1.0 to +3.6	V
$P_{D\,MAX}$	Allowable Power Dissipation		1	W
I_{CS}	Output Shorted Current		50	mA
T_{OPR}	Operating Temperature	Com.	0 to +70	°C
T_{STG}	Storage Temperature		–55 to +125	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to Vss.

RECOMMENDED DC OPERATING CONDITIONS (SSTL_2 Input/Output, T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min	Typ.	Max	Unit
V_{DD}	Supply Voltage		2.3	2.5	2.7	V
V_{DDQ}(1)	I/O Supply Voltage		2.3	2.5	2.7	V
V_{TT}	I/O Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH}(2)	Input High Voltage		V_{REF} + 0.15	—	V_{DDQ} + 0.3	V
V_{IL}(3)	Input Low Voltage		- 0.3	—	V_{REF} - 0.15	V
V_{REF}	I/O Reference Voltage		0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V
V_{IN}(DC)(4)	Input Voltage Level for CK and $\overline{CK}$		-0.3	—	V_{DDQ} + 0.3	V
V_{IX}(DC)	Crossing Point Voltage Level for CK and $\overline{CK}$		0.5 x V_{DDQ} - 0.2	0.5 x V_{DDQ}	0.5 x V_{DDQ} + 0.2	V
V_{ID}(DC)(5,6)	Input Differential Voltage Level for CK and $\overline{CK}$		0.36	—	V_{DDQ} + 0.6	V
I_{IL}	Input Leakage Current	0 ≤ V_{IN} ≤ V_{DD}, with all inputs at V_{SS}, except tested input	-2	—	2	µA
I_{OL}	Output Leakage Current	Output disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	-5	—	5	µA
V_{OH}	Output High Voltage Level	I_{OH} = -15.2mA	V_{TT} + 0.76	—	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = +15.2mA	—	—	V_{REF} - 0.76	V

Note:
1. V_{DDQ} must always be less than or equal to V_{DD}.
2. V_{IH} is allowed to exceed V_{DD} up to 3.6V for the period shorter than or equal to 5ns.
3. V_{IL} is allowed to drop to -1.0V for the period shorter than or equal to 5ns.
4. V_{IN}(DC) specifies the allowable DC execution of each differential input.
5. V_{ID}(DC) specifies the input differential voltage required for switching.
6. V_{IH} for CK or $\overline{CK}$ > V_{REF} + 0.18V; V_{IL} for CK or $\overline{CK}$ < V_{REF} - 0.18V.

CAPACITANCE CHARACTERISTICS (At T_A = 0 to +25°C, V_{DD} = V_{DDQ} = 2.5V, f = 100 MHz)

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Input Capacitance: CK and $\overline{CK}$	2	3	pF
C_{IN2}	Input Capacitance: All other input pins	2	3	pF
C_{IN3}	Data Mask Input/Output Capacitance: LDM/UDM	3.8	4.8	pF
C_{OUT}	Data Input/Output Capacitance: DQs and LDQS/UDQS	3.8	4.8	pF

DC ELECTRICAL CHARACTERISTICS (1,2,3,4,5) (V_{DD} = 2.5V +/- 0.2V, T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition		Unit
I_{DD0}	Operating Current	One bank operation; Active-Precharge; DQ, DM and DQS inputs change once per clock cycle; Address and Control inputs change once per two clock cycles; tRC = tRC (min)	110	mA
I_{DD1}	Operating Current	One bank operation; Active-Read-Precharge; BL = 4; CL = 2.5; Address and Control inputs change once per clock cycle; tRCDRD = 4 x tCK; tRC = tRC (min); IOUT = 0mA;	140	mA
I_{DD2P}	Precharge Power-Down Standby Current	All banks Idle; CKE ≤ V_{IL}	3	mA
I_{DD2F}	Floating Idle Standby Current	CKE ≥ V_{IH}; $\overline{CS}$ ≥ V_{IH}; DQ, DQS, DM = V_{REF}	35	mA
I_{DD2Q}	Quiet Idle Standby Current	All banks idle; Address and control inputs change once per clock cycle; CKE = High; $\overline{CS}$ = High (Deselect); VIN = VREF for DQ, DQS, and DM; tCK = tCK (min)	30	mA
I_{DD3P}	Active Power-Down Standby Current	One bank Active; CKE = Low; tCK = tCK (min)	20	mA
I_{DD3N}	Active Standby Current	One bank Active; $\overline{CS}$ = High; CKE = High; Address and Control inputs change once per clock cycle; DQ, DQS, and DM change twice per clock cycle; tRC = tRC (max);	55	mA
I_{DD4R}	Operating Current Burst Read	One bank Active; CKE ≧ V_{IH}; BL = 2; Address and Control inputs change once per clock cycle; tCK = tCK (min); IOUT = 0mA; CL = 2.5	205	mA
I_{DD4W}	Operating Current Burst Write	One bank Active; BL = 2; Address and Control inputs change once per clock cycle; DQ, DQS, DM change twice per clock cycle; CKE ≥ V_{IH}; CL = 2.5	205	mA
I_{DD5}	Auto Refresh Current	tRC = tRFC (min); Input ≤ V_{IL} or ≥ V_{IH}	200	mA
I_{DD6}	Self Refresh Current	Input ≥ V_{DD}-0.2V; Input ≤ 0.2V	3	mA
I_{DD7}	Operating Current	Four bank interleaved Reads with Auto Precharge; BL = 4; Address and Controls inputs change per Read, Write, or Active command; one bank with tRC = tRC (min)	350	mA

Notes:
1. Operating outside the "Absolute Maximum Ratings" may lead to temporary or permanent device failure.
2. Power up sequence describe in "Initialization" section.
3. All voltages are referenced to V_{SS}.
4. I_{DD} tested without DQ pins connected.
5. I_{DD} values tested with t_{CK} = t_{CK} (min).

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5V +/- 0.2V, T_A = 0°C to +70°C)

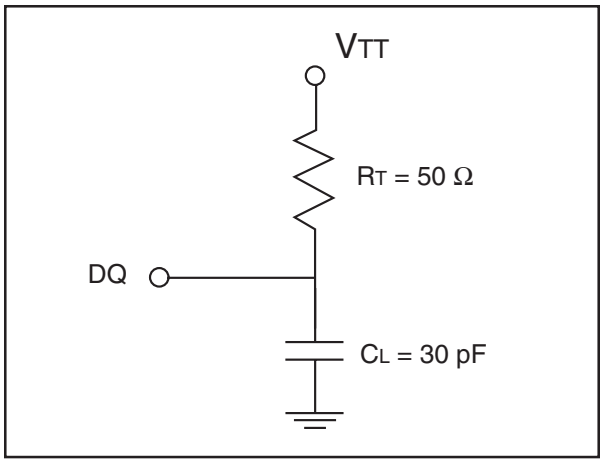
			-6 (2.5-3-3)		
Symbol	**Parameter**	**Test Condition**	**Min.**	**Max.**	**Unit**
t_{CK}	Clock Cycle Time	CL = 2	7.5	12	ns
		CL = 2.5	6	12	
t_{CH}	Clock High Level Width		0.45	0.55	t_{CK}
t_{CL}	Clock Low Level Width		0.45	0.55	t_{CK}
t_{HP}	Clock Half Period		t_{CH} or t_{CL}	—	ns
t_{AC}	Output Access Time from CK, $\overline{CK}$		-0.7	0.7	ns
t_{DQSCK}	DQS-Out Access Time from CK, $\overline{CK}$		-0.6	0.6	ns
t_{DQSQ}	DQS-DQ Skew		—	0.45	ns
t_{QH}	Output DQS Valid Window		t_{HP} - t_{QHS}	—	ns
t_{QHS}	Data Hold Skew factor		—	0.55	ns
t_{HZ}	Data Out High Impedance time from CK, $\overline{CK}$		-0.7	0.7	ns
t_{LZ}	Data Out Low Impedance time from CK, $\overline{CK}$		-0.7	0.7	ns
t_{RPRE}	Read Preamble		0.9	1.1	t_{CK}
t_{RPST}	Read Postamble		0.4	0.6	t_{CK}
t_{DQSS}	CK to Valid DQS-In		0.75	1.25	t_{CK}
t_{DSS}	DQS falling edge to CK setup time		0.2	—	t_{CK}
t_{DSH}	DQS falling edge hold time from CK		0.2	—	t_{CK}
t_{WPRES}	Write Preamble Setup Time		0	—	ns
t_{WPRE}	Write Preamble		0.25	—	ns
t_{WPST}	Write Postamble		0.4	0.6	t_{CK}
t_{DQSH}	DQS-In High Level Pulse Width		0.35	—	t_{CK}
t_{DQSL}	DQS-In Low Level Pulse Width		0.35	—	t_{CK}
t_{IS}	Address and Control Input Setup Time		0.75	—	ns
t_{IH}	Address and Control Input Hold Time		0.75	—	ns
t_{IPW}	Address and Control Input Pulse Width		2.2	—	ns
t_{DS}	DQ and DM Setup Time to DQS		0.45	—	ns
t_{DH}	DQ and DM Hold Time to DQS		0.45	—	ns
t_{RC}	Active to Active/ Auto Refresh Command Period		60	—	ns
t_{RFC}	Auto Refresh to Active/ Auto Refresh Command Period		72	—	ns
t_{RAS}	Active to Precharge Command Period		42	120K	ns
t_{RCDRD}	$\overline{RAS}$ to $\overline{CAS}$ Delay in Read		18	—	ns
t_{RCDWR}	$\overline{RAS}$ to $\overline{CAS}$ Delay in Write		18	—	ns
t_{RP}	Row Pre-charge Time		18	—	ns
t_{RAP}	Active to Auto Precharge delay		t_{RCD} min.	—	ns
t_{RRD}	Row Active to Row Active Delay		12	—	ns
t_{WR}	Write Recovery Time		15	—	ns
t_{MRD}	Mode Register Load Delay		2	—	t_{CK}
t_{DAL}	Auto Pre-charge Write Recovery + Pre-charge		$t_{WR}/t_{CK}+t_{RP}/t_{CK}$	—	t_{CK}
t_{REF}	Refresh Interval Time		—	15.6	µs

Notes:
1. Operating outside the “Absolute Maximum Ratings” may lead to temporary or permanent device failure.
2. Power up sequence describe in “Initialization” section.
3. All voltages are referenced to Vss.

Notes:
1. All AC parameters measuremed with the following test conditions.
2. This parameter defines the signal transition delay from the crossing point of CK and $\overline{CK}$. The signal transition is defined to occur when the signal level crosses VTT.
3. The timing reference level is VTT.
4. Output valid window is defined to be the period between two successive transition of data out or DQS (read) signals. The signal transition is defined to occur when the signal level crosses VTT.
5. t_{HZ} is defined as the data output transition delay from Low-Z to High-Z at the end of a read burst operation. The timing reference is the crossing point of CK and $\overline{CK}$. This parameter is not referred to a specific voltage level, but when the device output stops driving.
6. t_{LZ} is defined as the data output transition delay from High-Z to Low-Z at the beginning of read operation. This parameter is referring to a specific voltage level, but when the device output begins driving.
7. Input valid windows is defined to be the period between two successive transition of data input or DQS (write) signals. The signal transition is defined to occur when the signal level crosses V_{REF}.
8. The timing reference level is V_{REF}.
9. The transition from Low-Z to High-Z is defined to occur when the device output stops driving. There is no specific reference voltage to judge this transition.
10. t_{CK} (max.) is determined by the locking range of the DLL. Beyond this lock range, the DLL operation is assured.
11. $t_{CK} = t_{CK}$ (min) when these parameters are measured. Otherwise, absolute minimum values of these values are 10% of t_{CK}.
12. VDD is assumed to be 2.5V ± 0.2V. V_{DD} power supply variation per cycle expected to be less than 0.4V per 400 cycles.
13. $t_{DAL} = (t_{WR}/t_{CK})+(t_{RP}/t_{CK})$. For each of the add-ins, if not an integer already, round up to the nearest integer.

AC TEST CONDITIONS

Output Load



AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Input High Voltage	V_{IH} (AC)	V_{REF} + 0.31	V
Input Low Voltage	V_{IL} (AC)	V_{REF} - 0.31	V
Input Signal Slew Rate	SLEW	1	V/ns
Input Timing Reference Level	V_{REF}	$V_{DDQ}/2$	V
Termination Voltage	V_{TT}	V_{REF}	V
Input Differential Voltage (CK and $\overline{CK}$)	V_{ID} (AC)	0.62	V
Input Differential Crossing Voltage	V_{IX} (AC)	V_{REF}	V

OPERATING FREQUENCY / LATENCY RELATIONSHIPS (t_{CK} = 6ns, CL = 2.5)

SYMBOL	PARAMETER		UNITS
t_{WPD}	Write to Pre-charge command delay (same bank)	4 + BL/2	Cycle
t_{RPD}	Read to Pre-charge command delay (same bank)	BL/2	Cycle
t_{WRD}	Write to Read command delay (to input all data)	2 + BL/2	Cycle
t_{BSTW}	Burst Stop command to Write command delay	3	Cycle
t_{BSTZ}	Burst Stop command to DQ High-Z	2.5	Cycle
t_{RWD}	Read command to Write command delay (to output all data)	3 + BL/2	Cycle
t_{HZP}	Pre-charge command to High-Z	2.5	Cycle
t_{WCD}	Write command to data in latency	1	Cycle
t_{WR}	Write Recovery	3	Cycle
t_{DMD}	DM to Data-In latency	0	Cycle
t_{MRD}	Mode Register Set command cycle time	2	Cycle
t_{SNR}	Self Refresh Exit to non-read command	12	Cycle
t_{SRD}	Self Refresh Exit to Read command	200	Cycle
t_{PDEN}	Power Down Entry	1	Cycle
t_{PDEX}	Power Down Exit to command input	1	Cycle

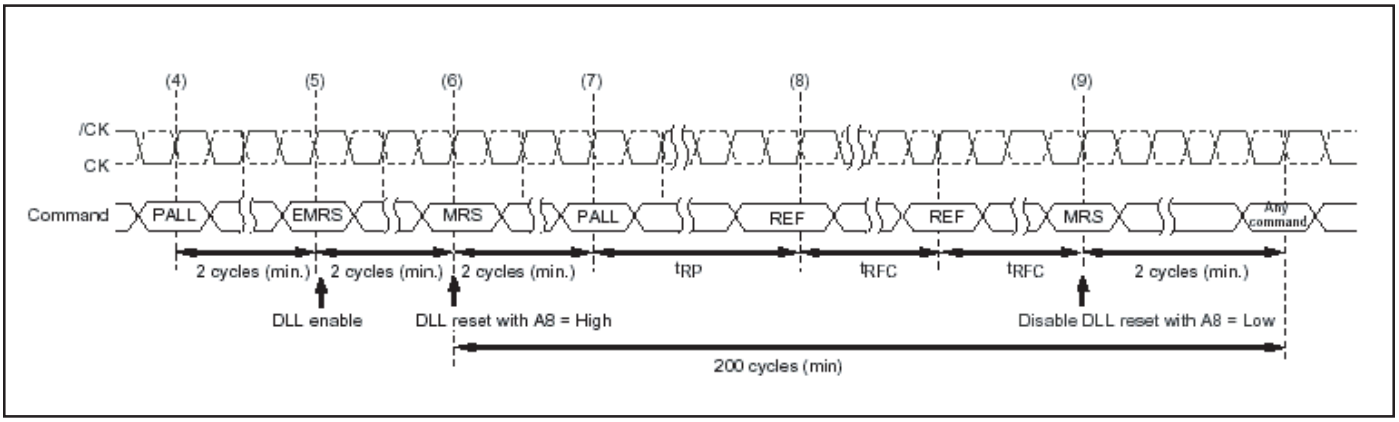
FUNCTIONAL DESCRIPTION

The 128Mbit DDR SDRAM is a high-speed CMOS device with four banks that operate at 2.5V. Each 32Mbit bank is organized as 4,096 rows of 512 columns for the x16 option. Pre-fetch architecture allows Read and Write accesses to be double-data rate and burst oriented. Accesses start at a selected column location and continue every half-clock cycle for a programmed number of times. The Read or Write operation begins with an Active command to transmit the selected bank and row (A0-A11 bits are sampled). This is followed by a Read or Write command to sample the address bits again to determine the first column to access. When access to the memory is not necessary, the device can be put into a Power Down mode in which current consumption is minimized. Prior to normal operation, the device must be initialized in a defined procedure to function properly. The following sections describe the steps of initialization, the mode register definitions, command descriptions, and device operation.

INITIALIZATION

The DDR SDRAM must be powered-on and initialized in a series of defined steps for proper operation. First, power is applied to VDD, and then to VDDQ. After these have reached stable values, VREF and V_{TT} are ramped up. If this sequence is not followed, latch-up could occur and cause damage to the device. The input CKE must be asserted and held to a LVCMOS Low level during this time to prevent unwanted commands from being executed. The outputs I/O and DQS remain in high impedance until driven during a normal operation. Once VDD, VDDQ, V_{TT}, VREF, and CKE are stable values, the clock inputs can begin to be applied. For a time period of at least 200µs, valid CK and $\overline{CK}$ cycles must be applied prior to any command being issued to the device. CKE needs to then be raised to SSTL 2 logic High and issue a NOP or Deselect command to initialize the internal logic of the DRAM. Next, a Pre-charge All command is given to the device, followed by a NOP/Deselect command on each clock cycle for at least tRP. The Load Extended Mode Register should be issued to enable DLL, followed by another series of NOP/Deselect commands for at least tMRD. After this time, the Load Mode Register command should be issued to reset the DLL, again followed by a series of NOP or Deselect commands for at least tMRD. (Note: whenever the DLL is reset, 200 clock cycles must occur prior to any Read command.) The Pre-charge command is then issued, with NOP/Deselect commands for at least tRP. Next, two Auto-Refresh commands are issued, each followed by NOP/Deselect commands for at least tRFC. At this point, the JEDEC specification recommends that a DDR SDRAM receive another Load Mode Register command to clear the DLL, with NOP/Deselect commands for at least tMRD. The device is now ready to receive a valid command for normal operation.

POWER-UP SEQUENCE AFTER CKE GOES HIGH



MODE REGISTER DEFINITION

The mode register allows configuration of the operating mode of the DDR SDRAM. This register is loaded as a step in the normal initialization of the device. The Load Mode Register command samples the values on inputs A0-A11, BA0 (Low) and BA1 (Low) and stores them as register values M0-M13. The values in the register determine the burst length, burst type, CAS latency timing, and DLL Reset/Clear. It should be noted that some bit values are reserved and should not be loaded into the register. The data in the mode register is retained until it is re-loaded or the DDR SDRAM loses its power (except for bit M8, which is cleared automatically). The register can be loaded only if all banks are idle. After the Load Mode Register command, a minimum time of tMRD must pass before the subsequent command is issued.

CAS LATENCY

After a Read command is issued to the device, a latency of several clock cycles is necessary prior to the validity of data on the data bus. Also known as CAS Latency (CL), the value can be configured as 2 or 2.5, via the bits M4-M6 loaded into the register. The maximum frequency allowed with the CAS setting is defined in AC Electrical Characteristics. If CL values are not defined, the device may not function properly.

MODE REGISTER DEFINITION

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
														Address Bus (Ax)
														Mode Register (Mx)

Burst Length

M2	M1	M0	M3=0	M3=1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

Burst Type

M3	Type
0	Sequential
1	Interleaved

Latency Mode

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

Operating Mode

M8	M7	M6-M0	Mode
0	0	Defined	Standard Operation
1	0	Defined	Standard Operation w/DLL Reset
—	—	—	All Other States Reserved

Operating Mode

M13	M12	M11	M10	M9	Mode
0	0	0	0	0	Standard operation
—	—	—	—	—	All Other States Reserved

BURST LENGTH

The highest access throughput of this device can be achieved by using a burst of either Read or Write accesses. The number of accesses in each burst would be pre-configured to be 2, 4, or 8, as shown in Mode Register Definition (bits M0-M2). When a Read or Write command is given to the device, the address bits A0-A8 (x16) select the block of columns and the starting column for the subsequent burst. The accesses in this burst can only reference the selected block, and may wrap-around if a boundary is reached. The Burst Definition table indicates the relationship between the least significant address bits and the starting column. The most significant address bits can select any unique block of columns in the currently activated row.

BURST TYPE

Bursts can be made in either of two types: sequential or interleaved. The burst type is programmed during a Load Mode Register command (bit M3). During a Read or Write burst, the order of accesses is determined by burst length, starting column, and burst type, as indicated in the Burst Definition table.

DLL RESET/CLEAR

To cause a DLL reset, the bit M8 is set to 1 in the Load Mode Register command. When the DLL is reset, 200 clock cycles are required to occur prior to any Read operation. To clear the DLL for normal operation, the bit M8 is set to 0. This device does not require it, but JEDEC specifications require that any time that the DLL is reset, it later be cleared prior for normal operation.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses in a Burst	
				Sequential	Interleaved
	A2	A1	A0		
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

EXTENDED MODE REGISTER DEFINITION

The Extended Mode Register is a second register to enable additional functions of the DDR SDRAM. This register is loaded as a step in the normal initialization of the device. The Load Extended Mode Register command samples the values on inputs A0-A11, BA0 (High) and BA1 (Low) and stores them as register values E0-E13. The additional functions are DLL enable/disable and output drive strength. Similarly to the Load Mode Register, the Load Extended Mode Register has reserved bit values, a bank idle pre-requisite, and a tMRD time requirement. The data in the mode register is retained until it is reloaded or the device loses its power.

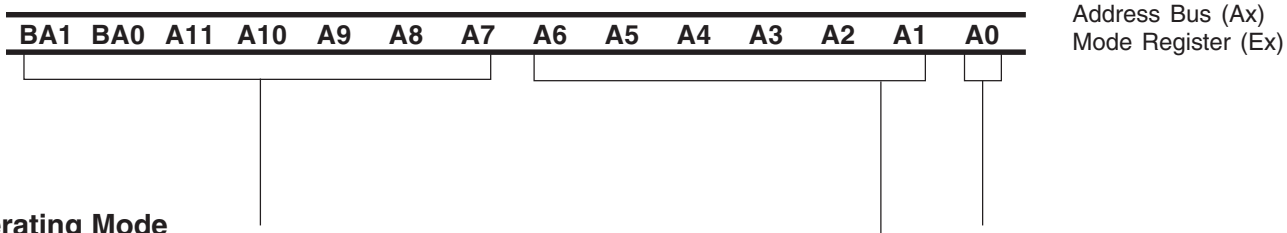
DLL Enable/Disable

When the Load Extended Mode Register command is issued, DLL should be enabled (E0 = 0). Normal operation of the device requires this, but DLL can be disabled for debugging or evaluation, if necessary.

Output Drive Strength

Normal drive strength for the outputs is specified as SSTL 2. However, there is an option for reduced drive strength included.

EXTENDED MODE REGISTER DEFINITION



Operating Mode

E13	E12	E11	E10	E9	E8	E7	Mode
0	1	0	0	0	0	0	Standard Operation
—	—	—	—	—	—	—	All Other States Reserved

DLL

E0	Status
0	Enable
1	Disable

Drive Strength

E6	E5	E4	E3	E2	E1	Type
0	0	0	0	0	0	Full Strength
0	0	0	0	0	1	Weak
—	—	—	—	—	—	All Other States Reserved

COMMANDS

All commands described in this section should be issued only when the initialization sequence is obeyed.

Deselect (DESL)

This feature blocks unwanted commands from being executed. Chip select ($\overline{CS}$) must be taken High to cause Deselect. Operations that are underway are not affected.

No Operation (NOP)

NOP is a command that prevents new commands from being executed. $\overline{CS}$ must be Low, while $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ must be High to issue NOP. NOP or Deselect commands must be issued during wait states to allow operations that are underway to continue uninterrupted.

Load Mode Register (MRS)

The Base Mode Register is loaded during a step of initialization to configure the DDR SDRAM. Load Mode Register is issued when BA0 and BA1 are Low, and A0-A11 are selected according to the Mode Register Definition.

Load Extended Mode Register (EMRS)

The Extended Mode Register is loaded during a step of initialization to enable the DLL of the device. Load Extended Mode Register is issued when BA0 is High, BA1 is Low, and A0-A11 are selected according to the Extended Mode Register Definition.

Read (READ/READA)

The Read command is used to begin a burst read access. When the command is given to the device, the BA0 and BA1 inputs select the bank, and address bits A0-A8 (x16) select the block of columns and the starting column for the subsequent burst. The crossing of the CK and $\overline{CK}$ signals will cause the output values on the I/O pins to be valid. The Auto Pre-charge function is one option in the Read command. If the Auto Pre-charge is enabled, the currently selected row will be pre-charged following the Read burst. If the function is not enabled, the selected row will remain open for further accesses at the end of the Read burst.

Write (WRIT/WRITA)

The Write command is used to begin a burst write access. When the command is given to the device, the BA0 and BA1 inputs select the bank, and address bits A0-A8 (x16) select the block of columns and the starting column for the subsequent burst. The rising edge on the Data Strobe input(s) will cause the input values on the Data Mask pin(s) and I/O pins to be sampled for the write operation. The Auto Pre-charge function is one option in the Write command. If the Auto Pre-charge is enabled, the currently selected row will be Pre-charged following the Write burst. If the function is not enabled, the selected row will remain open for further accesses at the end of the Write burst.

Pre-charge (PRE/PALL)

A Pre-charge command will de-activate an open row in a bank. The input A10 (x16) is sampled at this time to determine whether Pre-charge is applied to a single bank or all banks. After tRP, the bank has been pre-charged. It is de-activated, and goes into the idle state and must be activated before any Read or Write command can be issued to it. A Pre-charge command is treated as a NOP if either (a) the specified bank is already undergoing Pre-charge, or (b) the specified bank has no open row.

Auto Pre-charge

Auto Pre-charge is a feature that can be enabled as an option in a Read or Write command. If the input value on A10 (x16) is High during a Read or Write command, an automatic Pre-charge will occur just after the memory burst is completed. If the input value on A10 (x16) is Low, no Pre-charge will occur. With Auto Pre-charge, a minimum time of tRP must pass before the next command is issued to the same bank.

Active (ACT)

The Active command opens a row in preparation for a Read or Write burst. The row stays open for accesses until the bank receives a Pre-charge command. Other rows in the bank cannot be opened until the bank is de-activated with a Pre-charge command and another Active command is issued.

Burst Terminate (BST)

The Burst Terminate command truncates the burst of the most recently issued Read command (with Auto Pre-charge disabled). The open row being accessed in the Read burst remains open.

Auto Refresh (REF)

The DDR SDRAM is issued the Auto Refresh command during normal operation to maintain data in the memory array. All the banks must be idle for the command to be executed. The device has 4096 refresh cycles every 64ms.

Self Refresh (SELF)

To issue the Self Refresh command, CKE must be Low. When the DDR SDRAM is in Self Refresh mode, it retains the data contents without external clocking, and ignores other input signals. The DLL is disabled upon entering the Self Refresh mode, and is enabled again upon leaving the mode. To exit Self Refresh, all inputs must be stable prior to CKE going High. Next, a NOP command command must be issued on each clock cycle for at least t_{SNR} to ensure that internal refresh operations are completed. To prepare for a memory access, the DDR SDRAM must receive a DLL reset followed by a NOP command for 200 clock cycles.

DEVICE OPERATION

Bank and Row Activation

An Active command must be issued to the DDR SDRAM to open a bank and row prior to an access. The row will be available for a Read or Write command once a time tRCD has occurred. The Active command is depicted in the figure. As CK goes High, $\overline{CS}$ and $\overline{RAS}$ are Low, while CKE, $\overline{WE}$, and $\overline{CAS}$ are High. Upon issuing the Active command, the values on the address inputs specify the row, and BA0 and BA1 specify the bank. When an Active command is issued for a bank and row, another row in that same bank may be activated after a time tRC. When an Active command is issued for a bank and row, a row in a different bank may be activated after a time tRRD. (Note: to ensure that time requirement tRCD, tRC, or tRRD is met, NOP commands should be issued for a whole number of clock cycles that is greater than the time requirement (ie. tRCD) divided by the clock period.)

Read Operation

A Read command starts a burst from an activated row. The Read command is depicted in the figure. As CK goes High, $\overline{CS}$ and $\overline{CAS}$ are Low, while $\overline{RAS}$, CKE, and $\overline{WE}$ are High. The values on the inputs BA0 and BA1 specify the bank to access, and the address inputs specify the starting column in the open row. If Auto Pre-charge is enabled in the Read command, the open row will be pre-charged after completion of the Read burst. Unless stated otherwise, all timing diagrams for Read operations have disabled Auto Pre-charge.

The Read command causes data to be retrieved and placed in the pipeline. The subsequent command can be NOP, Read, or Terminate Burst. The data from the starting column specified in the Read command appears on I/O pins following a CAS latency of after the Read command. On each CK and $\overline{CK}$ crossing, the data from the next column in the burst sequence is output from the pipeline until the burst is completed (see Read Burst, Non-consecutive Read Burst, and Consecutive Read Burst). There are two cases in which a full Read burst length is not completed. The first is when the data retrieved from a subsequent Read burst interrupts the previous burst (see Random Read Accesses). The second is when a subsequent Burst Terminate command truncates the burst (see Terminating a Read Burst and Read to Write). The Burst Terminate and Read commands obey the same CAS latency timing such that they should be issued x cycles after a previous Read command, where x is the number of pairs of columns to output. By following a desired command sequence, continuous data can be output with either whole Read bursts or truncated Read bursts. Whenever a Read burst finishes and no other commands have been initiated, the I/O returns to High-Z.

If Auto Pre-charge is not enabled in the Read burst, the Pre-charge command can be issued separately following the Read command. The Pre-charge command should be received by the device x cycles after the Read command, where x is the desired number of pairs of columns to output during the Read burst. After the Pre-charge command, it is necessary to wait until both tRAS and tRP have been met before issuing a new command to the same bank.

Data Strobe output is driven synchronously with the output data on the I/O pins. The Low portion of the Data Strobe just prior to the first output data is the Read Pre-amble; and the Low portion coinciding with the last output data is the Read Post-amble. Before any Write command can be executed, any previous Read burst must have been completed normally or truncated by a Burst Terminate command. In the diagram Read to Write, a Burst Terminate command is issued to truncate a Read Burst early, and begin a Write operation. After the Write command, a time tDQSS is required prior to latching the data on the I/O.

Write Operation

A Write command starts a burst from an activated row. The Write command is depicted in the figure. As CK goes High, $\overline{CS}$, $\overline{WE}$, and $\overline{CAS}$ are Low, while CKE and $\overline{RAS}$ are High. The values on the inputs BA0 and BA1 specify the bank to access, and the address inputs specify the starting column in the open row. If Auto Pre-charge is enabled in the Write command, the open row will be pre-charged after completion of the Write burst and time tWR. Unless stated otherwise, all timing diagrams for Write operations have disabled Auto Pre-charge.

The Write command in conjunction with Data Strobe inputs causes data to be latched and placed in the pipeline. The Low portion of the Data Strobe between the Write command and the first rising edge of the strobe is the Write Pre-amble; and the Low portion following the last input data is the Write Post-amble. A minimum time of tDQSS after the Write, the next command can be NOP or Write. The data that is to be written to the starting column specified in the Write command will be latched upon the first rising edge of Data Strobe input(s) LDQS, UDQS (x16) after that Write command. On each Data Strobe transition from Low-to-High or High-to-Low, the input values on the I/O are sampled, and enter pipeline to be written in the pre-determined burst sequence (see Write Burst, Consecutive Write to Write, and Non-consecutive Write to Write). A new Write command can be issued x cycles after a previous Write command, where x is the number of pairs of columns to input. By following a desired command sequence, continuous data can be input with either whole Write bursts or truncated Write bursts. Whenever a Write burst finishes and no other commands have been initiated, the I/O returns to High-Z.

A Write burst may be followed by Read command, with or without truncating the Write burst. To avoid truncating the input data, the timing parameter tWTR should be obeyed before issuing the Read command (see Write to Read, Non-truncated). The period tWTR begins on the first positive clock edge after the last data input has been latched. The Write burst can be truncated deliberately by using the Data Mask feature and a Read command with an earlier timing (see Write to Read, Truncated).

If Auto Pre-charge is not enabled in the Write burst, the Pre-charge command can be issued separately some time following the Write command. The procedure to execute it is similar to the procedure to transition from a Write burst to a Read burst. To avoid truncating the input data, the timing parameter tWR should be obeyed before issuing the Pre-charge command (see Write to Pre-charge, Non-truncated). The period tWR begins on the first positive clock edge after the last data input has been latched. The Write burst can be truncated deliberately by using the Data Mask feature and a Pre-charge command with an earlier timing (see Write to Pre-charge, Truncated). After the Pre-charge command, it is necessary to wait until tRP has been met before issuing a new command to the same bank.

Power Down Operation

When the DDR SDRAM enters Power Down mode, power consumption is greatly reduced. To enter the mode, several conditions must be met. There must be neither a Read operation, nor a Write operation underway in the device at CK positive edge n – 1, with CKE stable High. Prior to CK positive edge n, CKE should go Low. A Power Down mode is entered if the appropriate command is issued as CK n goes High. (If the command at CK n is Auto Refresh, the SDRAM enters Self Refresh mode.) If the command at CK n is NOP or Deselect, the device will enter Pre-charge Power Down mode or Active Power Down mode. While in a Power Down mode, CKE must be stable Low, and CK and $\overline{CK}$ signals maintained, while other inputs are ignored. Pre-charge Power Down mode conserves additional power by freezing the DLL. To exit the Power Down mode, normal voltages and clock frequency are applied. Prior to CK positive edge n, CKE should go High. A NOP or Deselect command at CK n, allows a valid command to be issued at CK positive edge n + 1. (If exiting Self Refresh mode, the DLL is automatically enabled, and the device must be prepared according to the section describing Self Refresh.)

Pre-charge Operation

When this command is issued, either a particular bank, or all four banks will be de-activated after a time period of tRP. The bank(s) will be available for a row access until that time has occurred. The Pre-charge command is depicted in the figure. As CK goes High, $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ are Low, while CKE and $\overline{CAS}$ are High. The values on the address inputs are Don't Care, except for the input A10 (x16), which determines whether a single bank is selected for Pre-charge, or all four banks. If A10 is Low, the inputs BA0 and BA1 select the single bank; however, if A10 is High, BA0 and BA1 are Don't Care. Once any bank has been pre-charged, it becomes idle. Before any row can have a Read or Write access, it must be activated.

COMMAND TRUTH TABLE

DDR SDRAM recognize the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins. All other combinations than those in the table below are illegal.

		CKE									
Command	**Symbol**	**n – 1**	**n**	**$\overline{CS}$**	**$\overline{RAS}$**	**$\overline{CAS}$**	**$\overline{WE}$**	**BA1**	**BA0**	**AP**	**Address**
Ignore command	DESL	H	H	H	x	x	x	x	x	x	x
No operation	NOP	H	H	L	H	H	H	x	x	x	x
Burst stop in read command	BST	H	H	L	H	H	L	x	x	x	x
Column address and read command	READ	H	H	L	H	L	H	V	V	L	V
Read with auto-precharge	READA	H	H	L	H	L	H	V	V	H	V
Column address and write command	WRIT	H	H	L	H	L	L	V	V	L	V
Write with auto-precharge	WRITA	H	H	L	H	L	L	V	V	H	V
Row address strobe and bank active	ACT	H	H	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	H	L	L	H	L	V	V	L	x
Precharge all bank	PALL	H	H	L	L	H	L	x	x	H	x
Refresh	REF	H	H	L	L	L	H	x	x	x	x
	SELF	H	L	L	L	L	H	x	x	x	x
Mode register set	MRS	H	H	L	L	L	L	L	L	L	V
	EMRS	H	H	L	L	L	L	L	H	L	V

Remark: H: VIH. L: VIL. ×: VIH or VIL V: Valid address input
Note: The CKE level must be kept for 1 CK cycle at least.

CKE TRUTH TABLE

		CKE							
Current state	**Command**	**n – 1**	**n**	**$\overline{CS}$**	**$\overline{RAS}$**	**$\overline{CAS}$**	**$\overline{WE}$**	**Address**	**Notes**
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	x	2
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	x	2
Idle	Power down entry (PDEN)	H	L	L	H	H	H	x	
		H	L	H	x	x	x	x	
Self refresh	Self refresh exit (SELFX)	L	H	L	H	H	H	x	
		L	H	H	x	x	x	x	
Power down	Power down exit (PDEX)	L	H	L	H	H	H	x	
		L	H	H	x	x	x	x	

Remark: H: VIH. L: VIL. ×: VIH or VIL.

Notes:
1. All the banks must be in IDLE before executing this command.
2. The CKE level must be kept for 1 CK cycle at least.

Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR SDRAM.

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Precharging*1	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*11	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*11	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*11	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	×	×		ILLEGAL	—
Idle*2	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*11	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*11	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*11	—
	L	L	H	H	BA, RA	ACT	Activating	Active
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	H	×	REF, SELF	Refresh/ Self refresh*12	Idle/ Self refresh
	L	L	L	L	MODE	MRS	Mode register set*12	Idle
Refresh (auto-refresh)*3	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	×	×		ILLEGAL	—
	L	L	×	×	×		ILLEGAL	—
Activating*4	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL*11	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*11	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*11	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*11	—
	L	L	L	×	×		ILLEGAL	—
Active*5	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	Active
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation	Read/READA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting write operation	Write recovering/ precharging
	L	L	H	H	BA, RA	ACT	ILLEGAL*11	—
	L	L	H	L	BA, A10	PRE, PALL	Pre-charge	Idle
	L	L	L	×	×		ILLEGAL	—

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Read*[6]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	BST	Active
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst read operation to start new read	Active
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[13]	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting burst read operation to start pre-charge	Precharging
	L	L	L	×	×		ILLEGAL	—
Read with auto-pre-charge*[7]	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[14]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[14]	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11, 14]	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[11, 14]	—
	L	L	L	×	×		ILLEGAL	—
Write*[8]	H	×	×	×	×	DESL	NOP	Write recovering
	L	H	H	H	×	NOP	NOP	Write recovering
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst write operation to start read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Interrupting burst write operation to start new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting write operation to start pre-charge.	Idle
	L	L	L	×	×		ILLEGAL	—
Write recovering*[9]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]	—
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL*[11]	—
	L	L	L	×	×		ILLEGAL	—

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Write with auto-pre-charge*10	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*14	—
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL*14	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*11, 14	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*11, 14	—
	L	L	L	×	×		ILLEGAL	—

Remark: H: VIH. L: VIL. ×: VIH or VIL

Notes: 1. The DDR SDRAM is in "Precharging" state for tRP after precharge command is issued.
2. The DDR SDRAM reaches "IDLE" state tRP after precharge command is issued.
3. The DDR SDRAM is in "Refresh" state for tRFC after auto-refresh command is issued.
4. The DDR SDRAM is in "Activating" state for tRCD after ACT command is issued.
5. The DDR SDRAM is in "Active" state after "Activating" is completed.
6. The DDR SDRAM is in "READ" state until burst data have been output and DQ output circuits are turned off.
7. The DDR SDRAM is in "READ with auto-precharge" from READA command until burst data has been output and DQ output circuits are turned off.
8. The DDR SDRAM is in "WRITE" state from WRIT command to the last burst data are input.
9. The DDR SDRAM is in "Write recovering" for tWR after the last data are input.
10. The DDR SDRAM is in "Write with auto-precharge" until tWR after the last data has been input.
11. This command may be issued for other banks, depending on the state of the banks.
12. All banks must be in "IDLE".
13. Before executing a write command to stop the preceding burst read operation, BST command must be issued.
14. The DDR SDRAM supports the concurrent auto-precharge feature, a read with auto-precharge enabled,or a write with auto-precharge enabled, may be followed by any column command to other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply. (E.g. Conflict between READ data and WRITE data must be avoided.)

The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank, is summarized below.

From command	To command (different bank, non-interrupting command)	Minimum delay (Concurrent AP supported)	Units
Read w/AP	Read or Read w/AP	BL/2	tCK
	Write or Write w/AP	CL(rounded up)+ (BL/2)	tCK
	Precharge or Activate	1	tCK
Write w/AP	Read or Read w/AP	1 + (BL/2) + tWTR	tCK
	Write or Write w/AP	BL/2	tCK
	Precharge or Activate	1	tCK

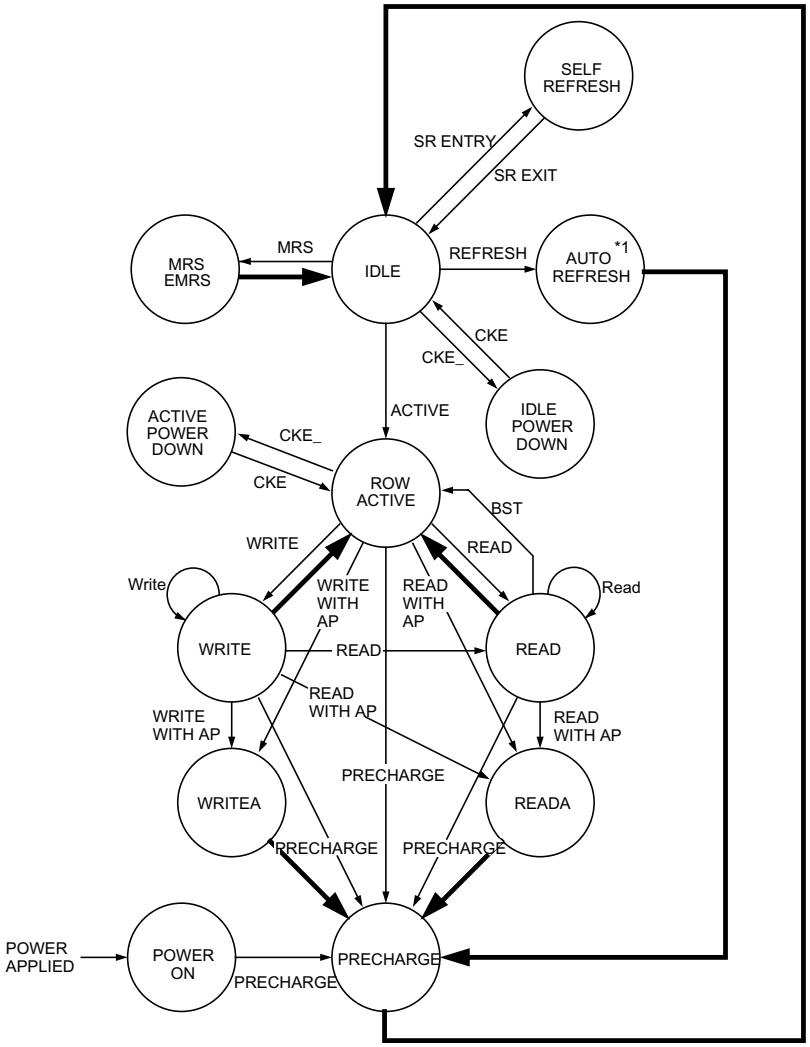
Command Truth Table for CKE

Current State	CKE								
	n – 1	n	/CS	/RAS	/CAS	/WE	Address	Operation	Notes
Self refresh	H	×	×	×	×	×	×	INVALID, CK (n-1) would exit self refresh	
	L	H	H	×	×	×	×	Self refresh recovery	
	L	H	L	H	H	×	×	Self refresh recovery	
	L	H	L	H	L	×	×	ILLEGAL	
	L	H	L	L	×	×	×	ILLEGAL	
	L	L	×	×	×	×	×	Maintain self refresh	
Self refresh recovery	H	H	H	×	×	×	×	Idle after tRC	
	H	H	L	H	H	×	×	Idle after tRC	
	H	H	L	H	L	×	×	ILLEGAL	
	H	H	L	L	×	×	×	ILLEGAL	
	H	L	H	×	×	×	×	ILLEGAL	
	H	L	L	H	H	×	×	ILLEGAL	
	H	L	L	H	L	×	×	ILLEGAL	
	H	L	L	L	×	×	×	ILLEGAL	
Power down	H	×	×	×	×	×		INVALID, CK (n – 1) would exit power down	
	L	H	H	×	×	×	×	EXIT power down → Idle	
	L	H	L	H	H	H	×		
	L	L	×	×	×	×	×	Maintain power down mode	
All banks idle	H	H	H	×	×	×		Refer to operations in Function Truth Table	
	H	H	L	H	×	×		Refer to operations in Function Truth Table	
	H	H	L	L	H	×		Refer to operations in Function Truth Table	
	H	H	L	L	L	H	×	CBR (auto) refresh	
	H	H	L	L	L	L	OPCODE	Refer to operations in Function Truth Table	
	H	L	H	×	×	×		Refer to operations in Function Truth Table	
	H	L	L	H	×	×		Refer to operations in Function Truth Table	
	H	L	L	L	H	×		Refer to operations in Function Truth Table	
	H	L	L	L	L	H	×	Self refresh	1
	H	L	L	L	L	L	OPCODE	Refer to operations in Function Truth Table	
	L	×	×	×	×	×	×	Power down	1
Row active	H	×	×	×	×	×	×	Refer to operations in Function Truth Table	
	L	×	×	×	×	×	×	Power down	1

Remark: H: VIH. L: VIL. ×: VIH or VIL

Note: Self refresh can be entered only from the all banks idle state. Power down can be entered only from all banks idle or row active state.

Simplified State Diagram



Automatic transition after completion of command.

Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

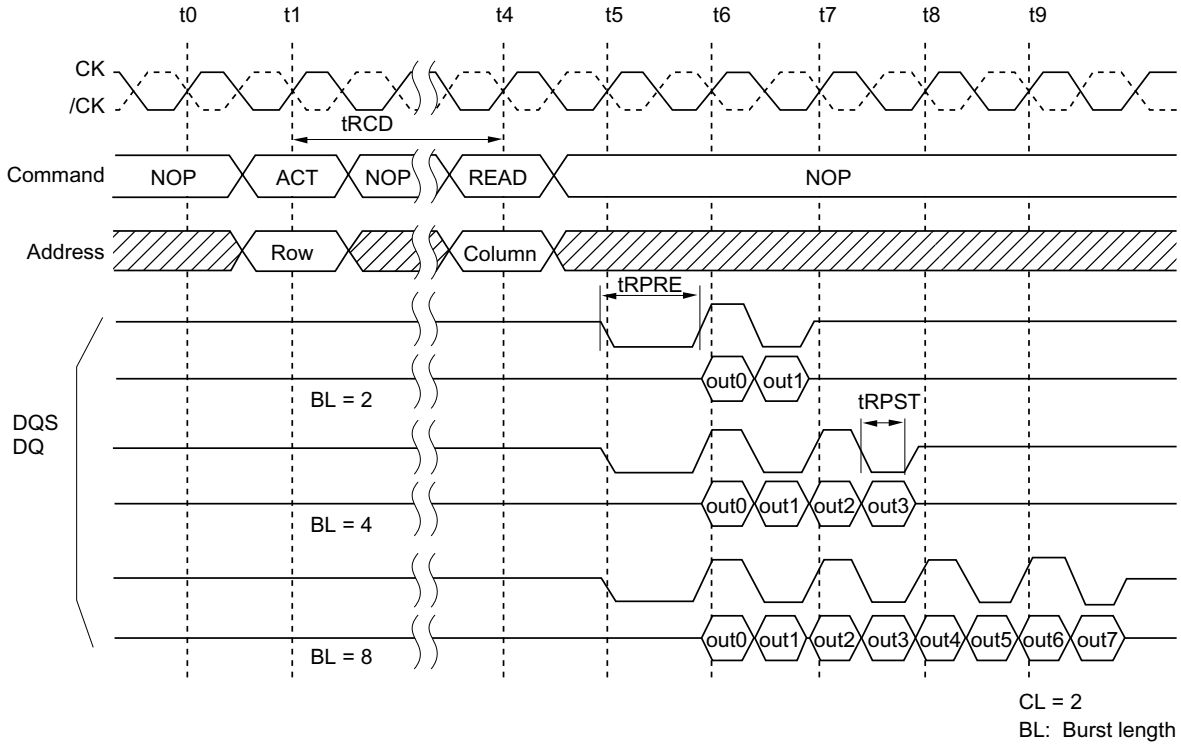
Read/Write Operations

Bank active

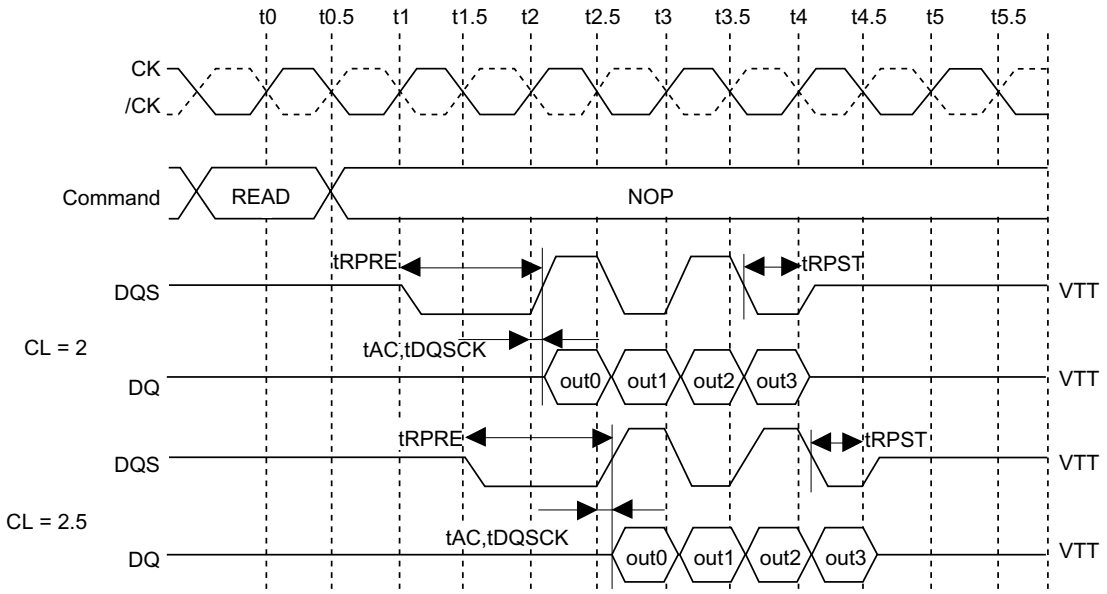
A read or a write operation begins with the bank active command [ACT]. The bank active command determines a bank address and a row address. For the bank and the row, a read or a write command can be issued tRCD after the ACT is issued.

Read operation

The burst length (BL), the /CAS latency (CL) and the burst type (BT) of the mode register are referred when a read command is issued. The burst length (BL) determines the length of a sequential output data by the read command that can be set to 2, 4, or 8. The starting address of the burst read is defined by the column address, the bank select address which are loaded via the A0 to A11 and BA0, BA1 pins in the cycle when the read command is issued. The data output timing are characterized by CL and tAC. The read burst start CL • tCK + tAC (ns) after the clock rising edge where the read command are latched. The DDR SDRAM output the data strobe through DQS simultaneously with data. tRPRE prior to the first rising edge of the data strobe, the DQS are driven Low from VTT level. This low period of DQS is referred as read preamble. The burst data are output coincidentally at both the rising and falling edge of the data strobe. The DQ pins become High-Z in the next cycle after the burst read operation completed. tRPST from the last falling edge of the data strobe, the DQS pins become High-Z. This low period of DQS is referred as read postamble.



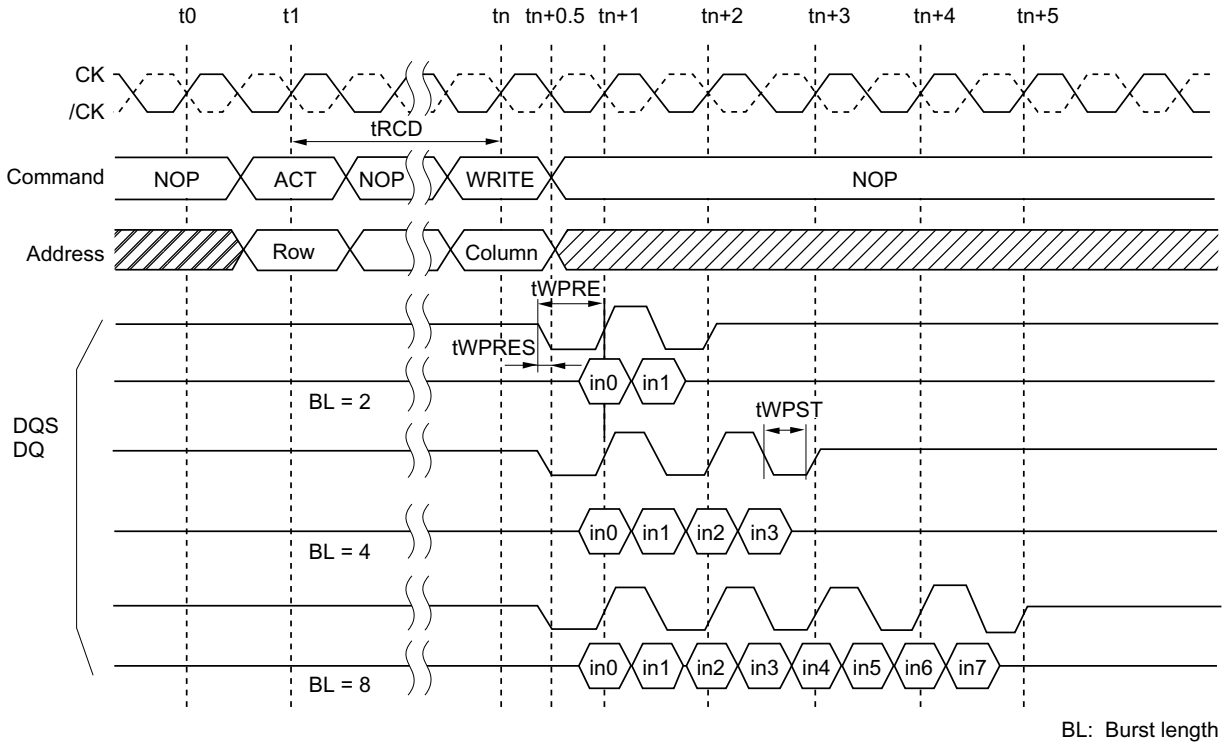
Read Operation (Burst Length)



Read Operation (/CAS Latency)

Write operation

The burst length (BL) and the burst type (BT) of the mode register are referred when a write command is issued. The burst length (BL) determines the length of a sequential data input by the write command that can be set to 2, 4, or 8. The latency from write command to data input is fixed to 1. The starting address of the burst read is defined by the column address, the bank select address which are loaded via the A0 to A11, BA0 to BA1 pins in the cycle when the write command is issued. DQS should be input as the strobe for the input-data and DM as well during burst operation. tWPRE prior to the first rising edge of the DQS should be set to Low and tWPST after the last falling edge of the data strobe can be set to High-Z. The leading low period of DQS is referred as write preamble. The last low period of DQS is referred as write postamble.



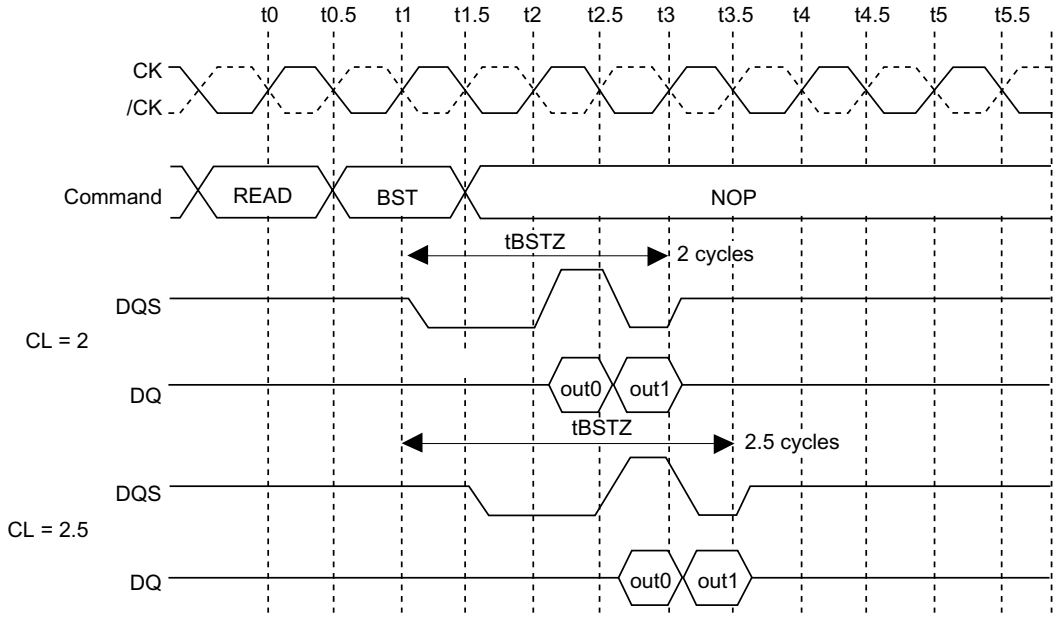
BL: Burst length

Write Operation

Burst Stop

Burst stop command during burst read

The burst stop (BST) command is used to stop data output during a burst read. The BST command stops the burst read and sets the output buffer to High-Z. tBSTZ (= CL) cycles after a BST command issued, the DQ pins become High-Z. The BST command is not supported for the burst write operation. Note that bank address is not referred when this command is executed.



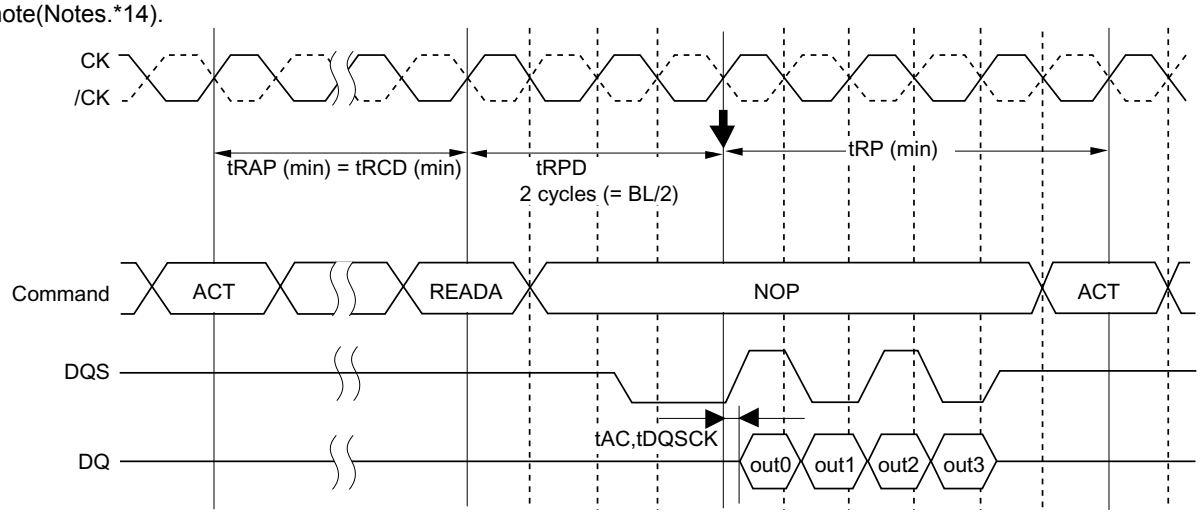
CL: /CAS latency

Burst Stop during a Read Operation

Auto Precharge

Read with auto-precharge

The precharge is automatically performed after completing a read operation. The precharge starts tRPD (BL/2) cycle after READA command input. tRAP specification for READA allows a read command with auto precharge to be issued to a bank that has been activated (opened) but has not yet satisfied the tRAS (min) specification. A column command to the other active bank can be issued the next cycle after the last data output. Read with auto-precharge command does not limit row commands execution for other bank. Refer to 'Function truth table and related note(Notes.*14).

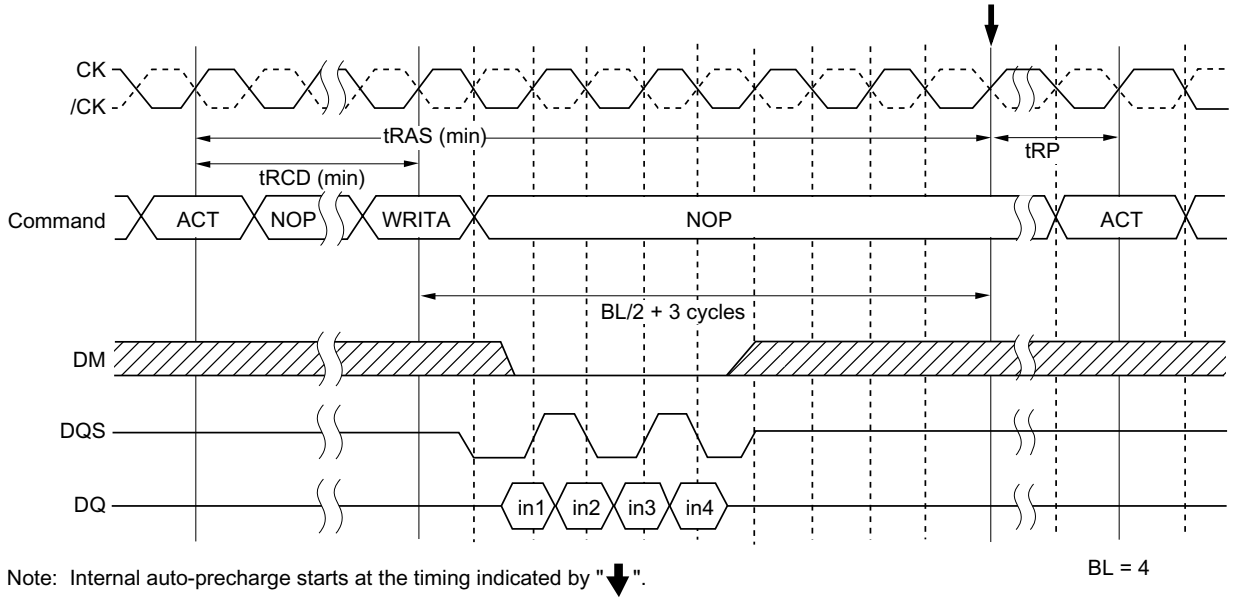


Note: Internal auto-precharge starts at the timing indicated by "↓".

Read with auto-precharge

Write with auto-precharge

The precharge is automatically performed after completing a burst write operation. The precharge operation is started (BL/ 2 + 3) cycles after WRITA command issued. A column command to the other banks can be issued the next cycle after the internal precharge command issued. Write with auto-precharge command does not limit row commands execution for other bank. Refer to the 'Read with Auto-Precharge Enabled, Write with Auto-Precharge Enabled' section. Refer to 'Function truth table and related note(Notes.*14)'.



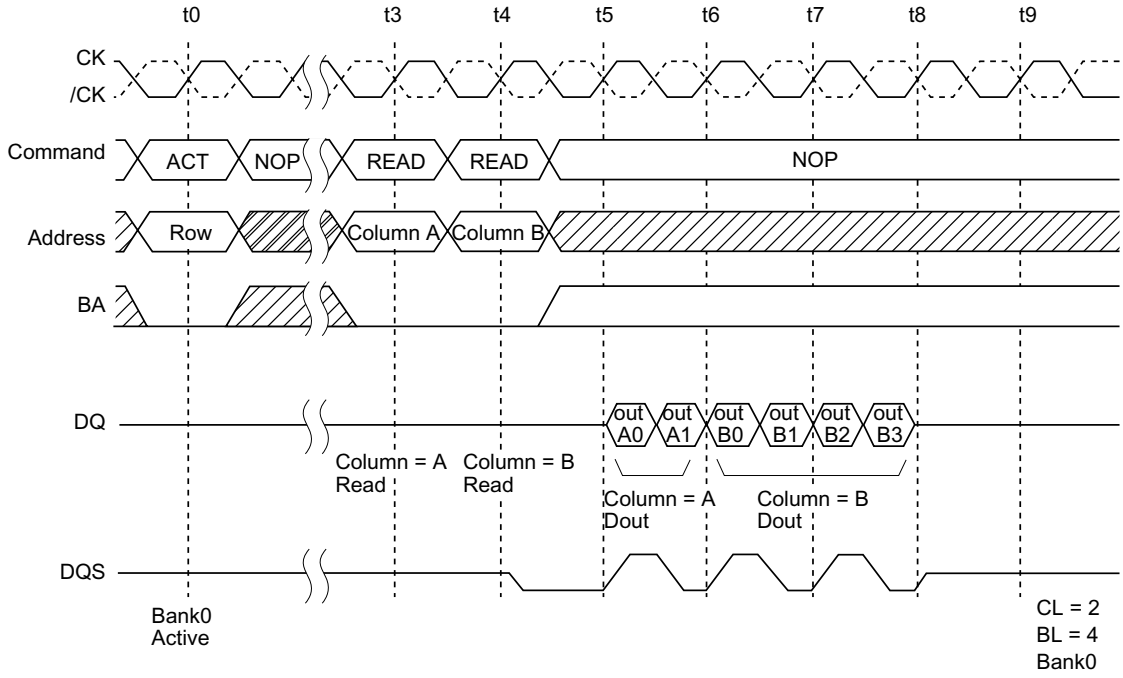
Note: Internal auto-precharge starts at the timing indicated by "↓".

Burst Write (BL = 4)

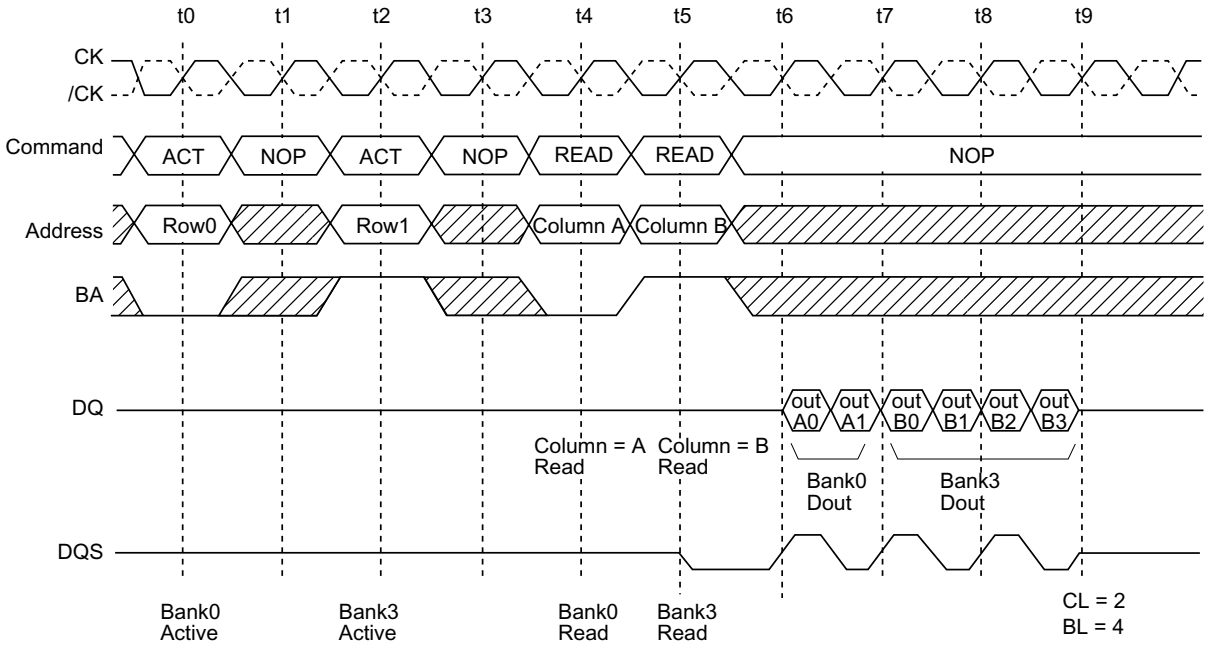
Command Intervals

A Read command to the consecutive Read command Interval

	Destination row of the consecutive read command			
	Bank address	Row address	State	Operation
1.	Same	Same	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
2.	Same	Different	—	Precharge the bank to interrupt the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
			IDLE	Precharge the bank without interrupting the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued.



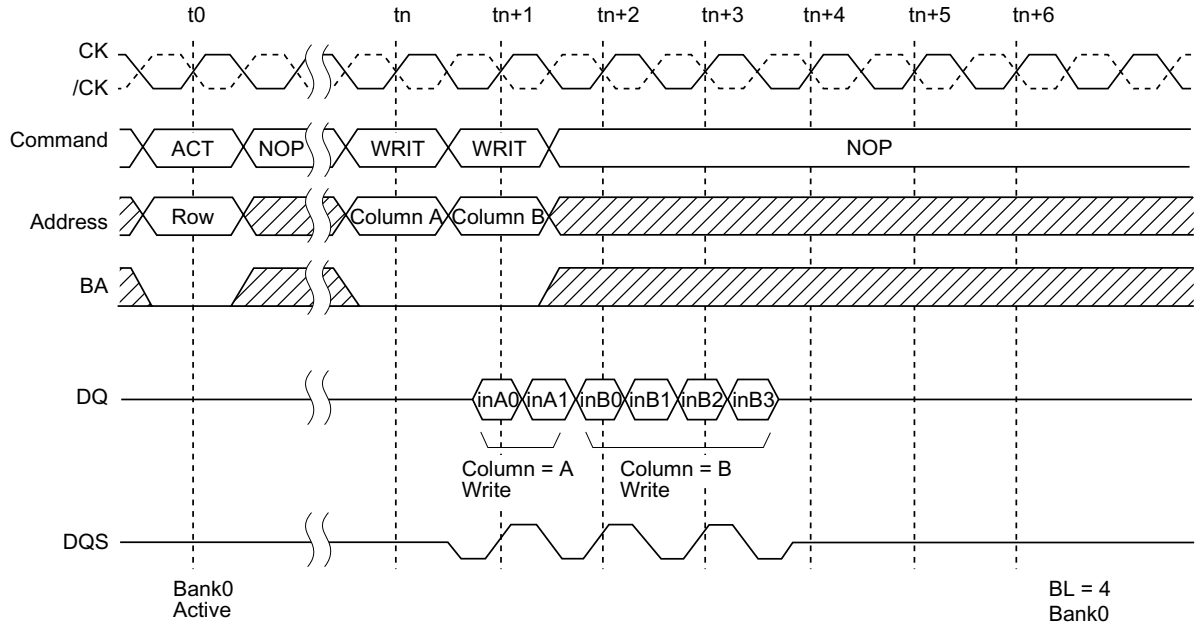
READ to READ Command Interval (same ROW address in the same bank)



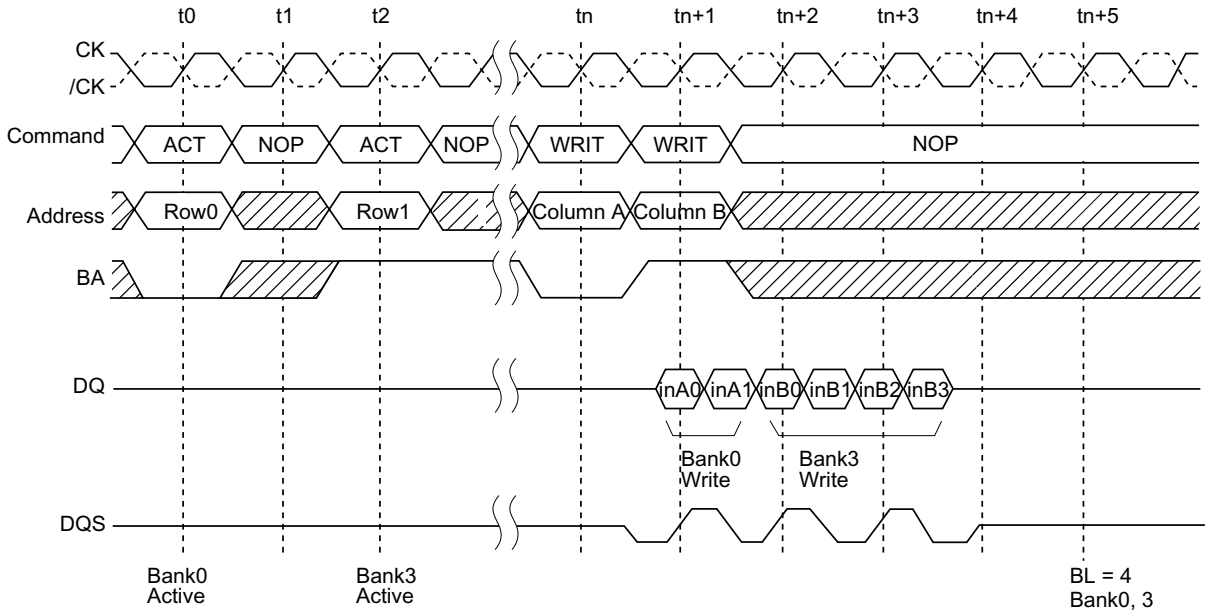
READ to READ Command Interval (different bank)

A Write command to the consecutive Write command Interval

	Destination row of the consecutive write command			
	Bank address	Row address	State	Operation
1.	Same	Same	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
2.	Same	Different	—	Precharge the bank to interrupt the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued. See 'A write command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
			IDLE	Precharge the bank without interrupting the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued.



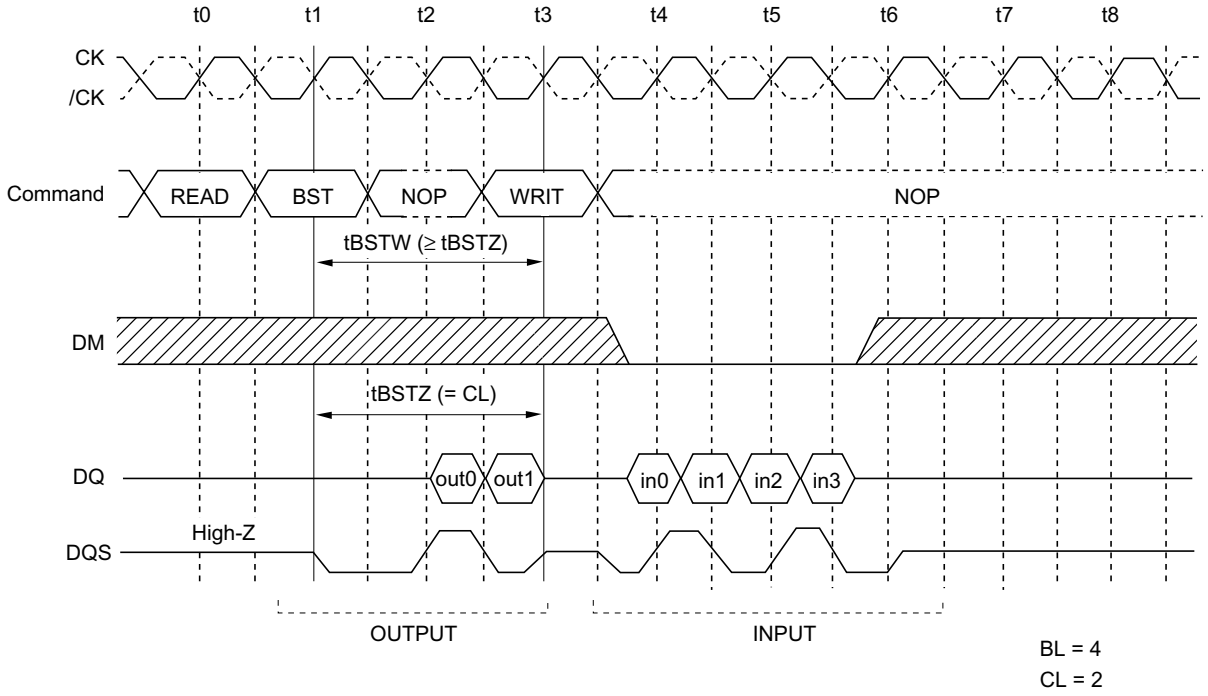
WRITE to WRITE Command Interval (same ROW address in the same bank)



WRITE to WRITE Command Interval (different bank)

A Read command to the consecutive Write command interval with the BST command

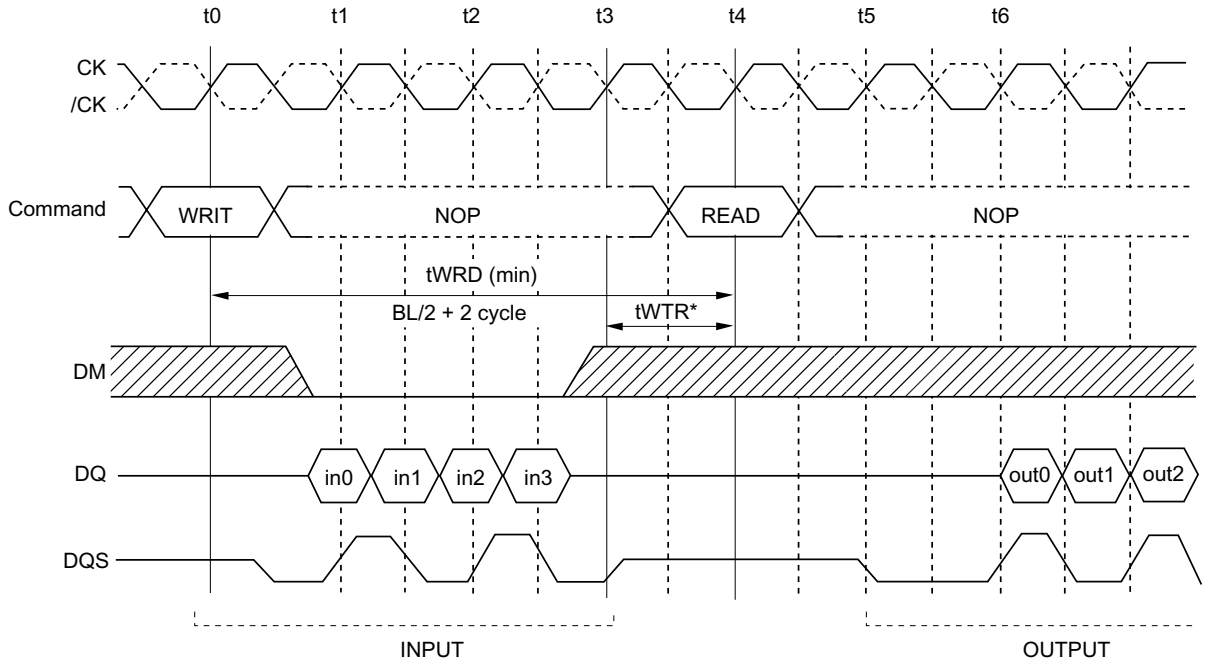
	Destination row of the consecutive write command			
	Bank address	Row address	State	Operation
1.	Same	Same	ACTIVE	Issue the BST command. tBSTW (≥ tBSTZ) after the BST command, the consecutive write command can be issued.
2.	Same	Different	—	Precharge the bank to interrupt the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	Issue the BST command. tBSTW (≥ tBSTZ) after the BST command, the consecutive write command can be issued.
			IDLE	Precharge the bank independently of the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued.



READ to WRITE Command Interval

A Write command to the consecutive Read command interval: To complete the burst operation

	Destination row of the consecutive read command			
	Bank address	Row address	State	Operation
1.	Same	Same	ACTIVE	To complete the burst operation, the consecutive read command should be performed tWRD (= BL/ 2 + 2) after the write command.
2.	Same	Different	—	Precharge the bank tWPD after the preceding write command. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	To complete a burst operation, the consecutive read command should be performed tWRD (= BL/ 2 + 2) after the write command.
			IDLE	Precharge the bank independently of the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued.



Note: tWTR is referenced from the first positive CK edge after the last desired data in pair tWTR.

BL = 4
CL = 2

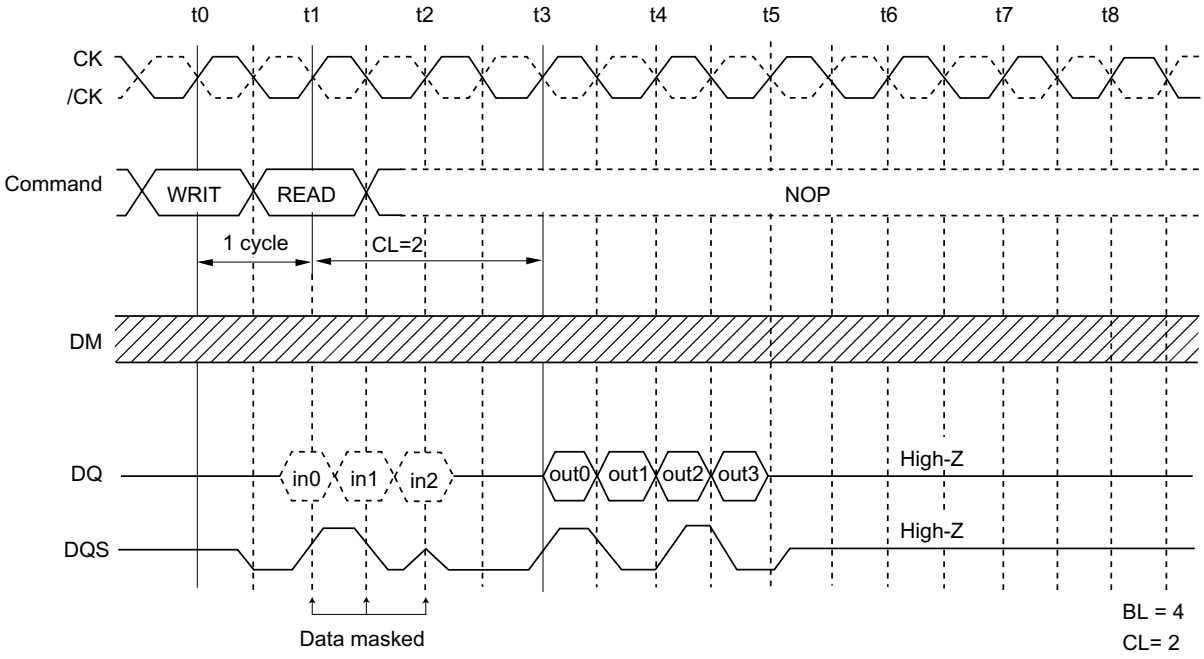
WRITE to READ Command Interval

A Write command to the consecutive Read command interval: To interrupt the write operation

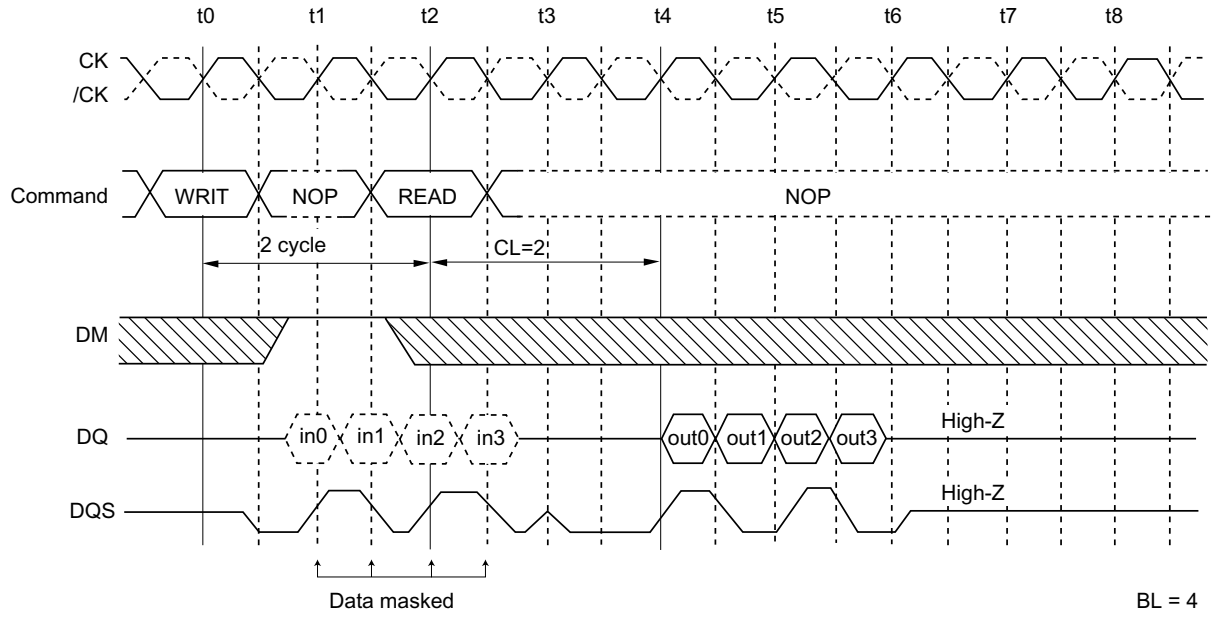
	Destination row of the consecutive read command			
	Bank address	Row address	State	Operation
1.	Same	Same	ACTIVE	DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary.
2.	Same	Different	—	—*1
3.	Different	Any	ACTIVE	DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary.
			IDLE	—*1

Note: 1. Precharge must be preceded to read command. Therefore read command can not interrupt the write operation in this case.

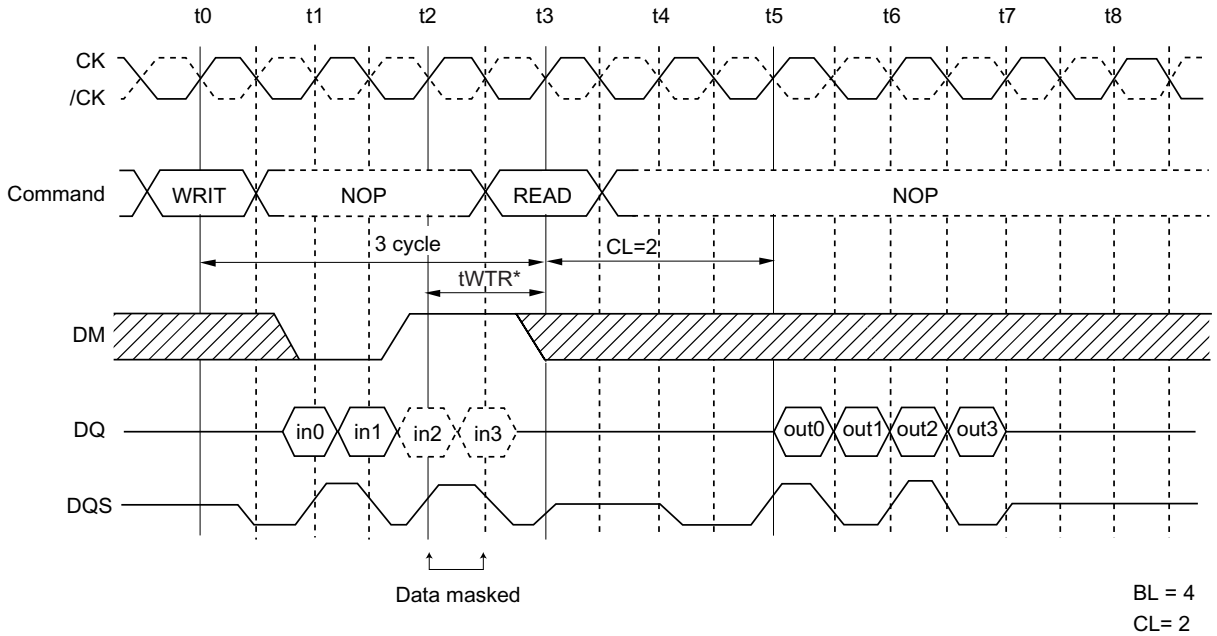
WRITE to READ Command Interval (Same bank, same ROW address)



[WRITE to READ delay = 1 clock cycle]



[WRITE to READ delay = 2 clock cycle]

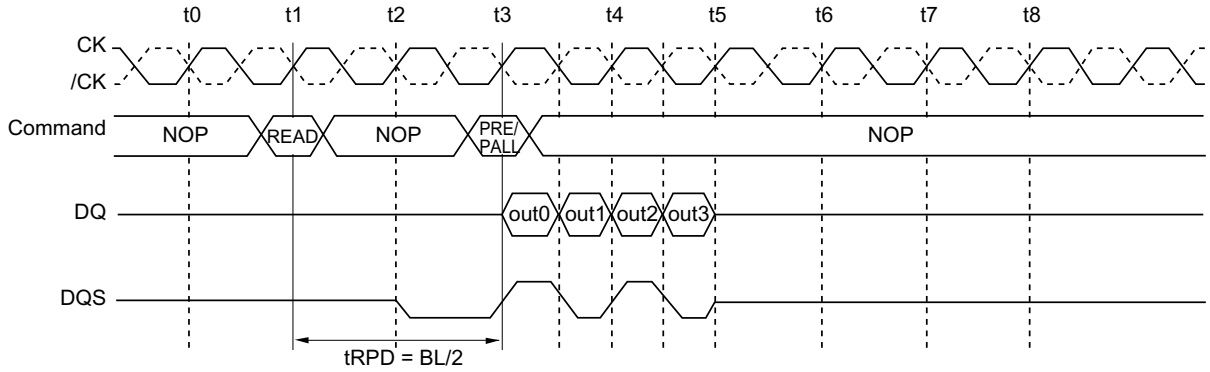


Note: tWTR is referenced from the first positive CK edge after the last desired data in pair tWTR.

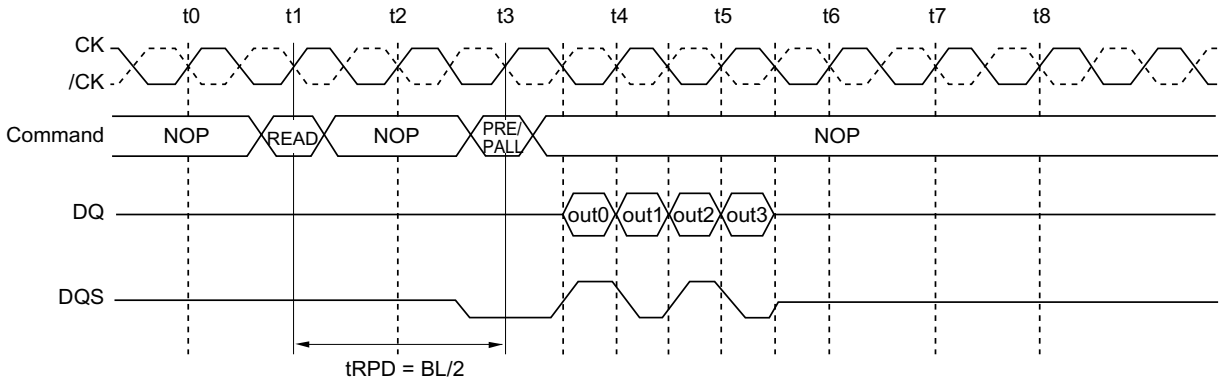
[WRITE to READ delay = 3 clock cycle]

A Read command to the consecutive Precharge command interval (same bank): To output all data

To complete a burst read operation and get a burst length of data, the consecutive precharge command must be issued tRPD (= BL/ 2 cycles) after the read command is issued.



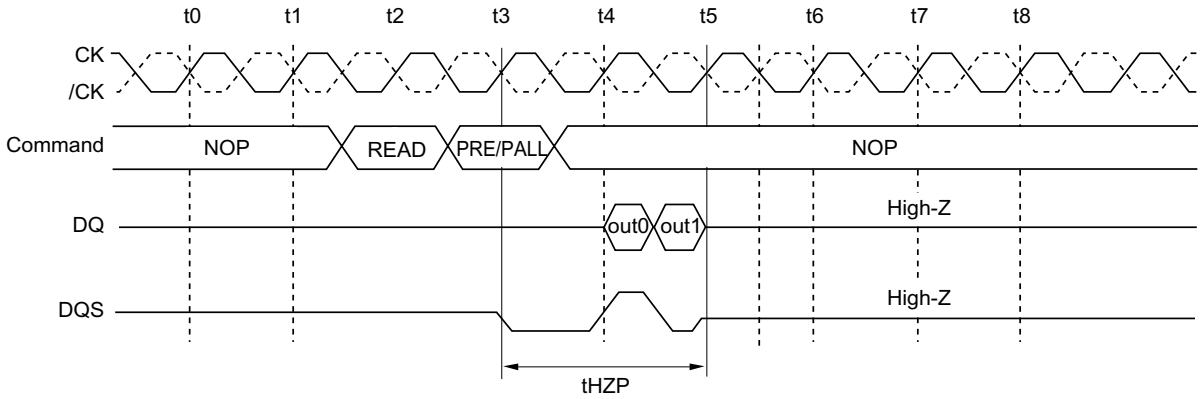
READ to PRECHARGE Command Interval (same bank): To output all data (CL = 2, BL = 4)



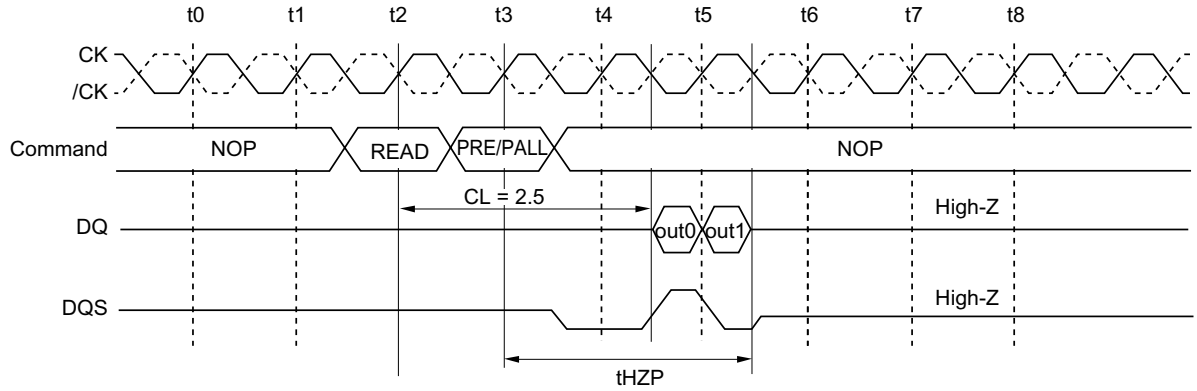
READ to PRECHARGE Command Interval (same bank): To output all data (CL = 2.5, BL = 4)

READ to PRECHARGE Command Interval (same bank): To stop output data

A burst data output can be interrupted with a precharge command. All DQ pins and DQS pins become High-Z tHZP (= CL) after the precharge command.



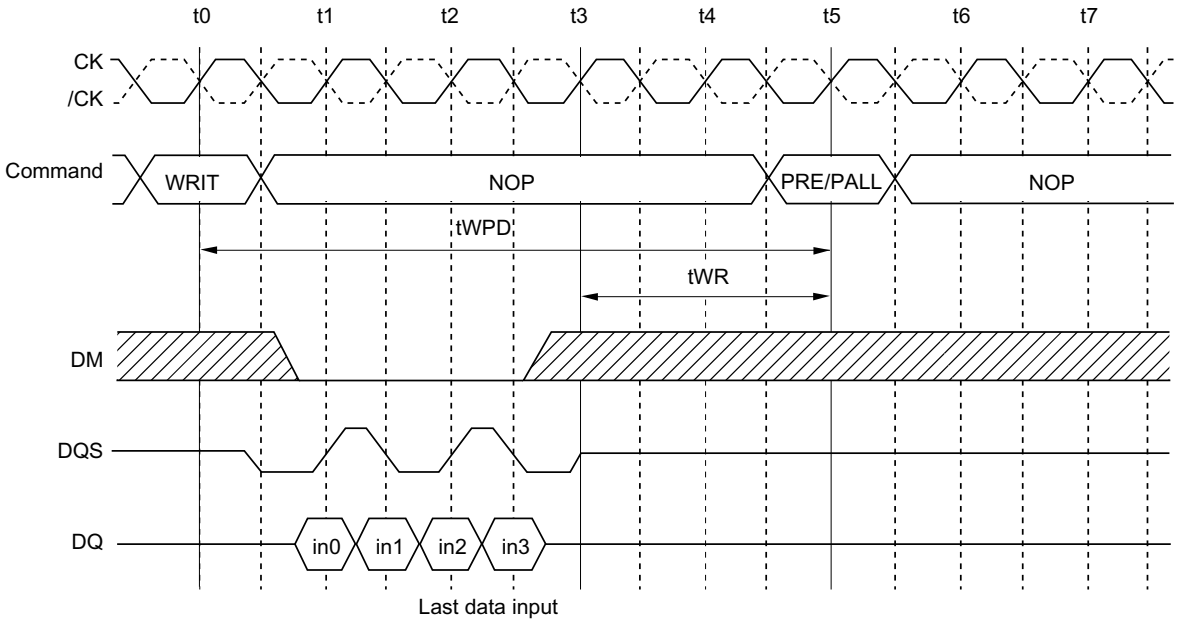
READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 2, BL = 2, 4, 8)



READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 2.5, BL = 2, 4, 8)

A Write command to the consecutive Precharge command interval (same bank)

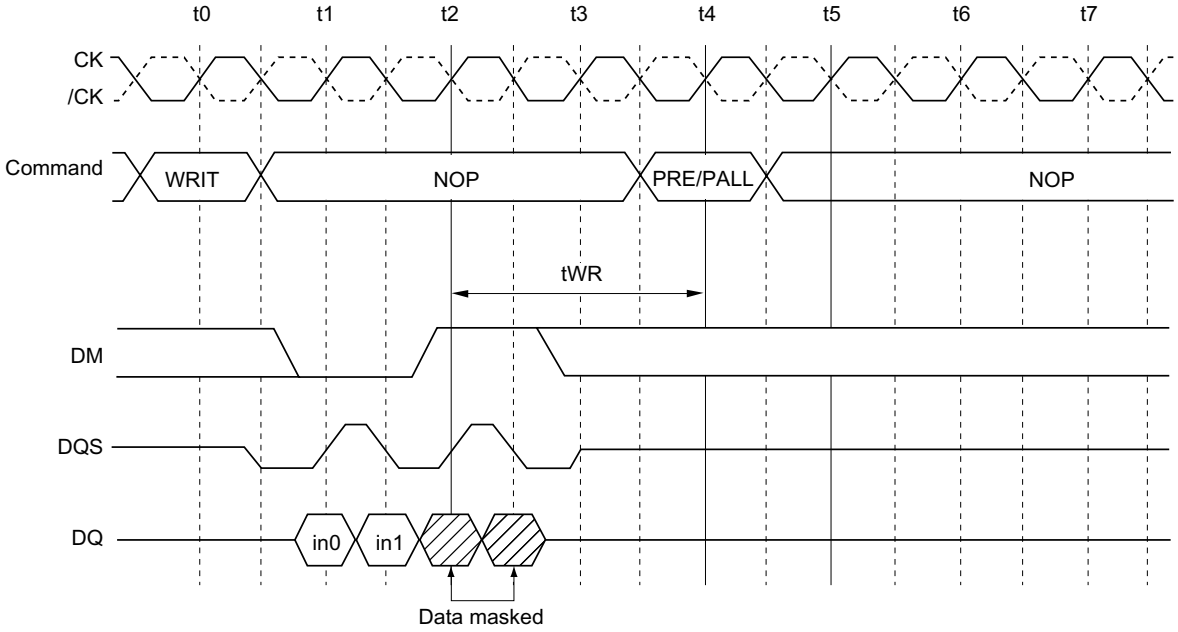
The minimum interval tWPD is necessary between the write command and the precharge command.



WRITE to PRECHARGE Command Interval (same bank) (BL = 4)

Precharge Termination in Write Cycles

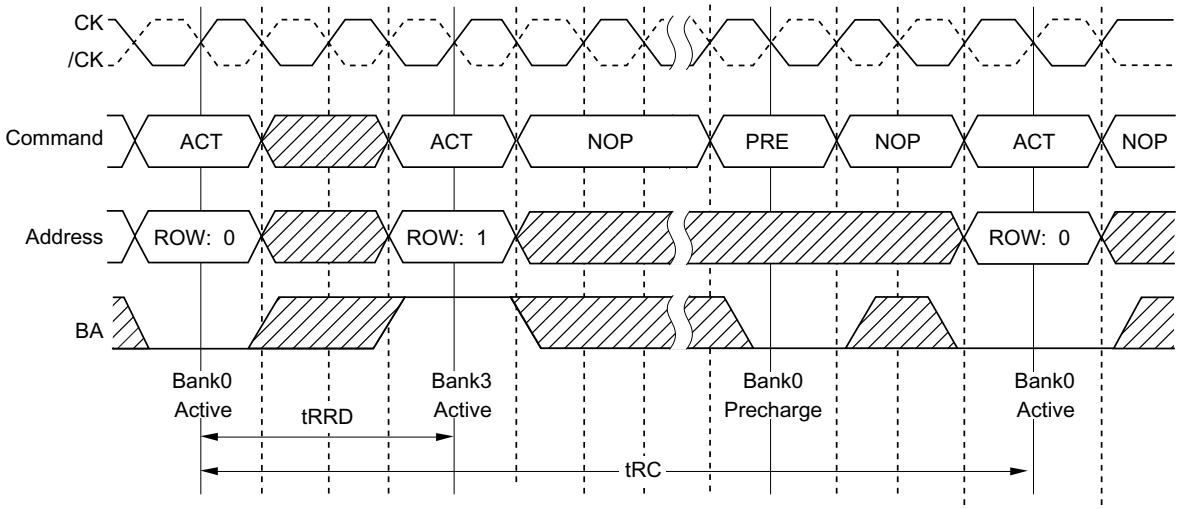
During a burst write cycle without auto precharge, the burst write operation is terminated by a precharge command of the same bank. In order to write the last input data, tWR (min) must be satisfied. When the precharge command is issued, the invalid data must be masked by DM.



Precharge Termination in Write Cycles (same bank) (BL = 4)

Bank active command interval

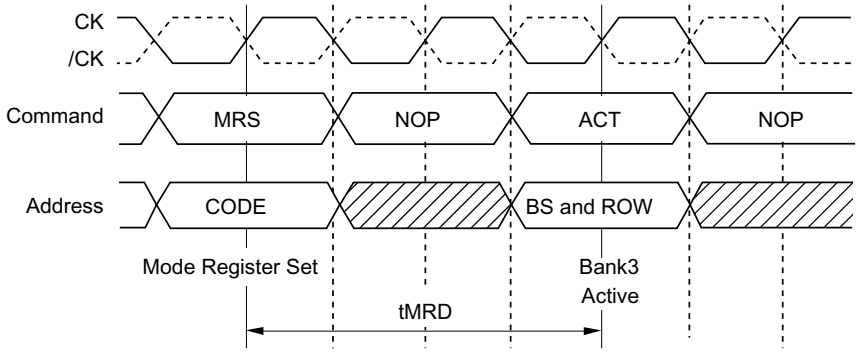
	Destination row of the consecutive ACT command			
	Bank address	Row address	State	Operation
1.	Same	Any	ACTIVE	Two successive ACT commands can be issued at tRC interval. In between two successive ACT operations, precharge command should be executed.
2.	Different	Any	ACTIVE	Precharge the bank. tRP after the precharge command, the consecutive ACT command can be issued.
			IDLE	tRRD after an ACT command, the next ACT command can be issued.



Bank Active to Bank Active

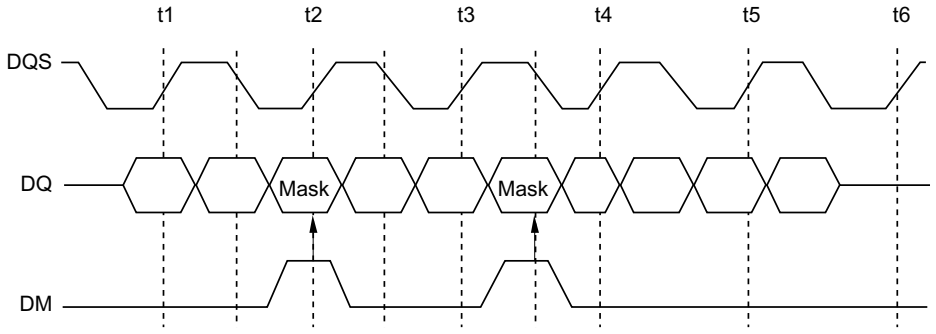
Mode register set to Bank-active command interval

The interval between setting the mode register and executing a bank-active command must be no less than tMRD.



DM Control

DM can mask input data. In ×16 products, UDM and LDM can mask the upper and lower byte of input data, respectively. By setting DM to Low, data can be written. When DM is set to High, the corresponding data is not written, and the previous data is held. The latency between DM input and enabling/disabling mask function is 0.

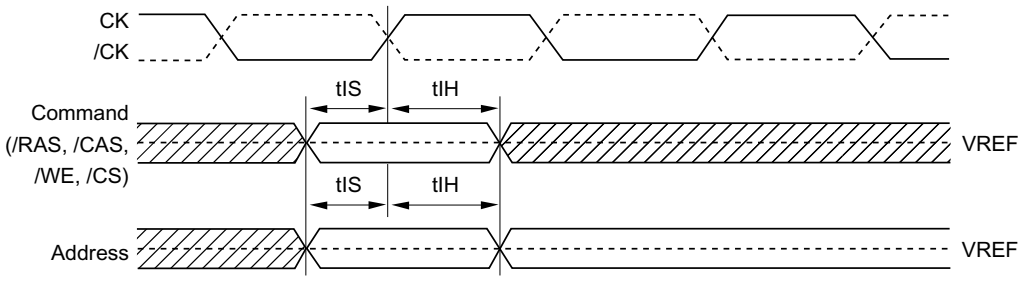


Write mask latency = 0

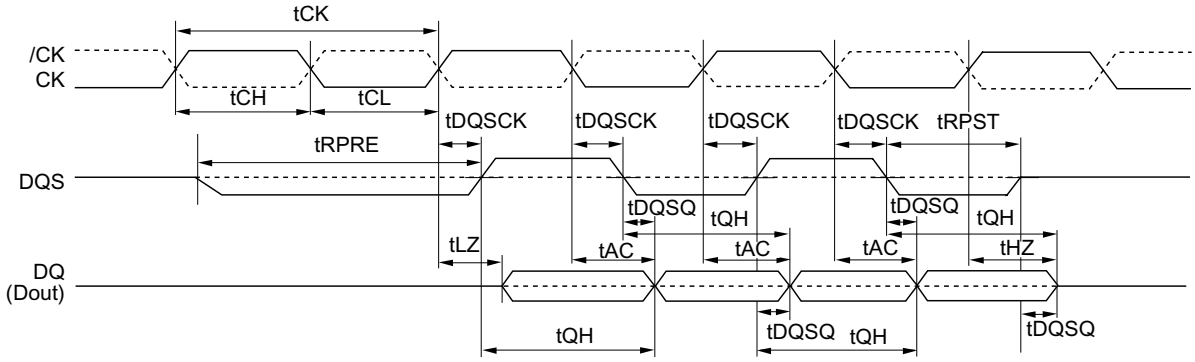
DM Control

Timing Waveforms

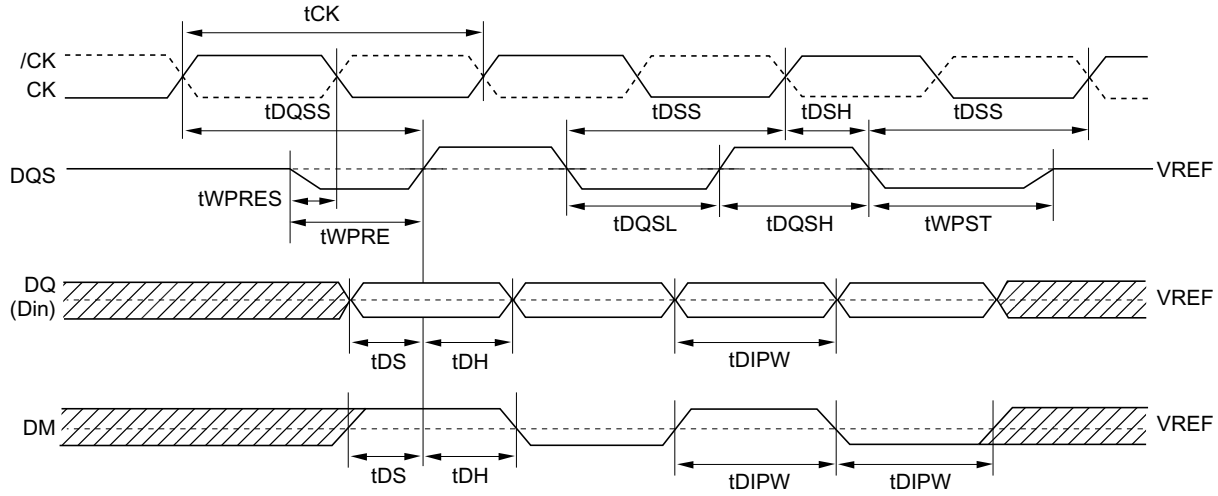
Command and Addresses Input Timing Definition



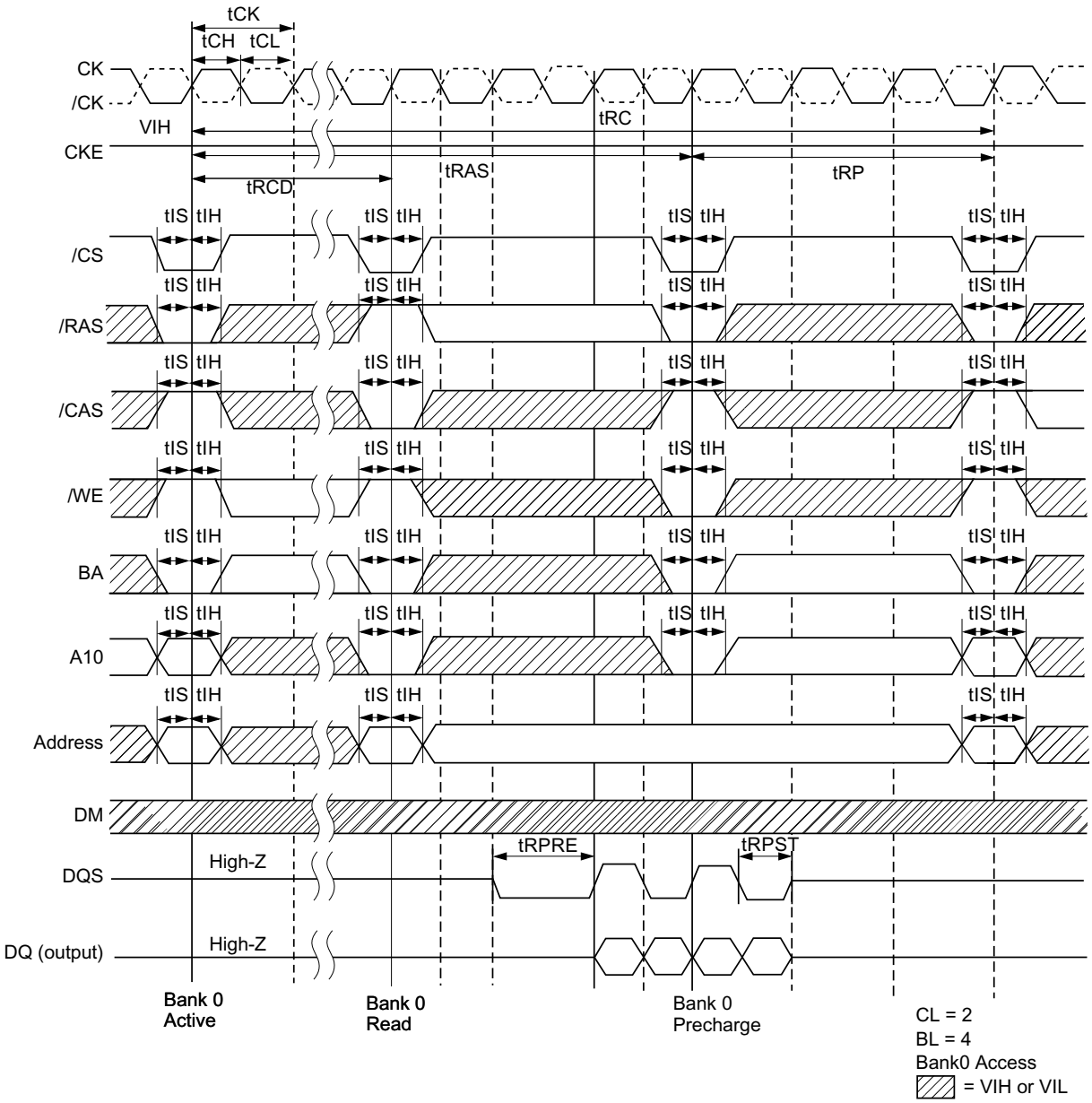
Read Timing Definition



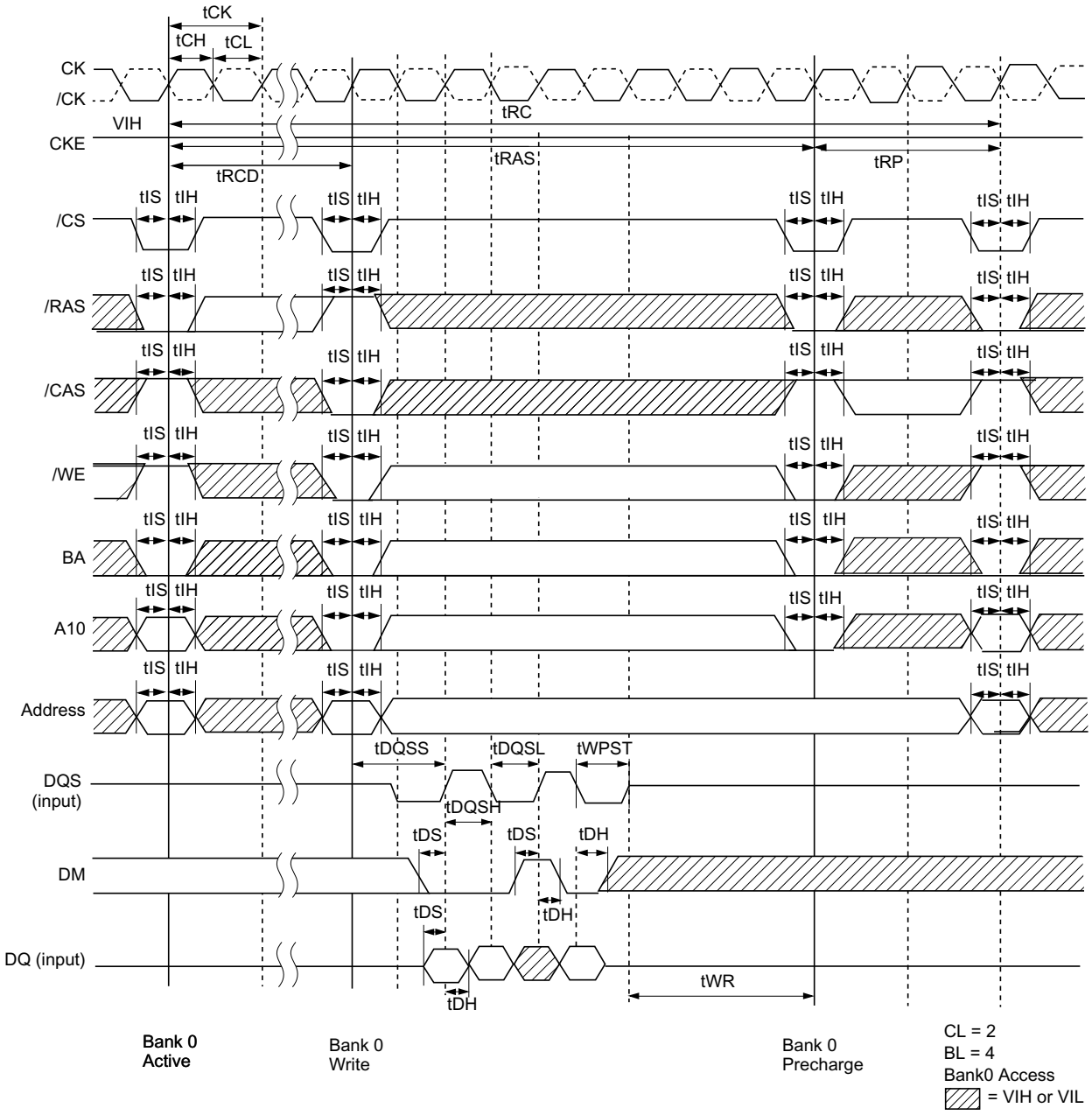
Write Timing Definition



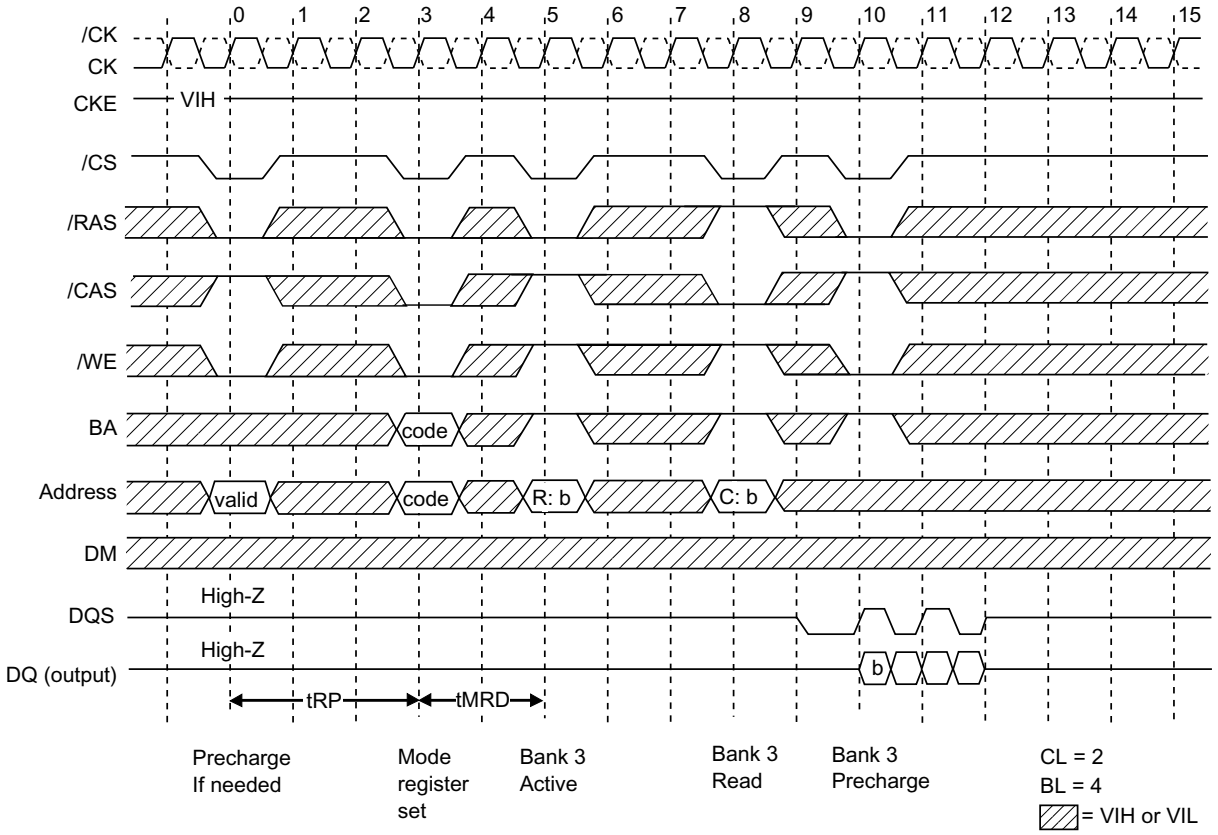
Read Cycle


tCK
tCH
tCL
CK
/CK
VIH
CKE
tRC
tRAS
tRP
tRCD
tIS
tIH
/CS
/RAS
/CAS
/WE
BA
A10
Address
DM
tRPRE
tRPST
DQS
High-Z
DQ (output)
High-Z
Bank 0
Active
Bank 0
Read
Bank 0
Precharge
CL = 2
BL = 4
Bank0 Access
= VIH or VIL

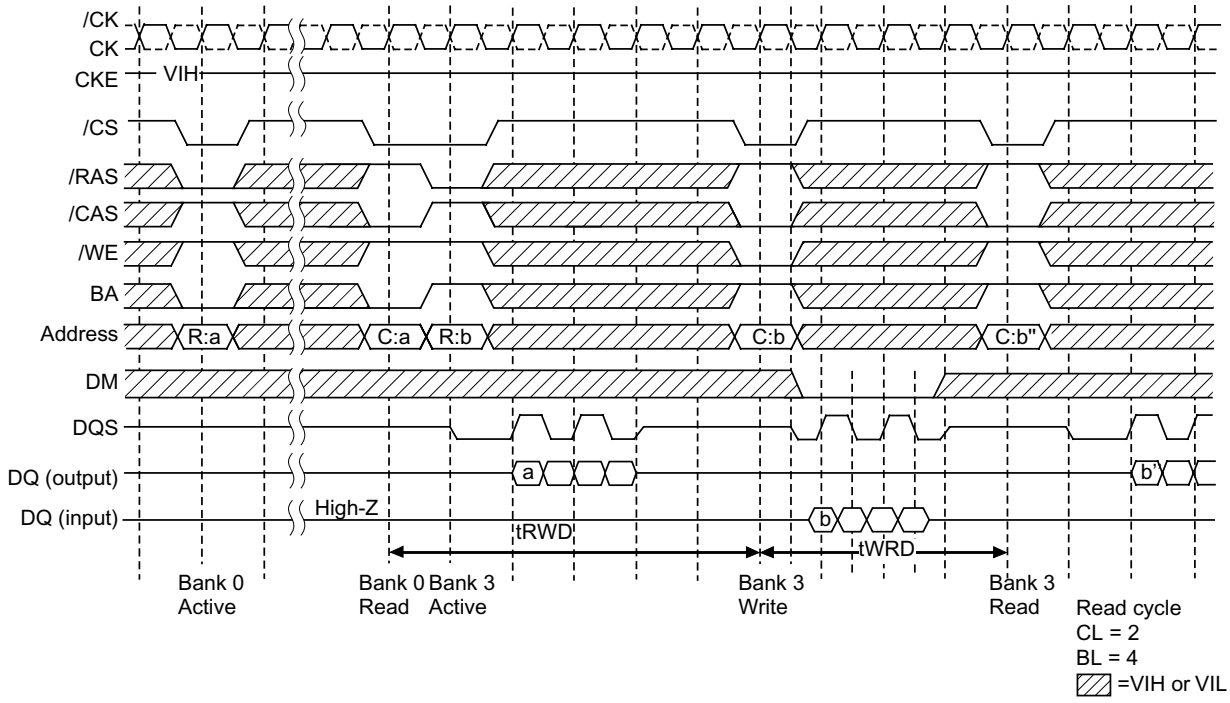
Write Cycle


tCK
tCH
tCL
CK
/CK
VIH
CKE
tRC
tRAS
tRP
tRCD
tIS
tIH
/CS
/RAS
/CAS
/WE
BA
A10
Address
tDQSS
tDQSL
tWPST
DQS
(input)
tDQSH
tDS
tDH
DM
DQ (input)
tWR
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CL = 2
BL = 4
Bank0 Access
= VIH or VIL

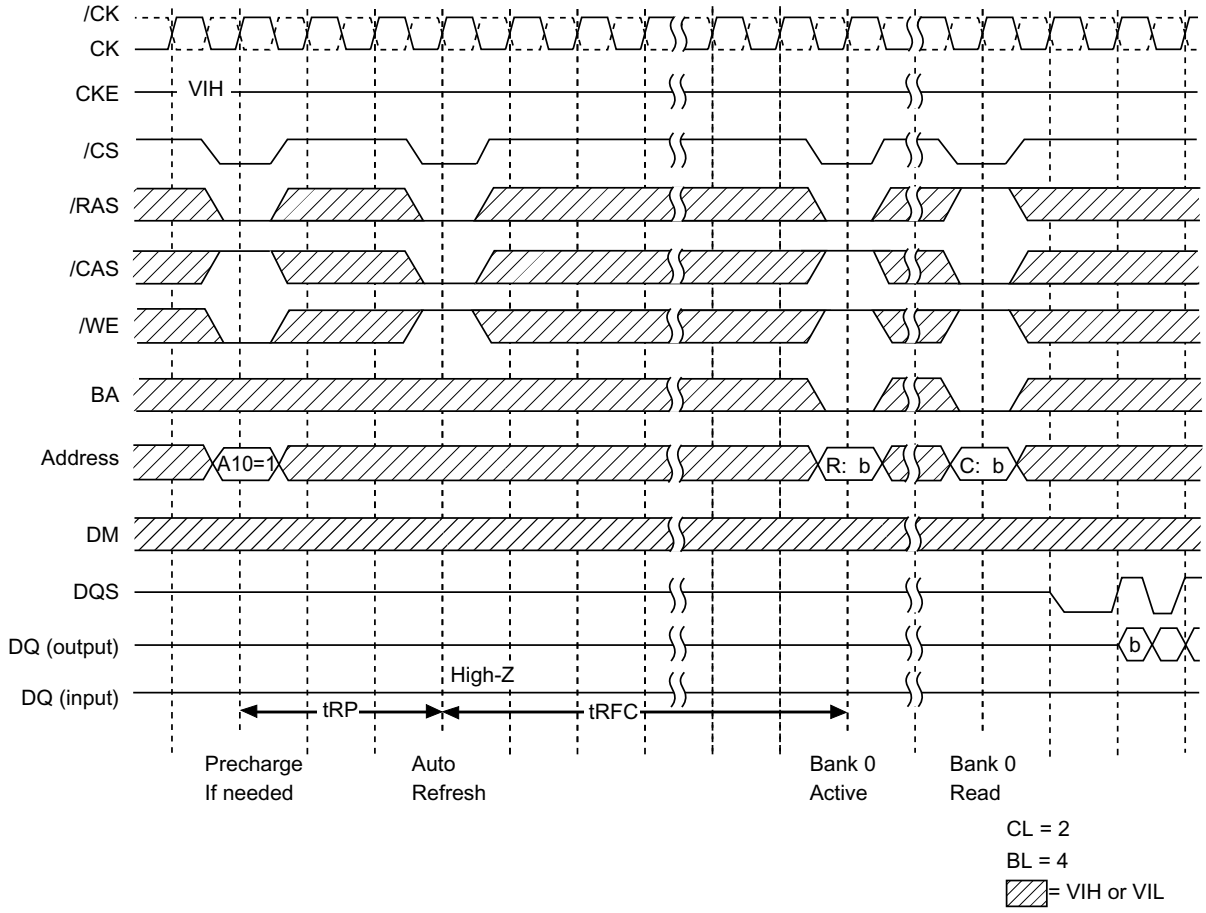
Mode Register Set Cycle



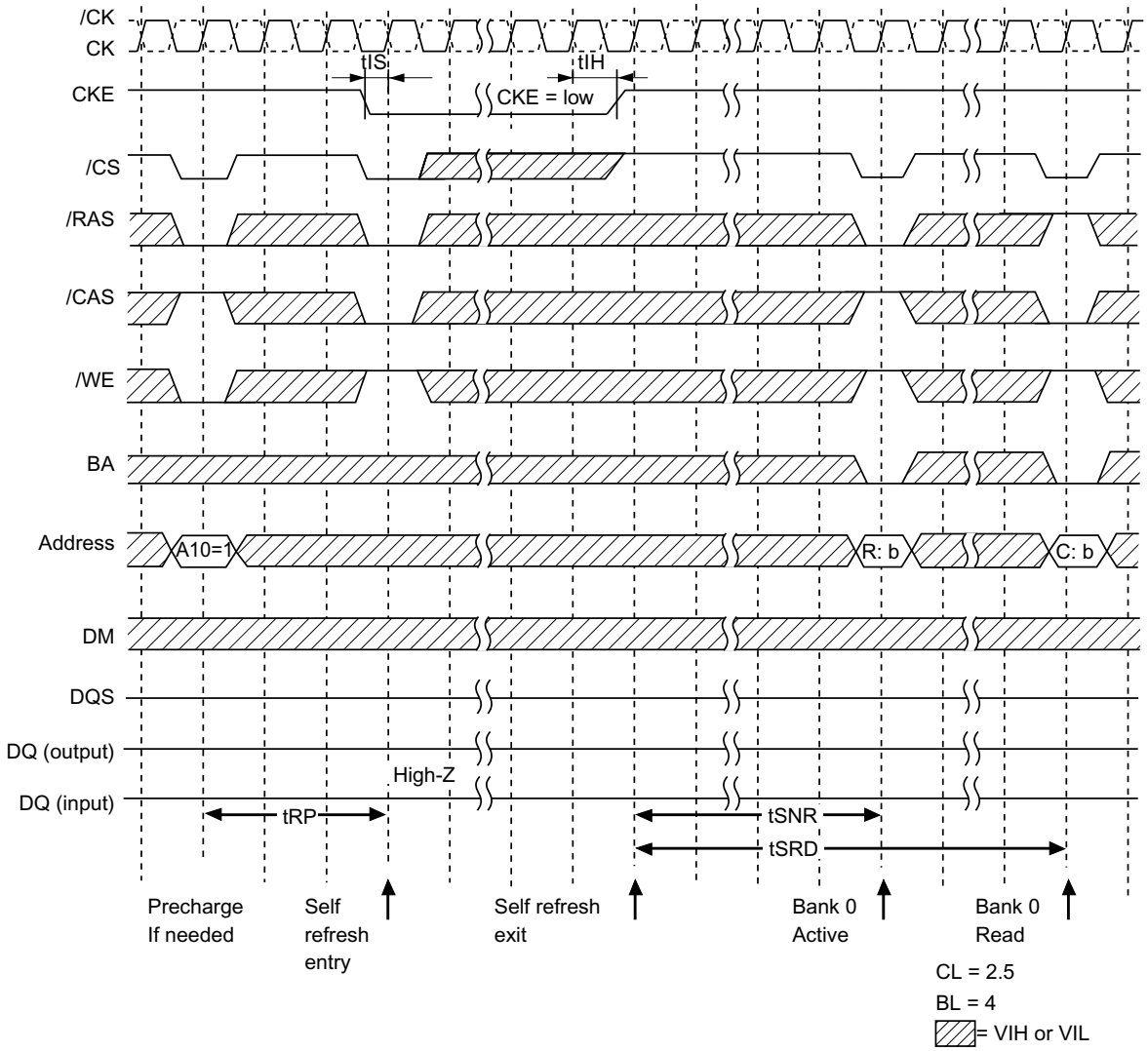
Read/Write Cycle



Auto Refresh Cycle



Self Refresh Cycle

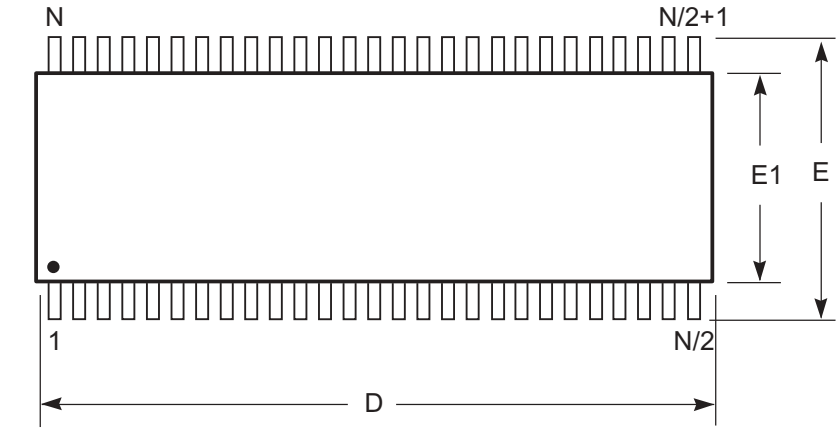


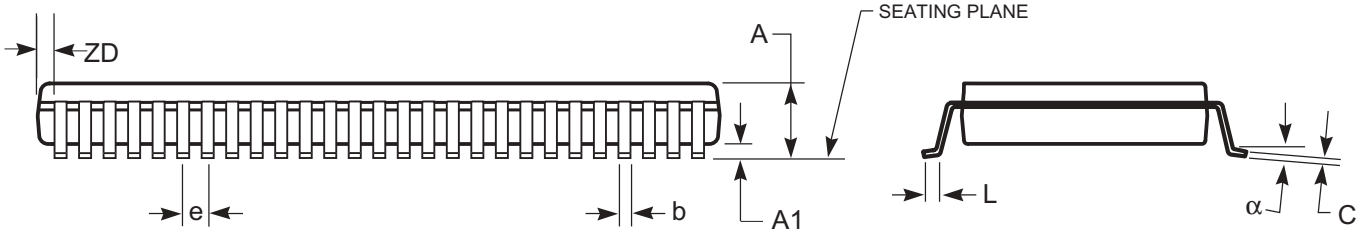
ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS43R16800A-6T	66-pin TSOP-II
166 MHz	6	IS43R16800A-6TL	66-pin TSOP-II, Lead-free

Plastic TSOP 66-pin
Package Code: T (Type II)





Notes:
1. Controlling dimension: millimieters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Plastic TSOP (T - Type II)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads (N)		66		
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	—	—	—	—
b	0.24	0.40	0.009	0.016
C	0.12	0.21	0.005	0.0083
D	22.02	22.42	0.867	0.8827
E1	10.03	10.29	0.395	0.405
E	11.56	11.96	0.455	0.471
e	0.65 BSC		0.026 BSC	
L	0.40	0.60	0.016	0.024
L1	—	—	—	—
ZD	0.71 REF		0.028 REF	
α	0°	8°	0°	8°