

## 8Meg x16 128-MBIT SYNCHRONOUS DRAM

PRELIMINARY INFORMATION  
MAY 2006

### FEATURES

- Clock frequency: 143 MHz
  - Fully synchronous; all signals referenced to a positive clock edge
  - Internal bank for hiding row access/precharge
  - Power supply
- |              |                 |                  |
|--------------|-----------------|------------------|
|              | V <sub>DD</sub> | V <sub>DDQ</sub> |
| IS42S16800A1 | 3.3V            | 3.3V             |
- LVTTL interface
  - Programmable burst length  
– (1, 2, 4, 8, full page)
  - Programmable burst sequence:  
Sequential/Interleave
  - Auto Refresh (CBR)
  - Self Refresh with programmable refresh periods
  - 4096 refresh cycles every 64 ms
  - Random column address every clock cycle
  - Programmable  $\overline{\text{CAS}}$  latency (2, 3 clocks)
  - Burst read/write and burst read/single write operations capability
  - Burst termination by burst stop and precharge command
  - Lead-free Availability

### OVERVIEW

ISSI's 128Mb Synchronous DRAM achieves high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input. The 128Mb SDRAM is organized as follows.

IS42S16800A1

2M x16x4 Banks

54-pin TSOPII

### KEY TIMING PARAMETERS

Parameter	-7	Unit
CK Cycle Time		
$\overline{\text{CAS}}$ Latency = 3	7	ns
$\overline{\text{CAS}}$ Latency = 2	7.5	ns
CK Frequency		
$\overline{\text{CAS}}$ Latency = 3	143	Mhz
$\overline{\text{CAS}}$ Latency = 2	133	Mhz
Access Time from Clock		
$\overline{\text{CAS}}$ Latency = 3	5	ns
$\overline{\text{CAS}}$ Latency = 2	5.4	ns

**DEVICE OVERVIEW**

The 128Mb SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 3.3V V<sub>DD</sub> and 3.3V V<sub>DDQ</sub> memory systems containing 134,217,728 bits. Internally configured as a quad-bank DRAM with a synchronous interface. Each 33,554,432-bit bank is organized as 4,096 rows by 512 columns by 16 bits.

The 128Mb SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CK. All inputs and outputs are LVTTTL compatible.

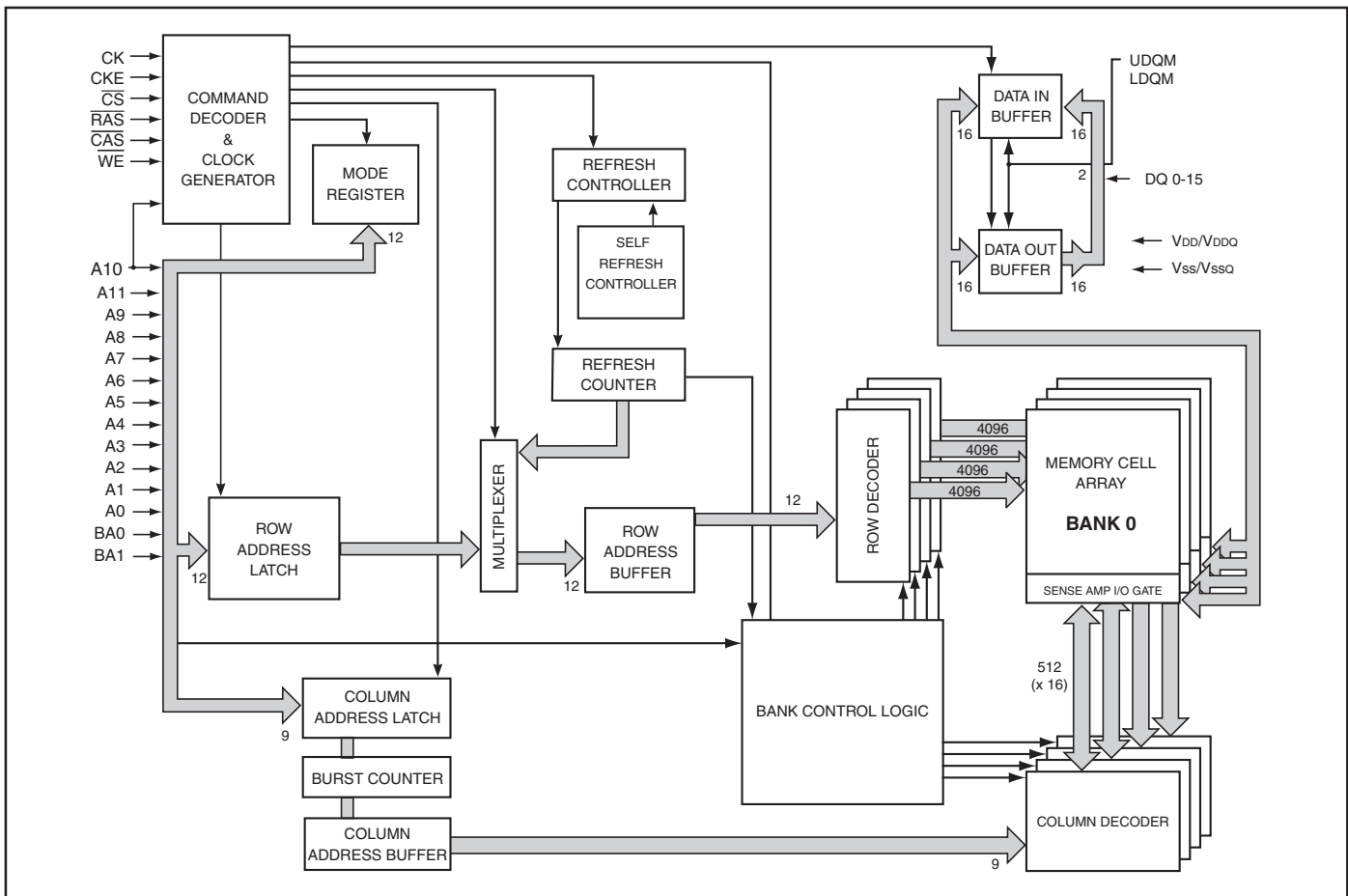
The 128Mb SDRAM has the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during burst access.

A self-timed row precharge initiated at the end of the burst sequence is available with the AUTO PRECHARGE function enabled. Precharge one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

SDRAM read and write accesses are burst oriented starting at a selected location and continuing for a programmed number of locations in a programmed sequence. The registration of an ACTIVE command begins accesses, followed by a READ or WRITE command. The ACTIVE command in conjunction with address bits registered are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The READ or WRITE commands in conjunction with address bits registered are used to select the starting column location for the burst access.

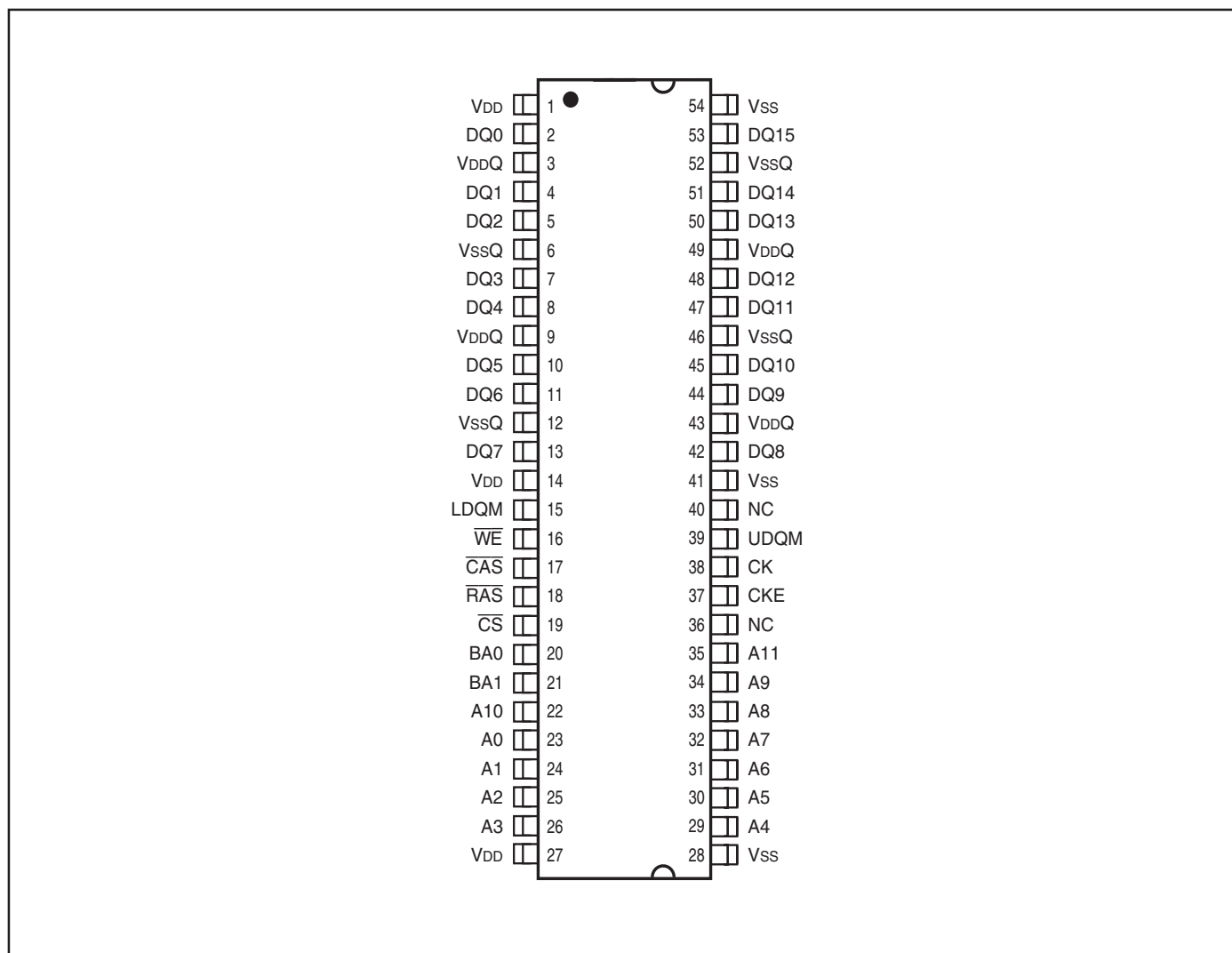
Programmable READ or WRITE burst lengths consist of 1, 2, 4 and 8 locations or full page, with a burst terminate option.

**FUNCTIONAL BLOCK DIAGRAM (2Mx16x4 BANKS)**



## PIN CONFIGURATIONS

54 pin TSOP - Type II for x16



## PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ15	Data I/O
CK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
LDQM	x16 Lower Byte, Input/Output Mask
UDQM	x16 Upper Byte, Input/Output Mask
V <sub>DD</sub>	Power
V <sub>SS</sub>	Ground
V <sub>DDQ</sub>	Power Supply for I/O Pin
V <sub>SSQ</sub>	Ground for I/O Pin
NC	No Connection

## PIN FUNCTIONS

Symbol	Type	Function (In Detail)
A0-A11	Input Pin	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column address A0-A8 (x16); with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
BA0, BA1	Input Pin	Bank Select Address: BA0 and BA1 defines which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
$\overline{\text{CAS}}$	Input Pin	$\overline{\text{CAS}}$ , in conjunction with the $\overline{\text{RAS}}$ and $\overline{\text{WE}}$ , forms the device command. See the "Command Truth Table" for details on device commands.
CKE	Input Pin	The CKE input determines whether the CK input is enabled. The next rising edge of the CK signal will be valid when is CKE HIGH and invalid when LOW. When CKE is LOW, the device will be in either power-down mode, clock suspend mode, or self refresh mode. CKE is an asynchronous input.
CK	Input Pin	CK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
$\overline{\text{CS}}$	Input Pin	The $\overline{\text{CS}}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{\text{CS}}$ is LOW, and disabled with $\overline{\text{CS}}$ is HIGH. The device remains in the previous state when $\overline{\text{CS}}$ is HIGH.
LDQM, UDQM	Input Pin	LDQM and UDQM control the lower and upper bytes of the I/O buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to the HIGH impedance state when LDQM/UDQM is HIGH. This function corresponds to $\overline{\text{OE}}$ in conventional DRAMs. In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and data can be written to the device. When LDQM or UDQM is HIGH, input data is masked and cannot be written to the device.
DQ0-DQ7 or DQ0-DQ15	Input/Output	Data on the Data Bus is latched on DQ pins during Write commands, and buffered for output after Read commands.
$\overline{\text{RAS}}$	Input Pin	$\overline{\text{RAS}}$ , in conjunction with $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ , forms the device command. See the "Command Truth Table" item for details on device commands.
$\overline{\text{WE}}$	Input Pin	$\overline{\text{WE}}$ , in conjunction with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ , forms the device command. See the "Command Truth Table" item for details on device commands.
V <sub>DDQ</sub>	Power Supply Pin	V <sub>DDQ</sub> is the output buffer power supply.
V <sub>DD</sub>	Power Supply Pin	V <sub>DD</sub> is the device internal power supply.
V <sub>SSQ</sub>	Power Supply Pin	V <sub>SSQ</sub> is the output buffer ground.
V <sub>SS</sub>	Power Supply Pin	V <sub>SS</sub> is the device internal ground.

## Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs.

Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all  $V_{DD}$  and  $V_{DDQ}$  pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed  $V_{DD}+0.3V$  on any of the input pins or  $V_{DD}$  supplies. The CK signal must be started at the same time. After power on, an initial pause of 200 $\mu$ s is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of two Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

## Programming the Mode Register

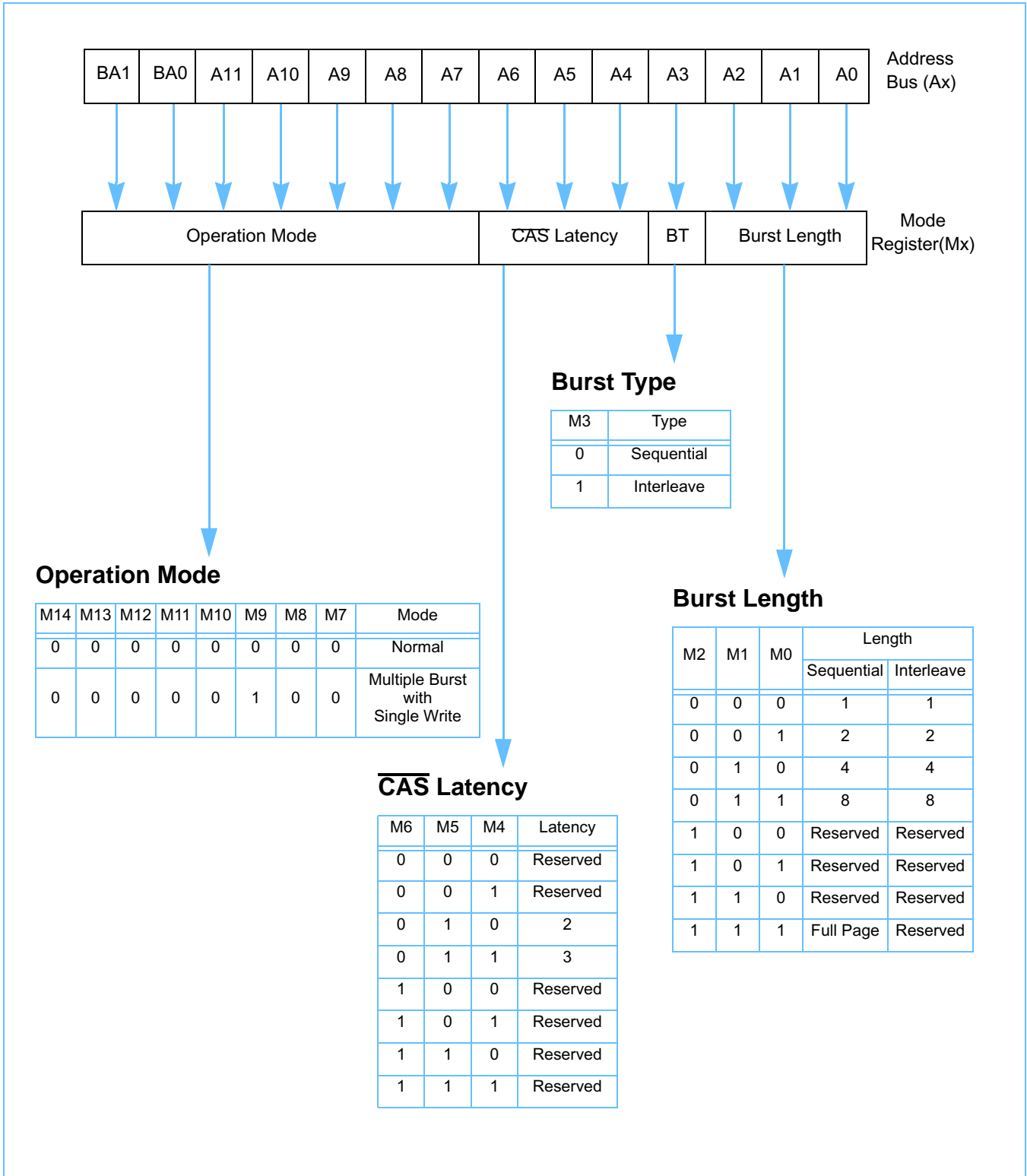
For application flexibility,  $\overline{CAS}$  latency, burst length, burst sequence, and operation type are user defined variables and must be programmed into the SDRAM Mode Register with a single Mode Register Set Command. Any content of the Mode Register can be altered by re-executing the Mode Register Set Command. If the user chooses to modify only a subset of the Mode Register variables, all four variables must be redefined when the Mode Register Set Command is issued.

After initial power up, the Mode Register Set Command must be issued before read or write cycles may begin. All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{CS}$ , and  $\overline{WE}$  at the positive edge of the clock. The address input data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued following the mode register set command once a delay equal to  $t_{RSC}$  has elapsed.

### $\overline{CAS}$ Latency

The  $\overline{CAS}$  latency is a parameter that is used to define the delay from when a Read Command is registered on a rising clock edge to when the data from that Read Command becomes available at the outputs. The  $\overline{CAS}$  latency is expressed in terms of clock cycles and can have a value of 2 or 3 cycles. The value of the  $\overline{CAS}$  latency is determined by the speed grade of the device and the clock frequency that is used in the application. A table showing the relationship between the  $\overline{CAS}$  latency, speed grade, and clock frequency appears in the Electrical Characteristics section of this document. Once the appropriate  $\overline{CAS}$  latency has been selected it must be programmed into the mode register after power up, for an explanation of this procedure see Programming the Mode Register in the previous section.

Mode Register Operation (Address Input For Mode Set)



## Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). There are three parameters that define how the burst mode will operate. These parameters include burst sequence, burst length, and operation mode. The burst sequence and burst length are programmable, and are determined by address bits A0 - A3 during the Mode Register Set command. Operation mode is also programmable and is set by address bits A7 - A11, BA0, and BA1.

The burst type is used to define the order in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequences are supported, sequential and interleaved. See the table below.

The burst length controls the number of bits that will be output after a Read Command, or the number of bits to be input after a Write Command. The burst length can be programmed to have values of 1, 2, 4, 8 and full page sequential burst.

Burst operation mode can be normal operation or multiple burst with single write operation. Normal operation implies that the device will perform burst operations on both read and write cycles until the desired burst length is satisfied. Multiple burst with single write operation was added to support Write Through Cache operation. Here, the programmed burst length only applies to read cycles. All write cycles are single write operations when this mode is selected.

## Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
2	x x 0	0, 1	0, 1
	x x 1	1, 0	1, 0
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
256 (Full Page)	n= A0-A7	Cn, Cn1+2, Cn+3, C+4, ...	Not supported

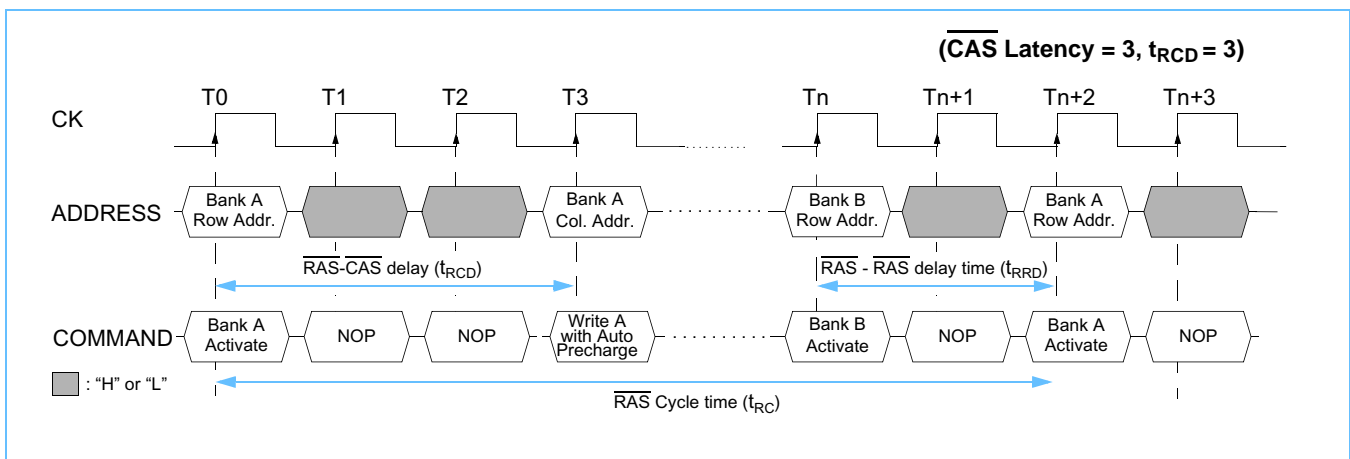
**Note:** Page length is a function of I/O organization and column addressing.  
x16 organization (CA0-CA8); Page Length = 512 bits

### Bank Activate Command

In relation to the operation of a fast page mode DRAM, the Bank Activate command correlates to a falling  $\overline{\text{RAS}}$  signal. The Bank Activate command is issued by holding  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$  high with  $\overline{\text{CS}}$  and  $\overline{\text{RAS}}$  low at the rising edge of the clock. The Bank Select address BA0 - BA1 is used to select the desired bank. The row address A0 - A11 is used to determine which row to activate in the selected bank.

The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must meet or exceed the  $\overline{\text{RAS}}$  to  $\overline{\text{CAS}}$  delay time ( $t_{\text{RCD}}$ ). Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device ( $t_{\text{RC}}$ ). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time ( $t_{\text{RRD}}$ ). The maximum time that each bank can be held active is specified as  $t_{\text{RAS(max)}}$ .

### Bank Activate Command Cycle



### Bank Select

The Bank Select inputs, BA0 and BA1, determine the bank to be used during a Bank Activate, Precharge, Read, or Write operation.

### Bank Selection Bits

BA0	BA1	Bank
0	0	Bank 0
1	0	Bank 1
0	1	Bank 2
1	1	Bank 3



## Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting  $\overline{\text{RAS}}$  high and  $\overline{\text{CAS}}$  low at the clock's rising edge after the necessary  $\overline{\text{RAS}}$  to  $\overline{\text{CAS}}$  delay ( $t_{\text{RCD}}$ ).  $\overline{\text{WE}}$  must also be defined at this time to determine whether the access cycle is a read operation ( $\overline{\text{WE}}$  high), or a write operation ( $\overline{\text{WE}}$  low). The address inputs determine the starting column address.

The SDRAM provides a wide variety of fast access modes. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles up to 133 MHz for PC133 or upto 166MHz for PC166 devices. The number of serial data bits for each access is equal to the burst length, which is programmed into the Mode Register.

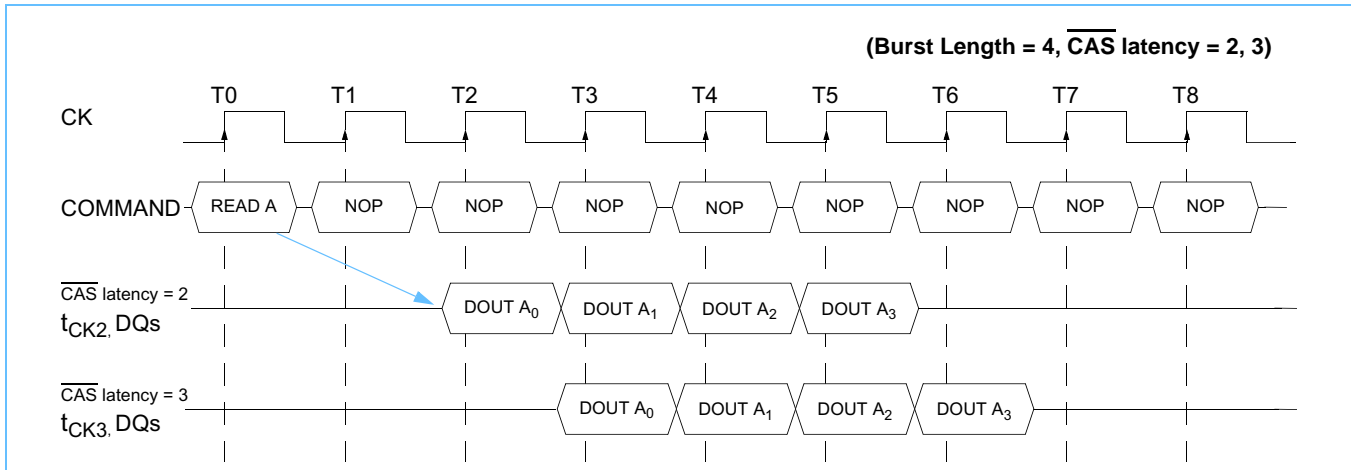
Similar to Page Mode of conventional DRAMs, a read or write cycle can not begin until the sense amplifiers latch the selected row address information. The refresh period ( $t_{\text{REF}}$ ) is what limits the number of random column accesses to an activated bank. A new burst access can be done even before the previous burst ends. The ability to interrupt a burst operation at every clock cycle is supported; this is referred to as the 1-N rule. When the previous burst is interrupted by another Read or Write Command, the remaining addresses are overridden by the new address.

Precharging an active bank after each read or write operation is not necessary providing the same row is to be accessed again. To perform a read or write cycle to a different row within an activated bank, the bank must be precharged and a new Bank Activate command must be issued. When more than one bank is activated, interleaved (ping pong) bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between multiple banks, fast and seamless data access operation among many different pages can be realized. When multiple banks are activated, column to column interleave operation can be done between different pages. Finally, Read or Write Commands can be issued to the same bank or between active banks on every clock cycle.

### Burst Read Command

The Burst Read command is initiated by having  $\overline{CS}$  and  $\overline{CAS}$  low while holding  $\overline{RAS}$  and  $\overline{WE}$  high at the rising edge of the clock. The address inputs determine the starting column address for the burst, the Mode Register sets the type of burst (sequential or interleave) and the burst length (1, 2, 4, 8). The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the  $\overline{CAS}$  latency that is set in the Mode Register.

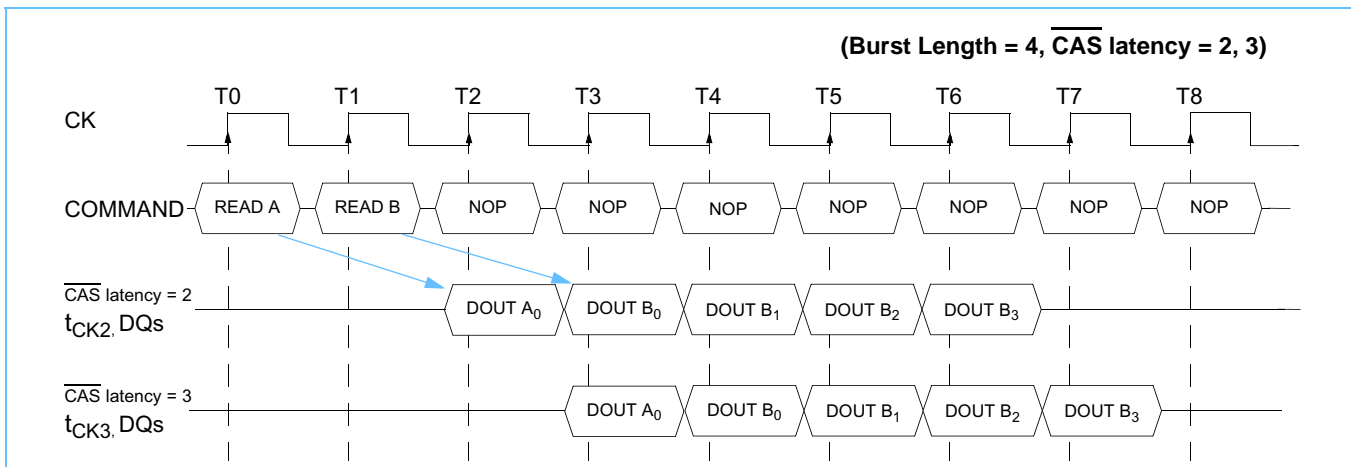
### Burst Read Operation



### Read Interrupted by a Read

A Burst Read may be interrupted before completion of the burst by another Read Command, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the burst length. The data from the first Read Command continues to appear on the outputs until the  $\overline{CAS}$  latency from the interrupting Read Command is satisfied, at this point the data from the interrupting Read Command appears.

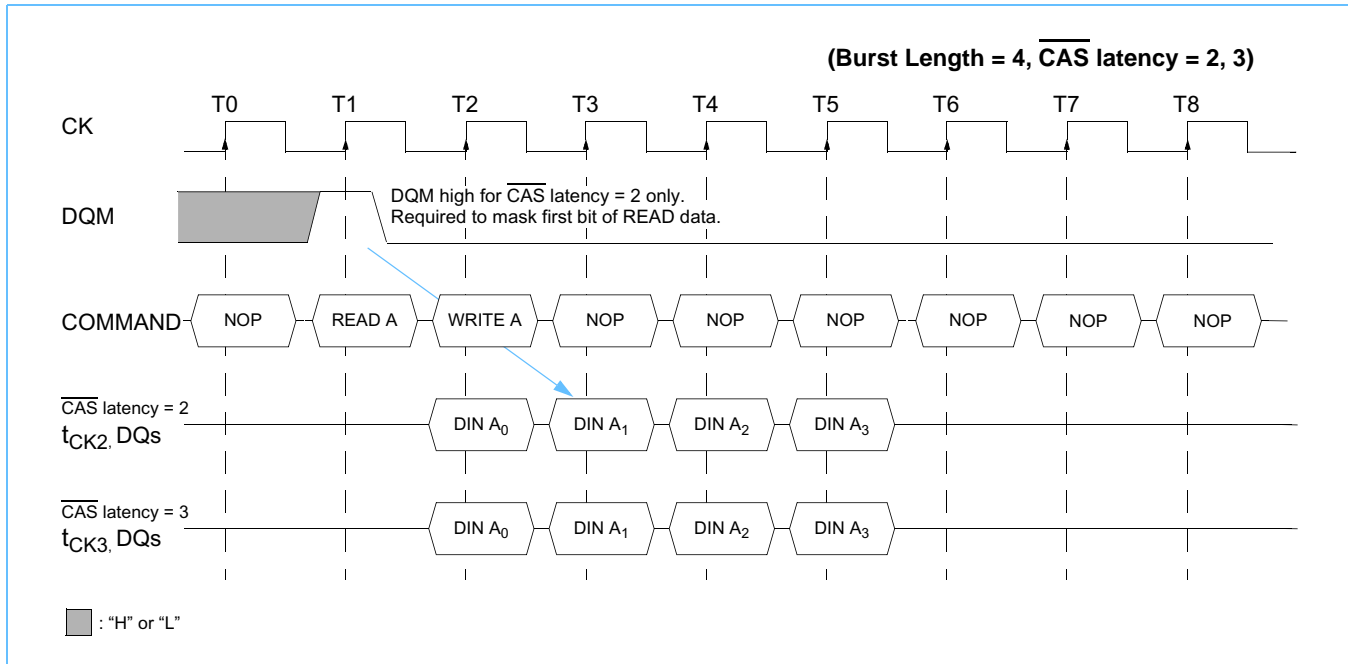
### Read Interrupted by a Read



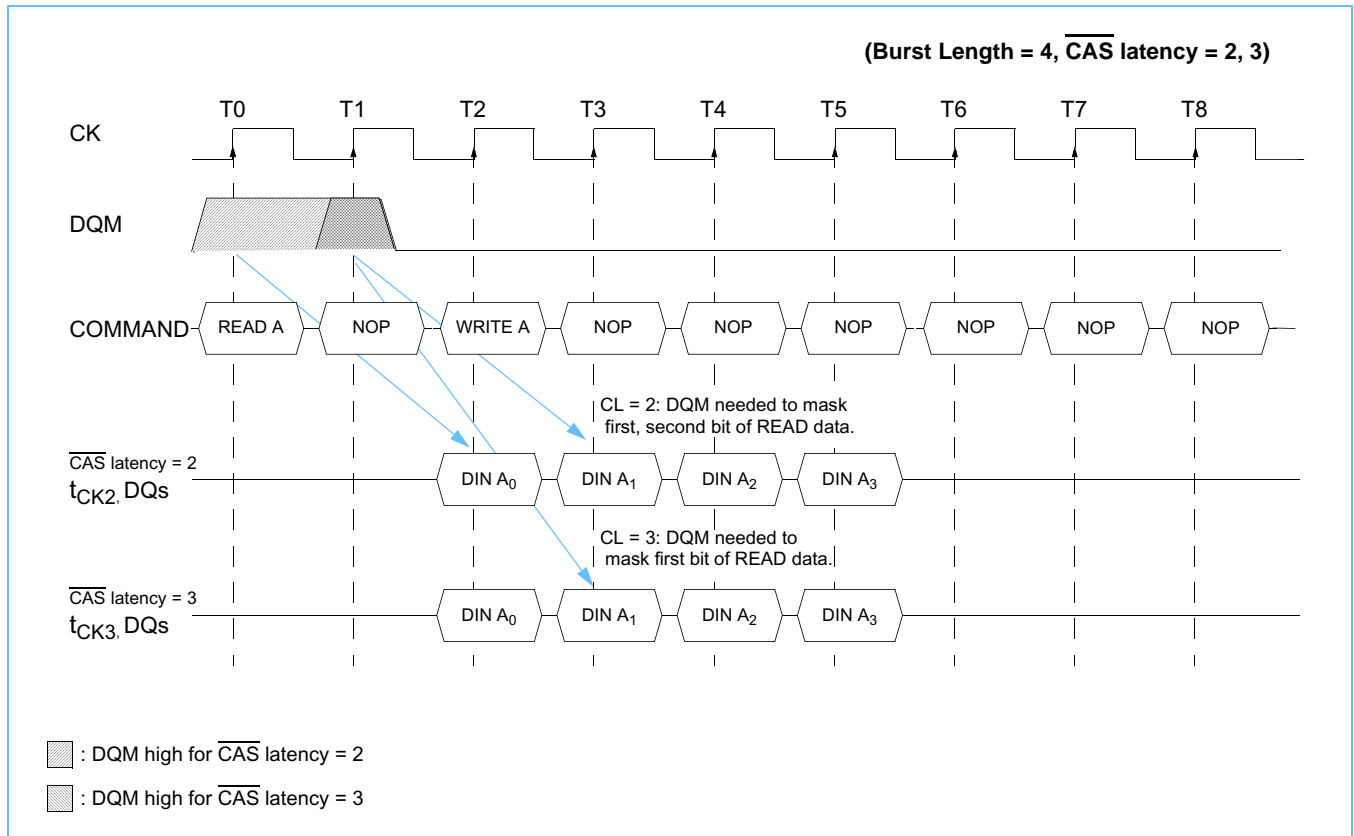
### Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first or second clocks cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus.

### Minimum Read to Write Interval



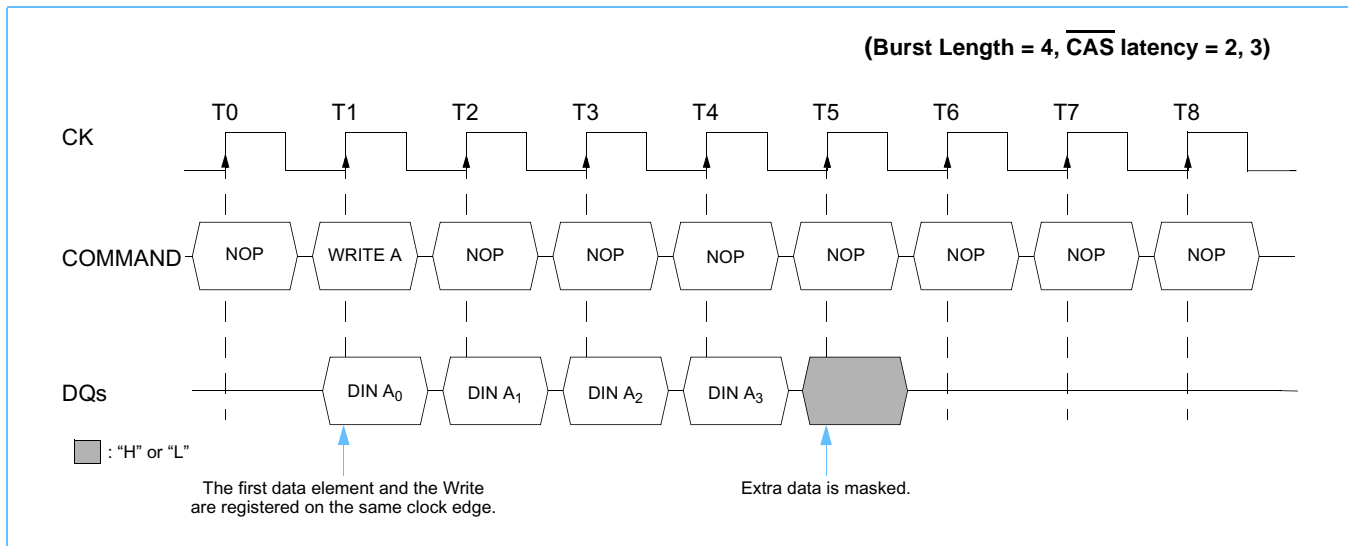
Non-Minimum Read to Write Interval



### Burst Write Command

The Burst Write command is initiated by having  $\overline{CS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  low while holding  $\overline{RAS}$  high at the rising edge of the clock. The address inputs determine the starting column address. There is no  $\overline{CAS}$  latency required for burst write cycles. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

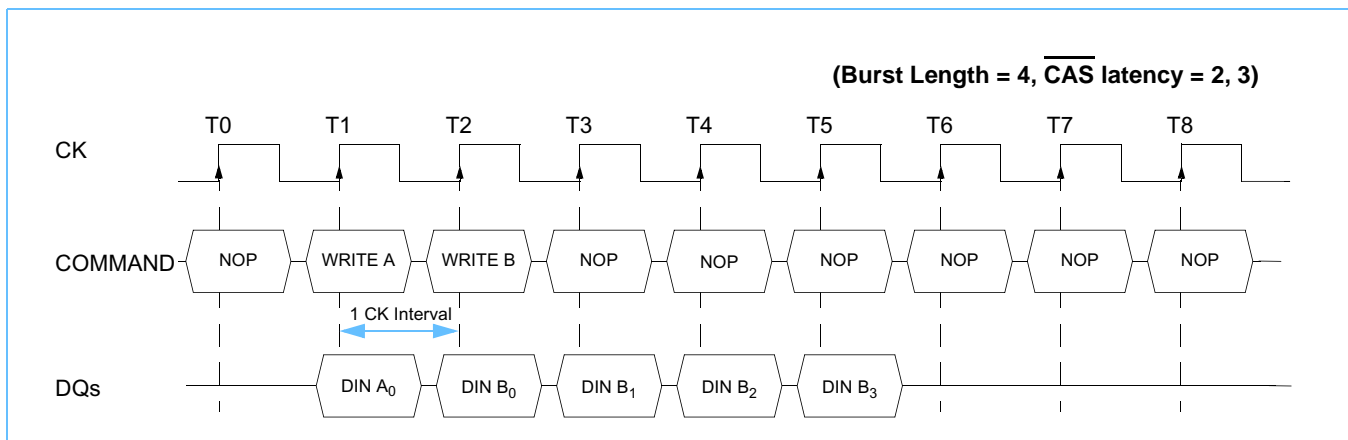
### Burst Write Operation



### Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

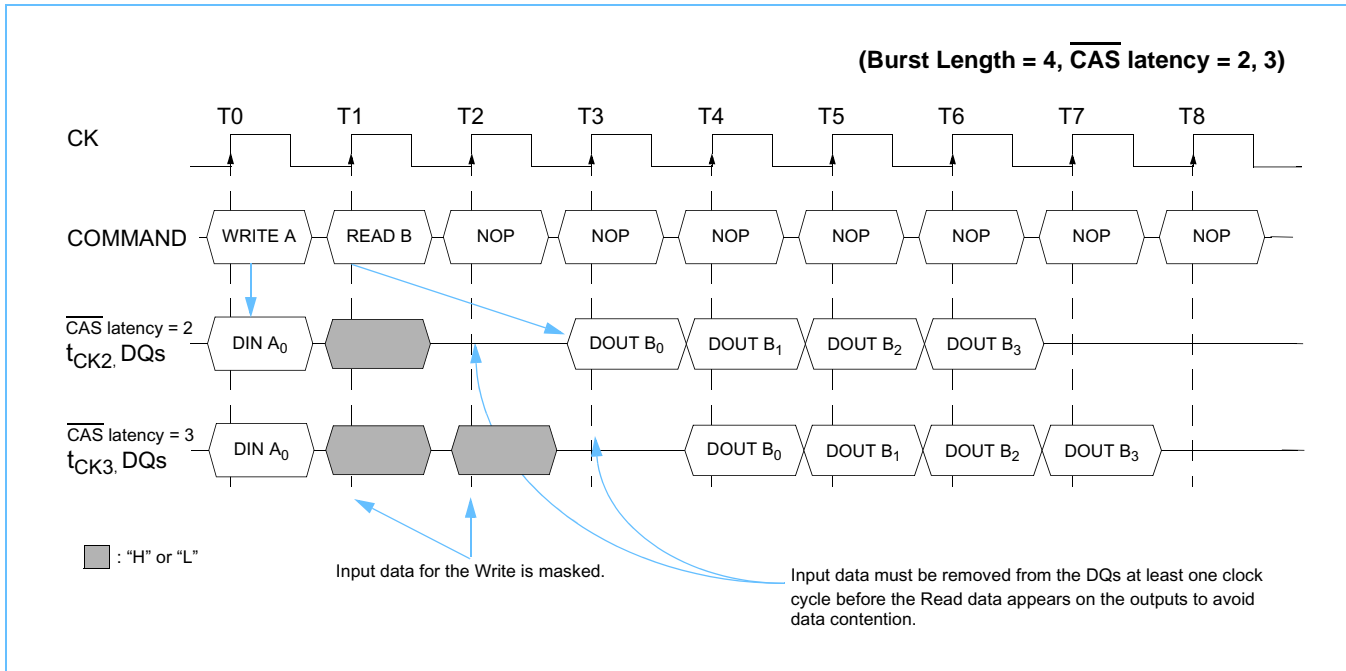
### Write Interrupted by a Write



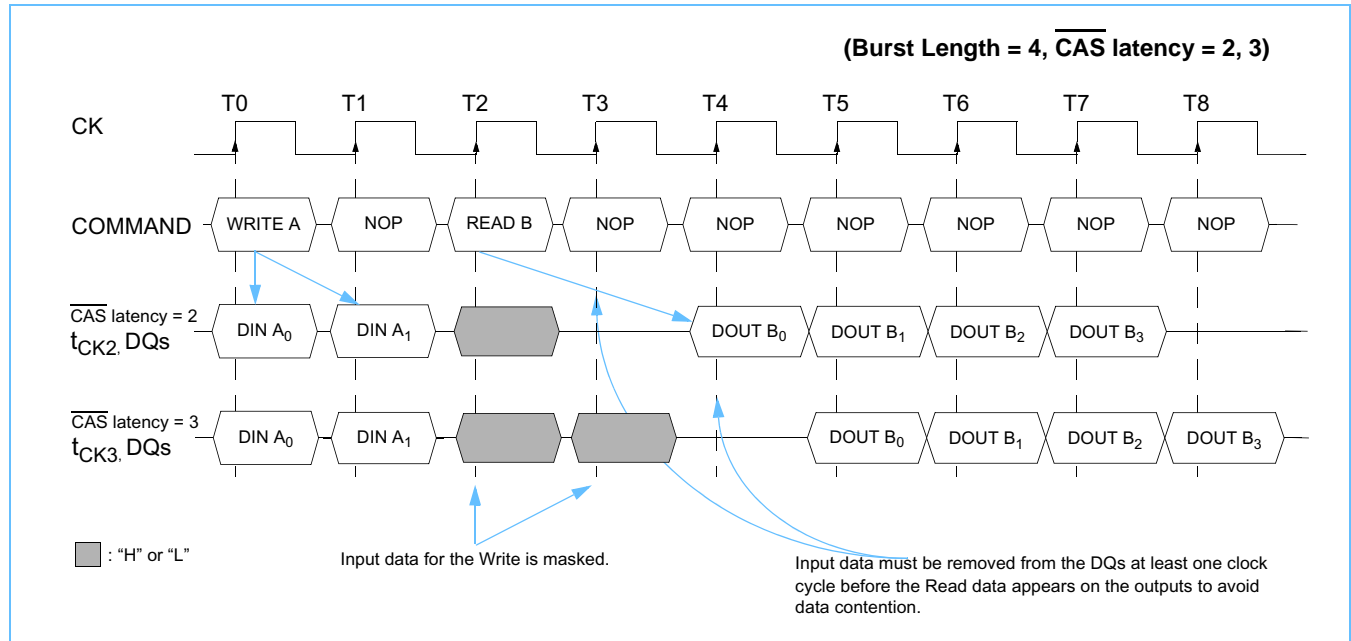
### Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is registered. The DQs must be in the high impedance state at least one cycle before the interrupting read data appears on the outputs to avoid data contention. When the Read Command is registered, any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Read Command is initiated will actually be written to the memory.

### Minimum Write to Read Interval



Non-Minimum Write to Read Interval



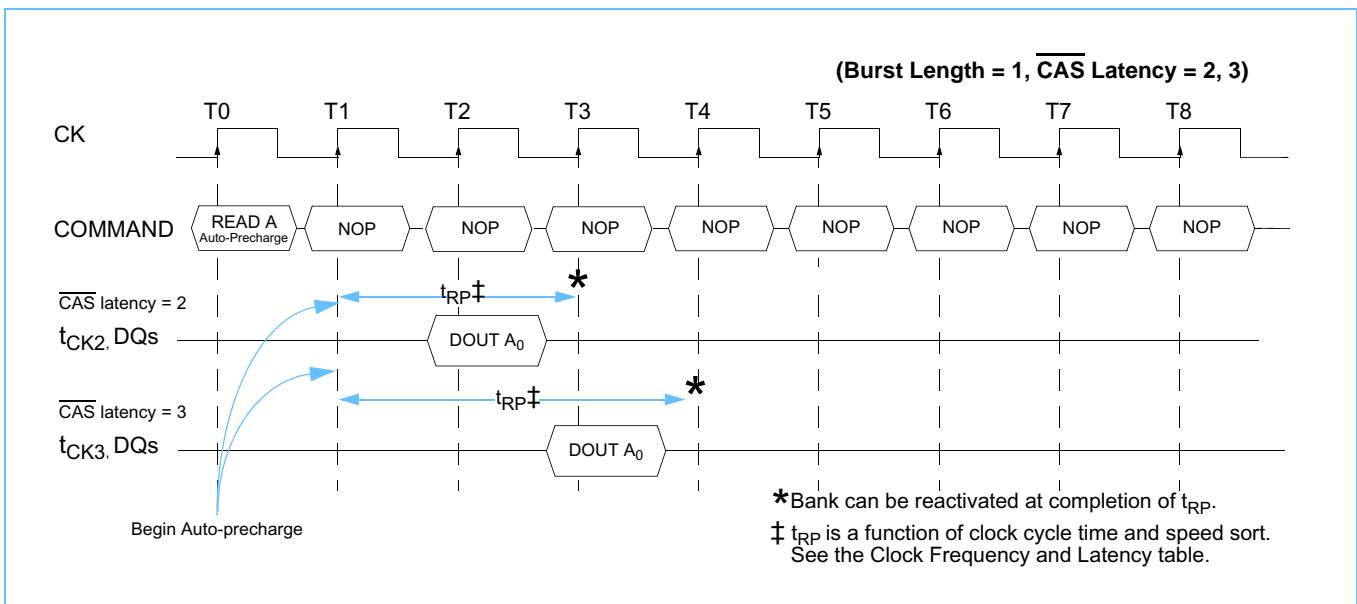
### Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the auto-precharge function. When a Read or a Write Command is given to the SDRAM, the  $\overline{\text{CAS}}$  timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge before all burst read cycles have been completed. Regardless of burst length, the precharge will begin (CAS latency - 1) clocks prior to the last data output. Auto-precharge can also be implemented during Write commands.

A Read or Write Command without auto-precharge can be terminated in the midst of a burst operation. However, a Read or Write Command with auto-precharge cannot be interrupted by a command to the same bank. Therefore use of a Read, Write, or Precharge Command to the same bank is prohibited during a read or write cycle with auto-precharge until the entire burst operation is completed. Once the precharge operation has started the bank cannot be reactivated until the Precharge time ( $t_{RP}$ ) has been satisfied.

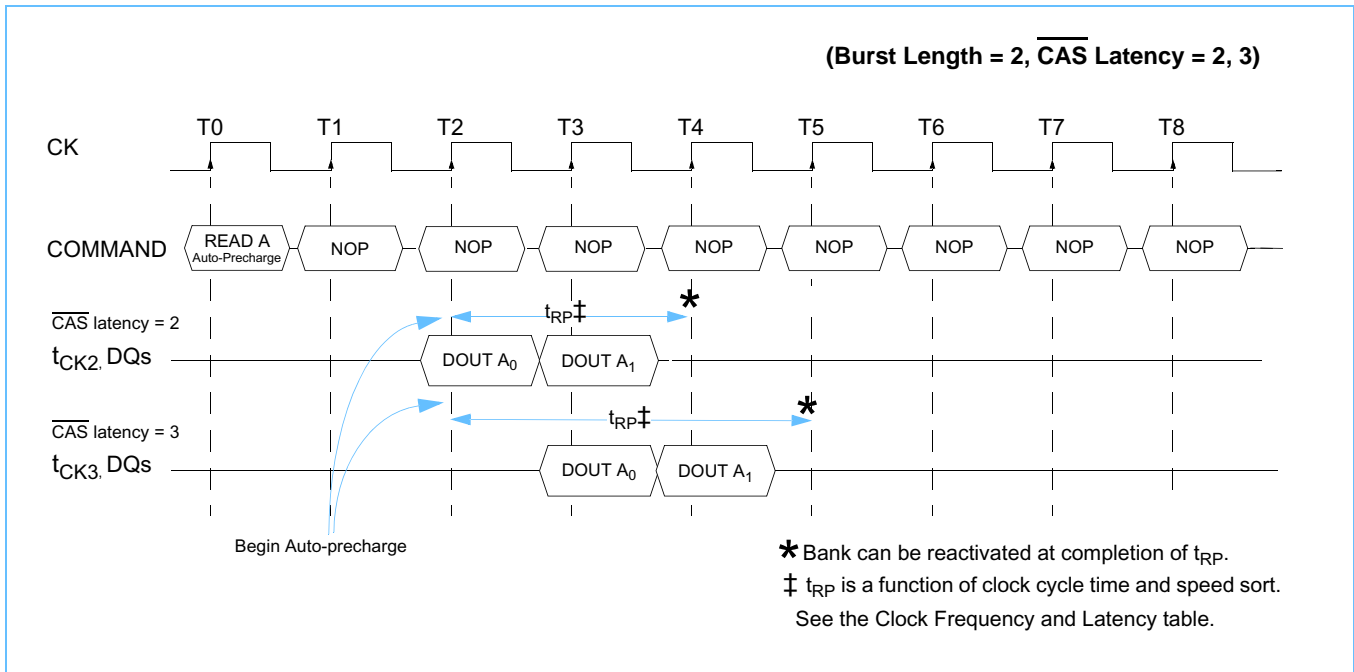
When using the Auto-precharge Command, the interval between the Bank Activate Command and the beginning of the internal precharge operation must satisfy  $t_{RAS(\min)}$ . If this interval does not satisfy  $t_{RAS(\min)}$  then  $t_{RCD}$  must be extended.

### Burst Read with Auto-Precharge

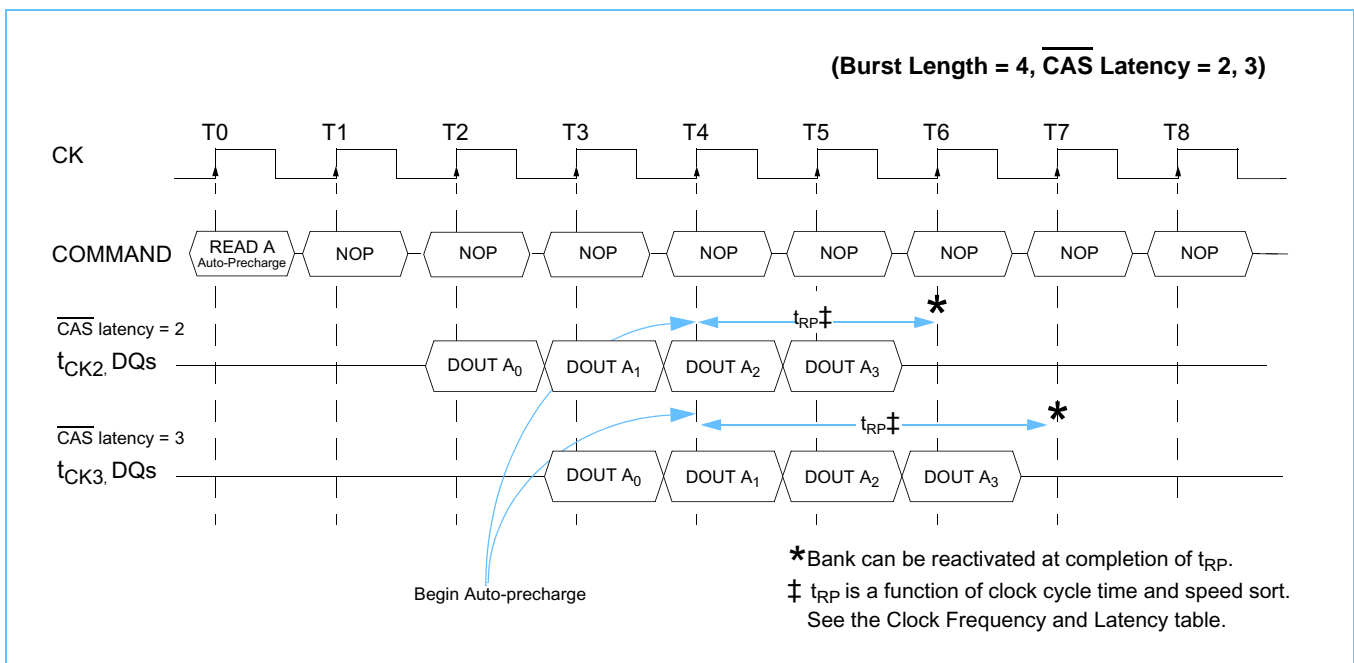




Burst Read with Auto-Precharge

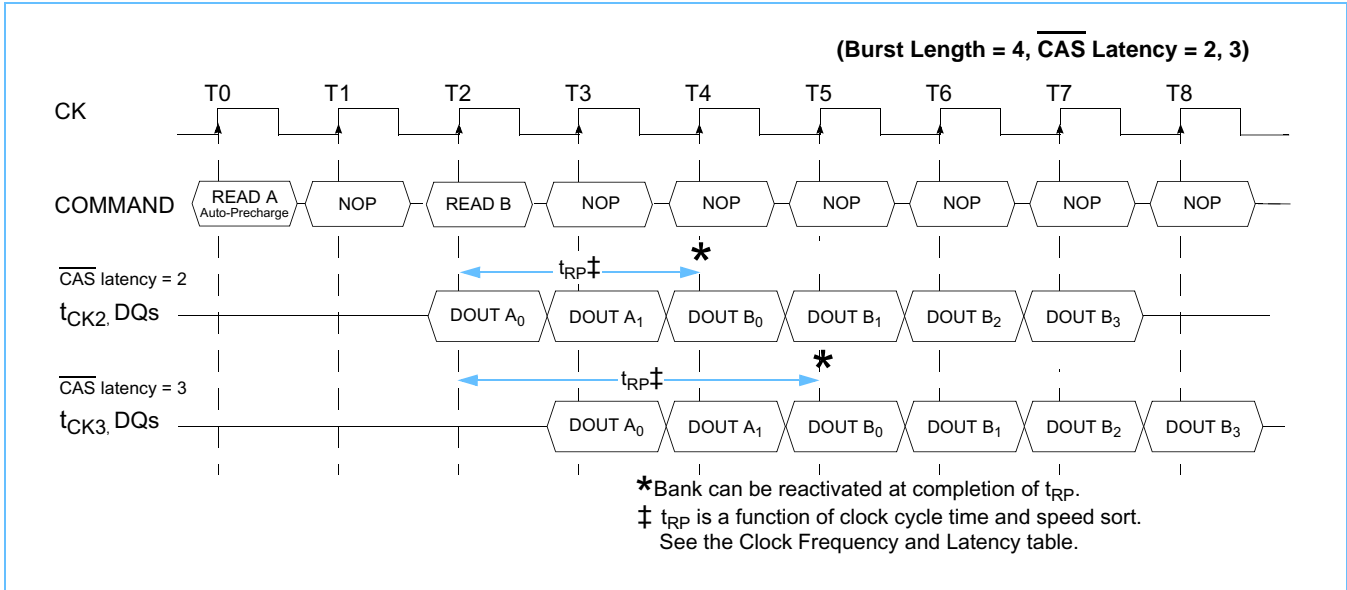


Burst Read with Auto-Precharge



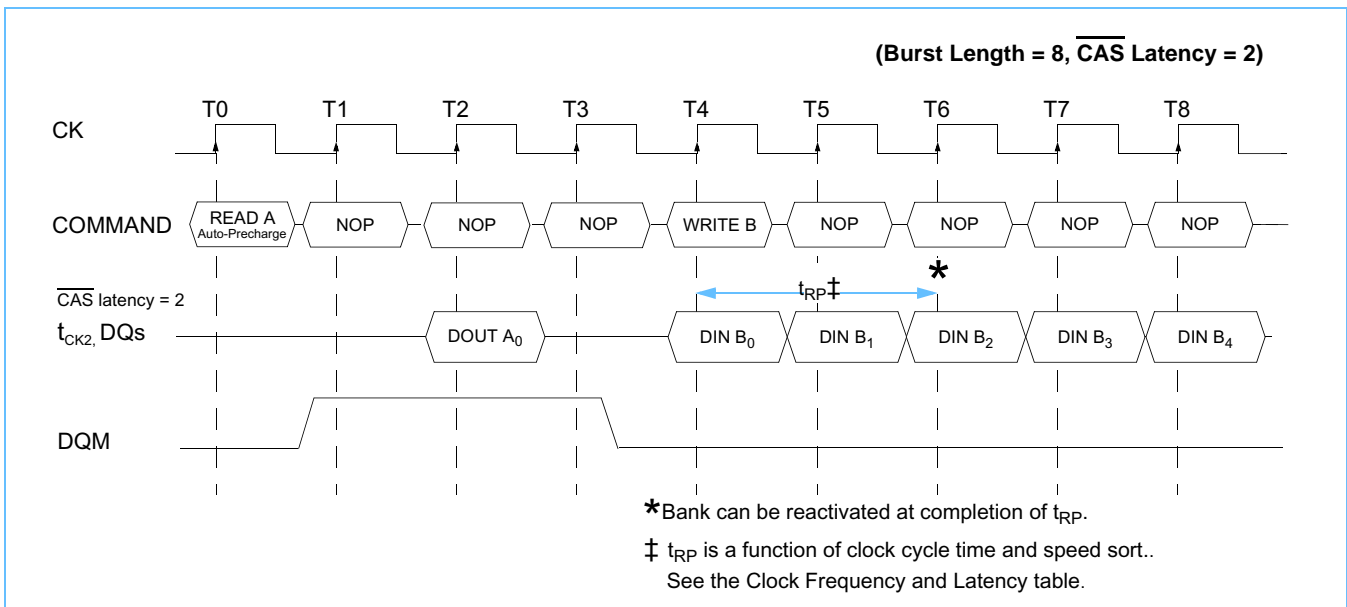
Although a Read Command with auto-precharge can not be interrupted by a command to the same bank, it can be interrupted by a Read or Write Command to a different bank. If the command is issued before auto-precharge begins then the precharge function will begin with the new command. The bank being auto-precharged may be reactivated after the delay  $t_{RP}$ .

### Burst Read with Auto-Precharge Interrupted by Read



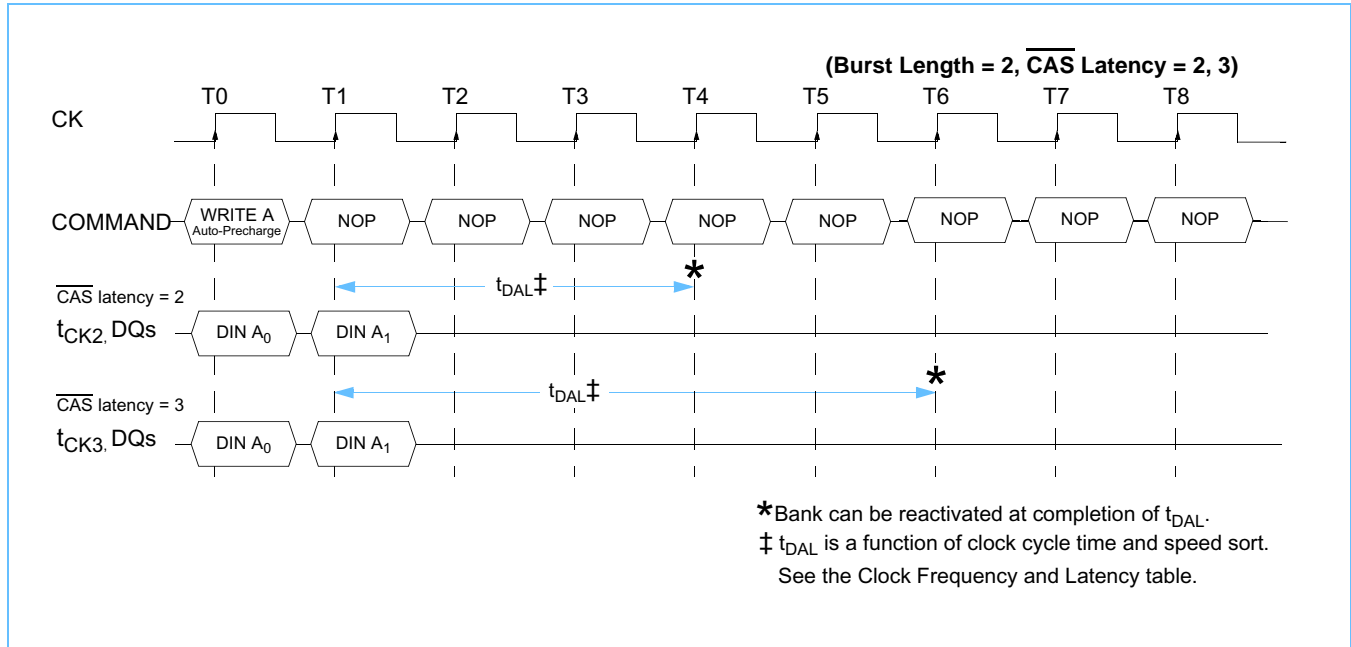
If interrupting a Read Command with auto-precharge with a Write Command, DQM must be used to avoid DQ contention.

### Burst Read with Auto-Precharge Interrupted by Write



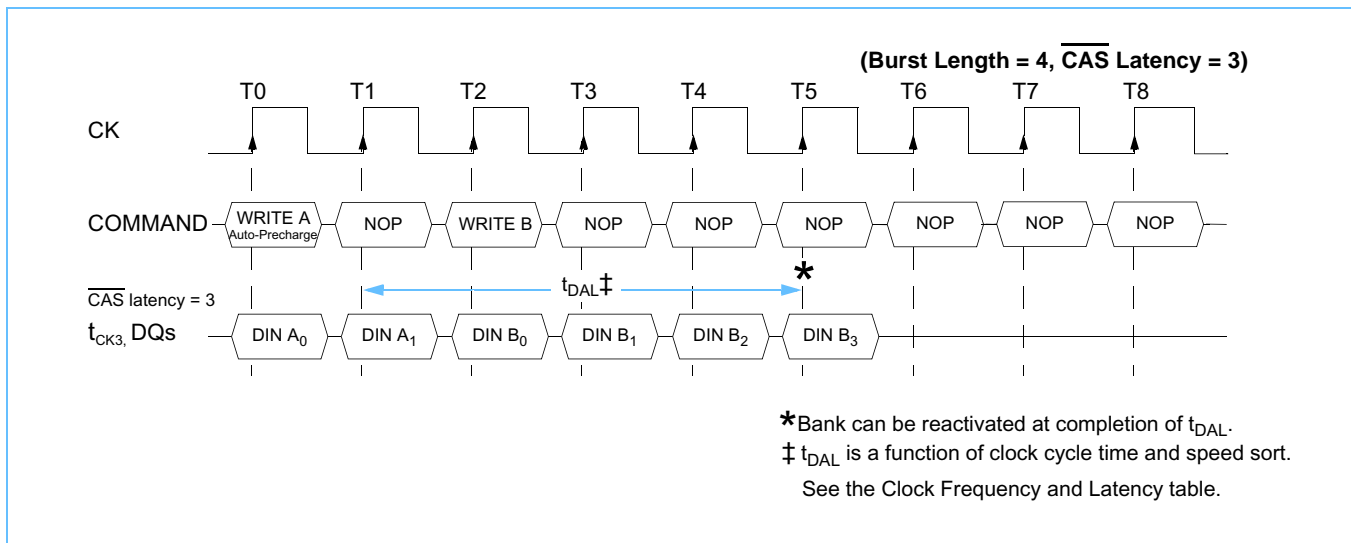
If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The bank undergoing auto-precharge cannot be reactivated until  $t_{DAL}$ , Data-in to Active delay, is satisfied.

### Burst Write with Auto-Precharge

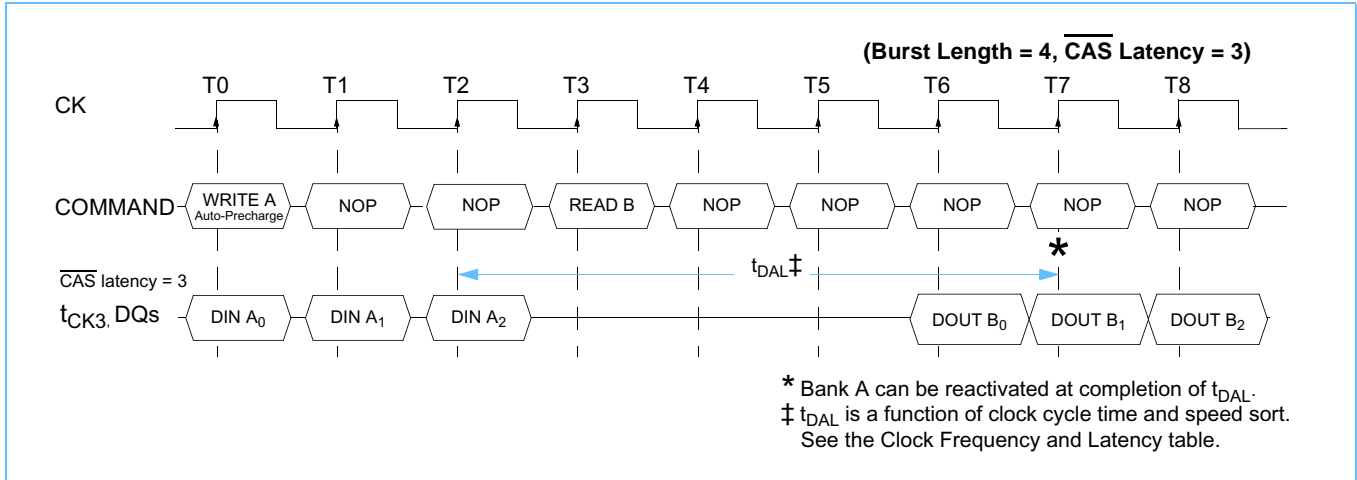


Similar to the Read Command, a Write Command with auto-precharge can not be interrupted by a command to the same bank. It can be interrupted by a Read or Write Command to a different bank, however. The interrupting command will terminate the write. The bank undergoing auto-precharge can not be reactivated until  $t_{DAL}$  is satisfied.

### Burst Write with Auto-Precharge Interrupted by Write



**Burst Write with Auto-Precharge Interrupted by Read**



**Precharge Command**

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when CS, RAS, and WE are low and CAS is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. Three address bits, A10, BA0, and BA1, are used to define which bank(s) is to be precharged when the command is issued.

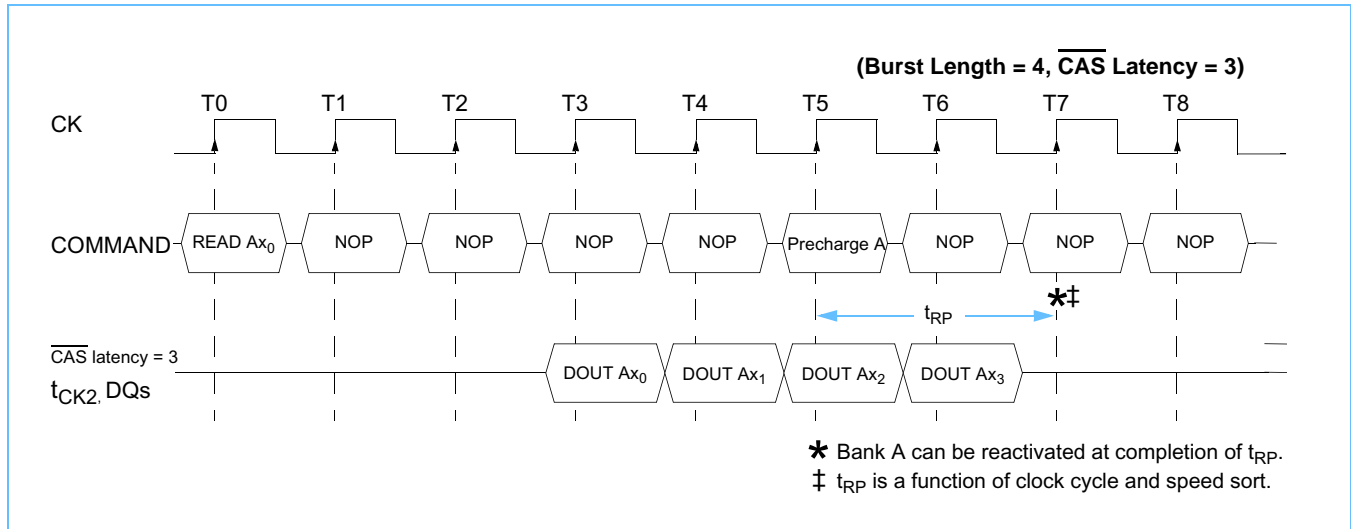
**Bank Selection for Precharge by Address Bits**

A10	Bank Select	Precharged Bank(s)
LOW	BA0, BA1	Single bank defined by BA0, BA1
HIGH	DON'T CARE	All Banks

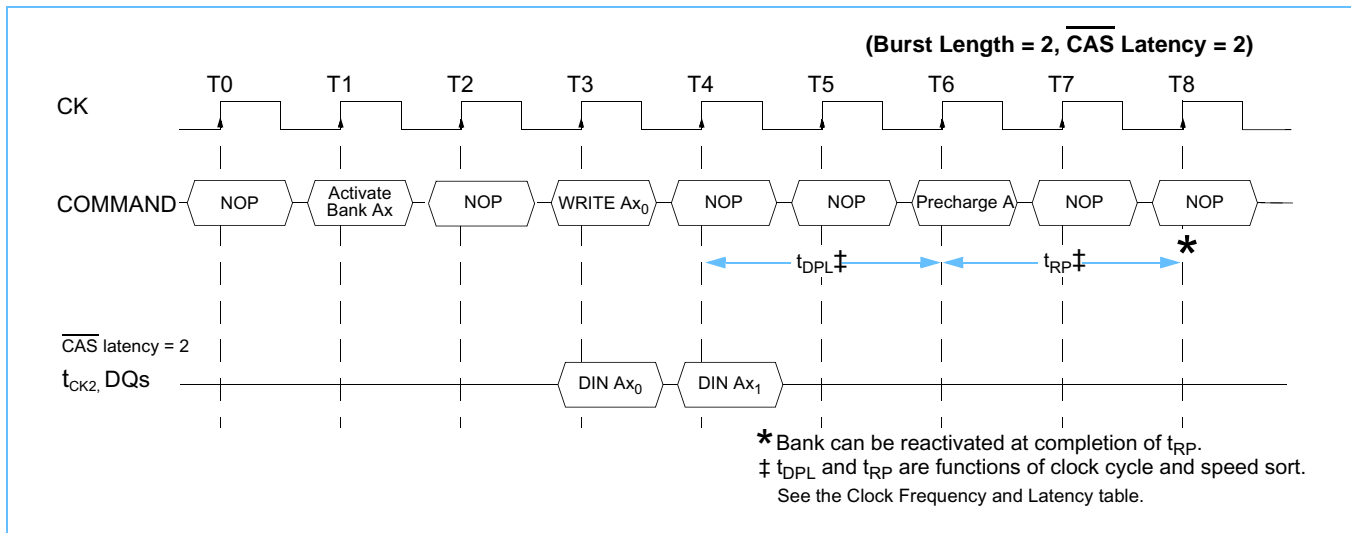
For read cycles, the Precharge Command may be applied ( $\overline{\text{CAS}}$  latency - 1) prior to the last data output. For write cycles, a delay must be satisfied from the start of the last burst write cycle until the Precharge Command can be issued. This delay is known as  $t_{\text{DPL}}$ , Data-in to Precharge delay.

After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time ( $t_{\text{RP}}$ ).

**Burst Read Followed by the Precharge Command**



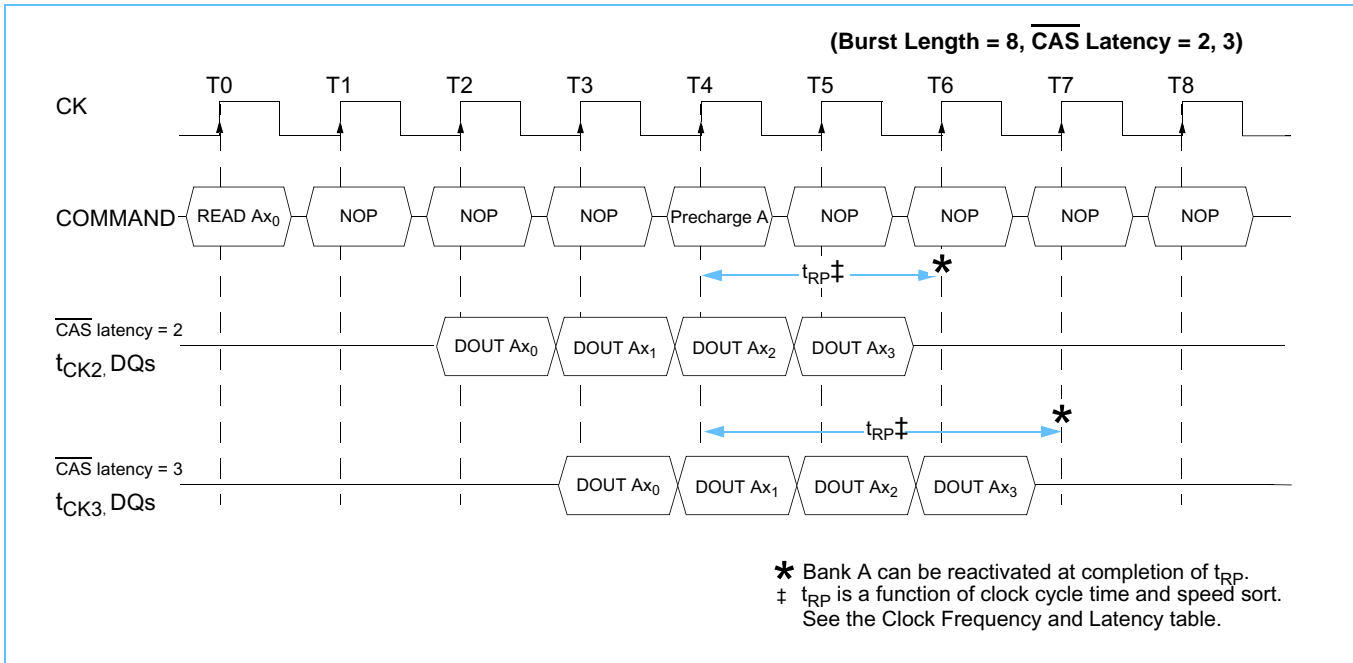
**Burst Write Followed by the Precharge Command**



### Precharge Termination

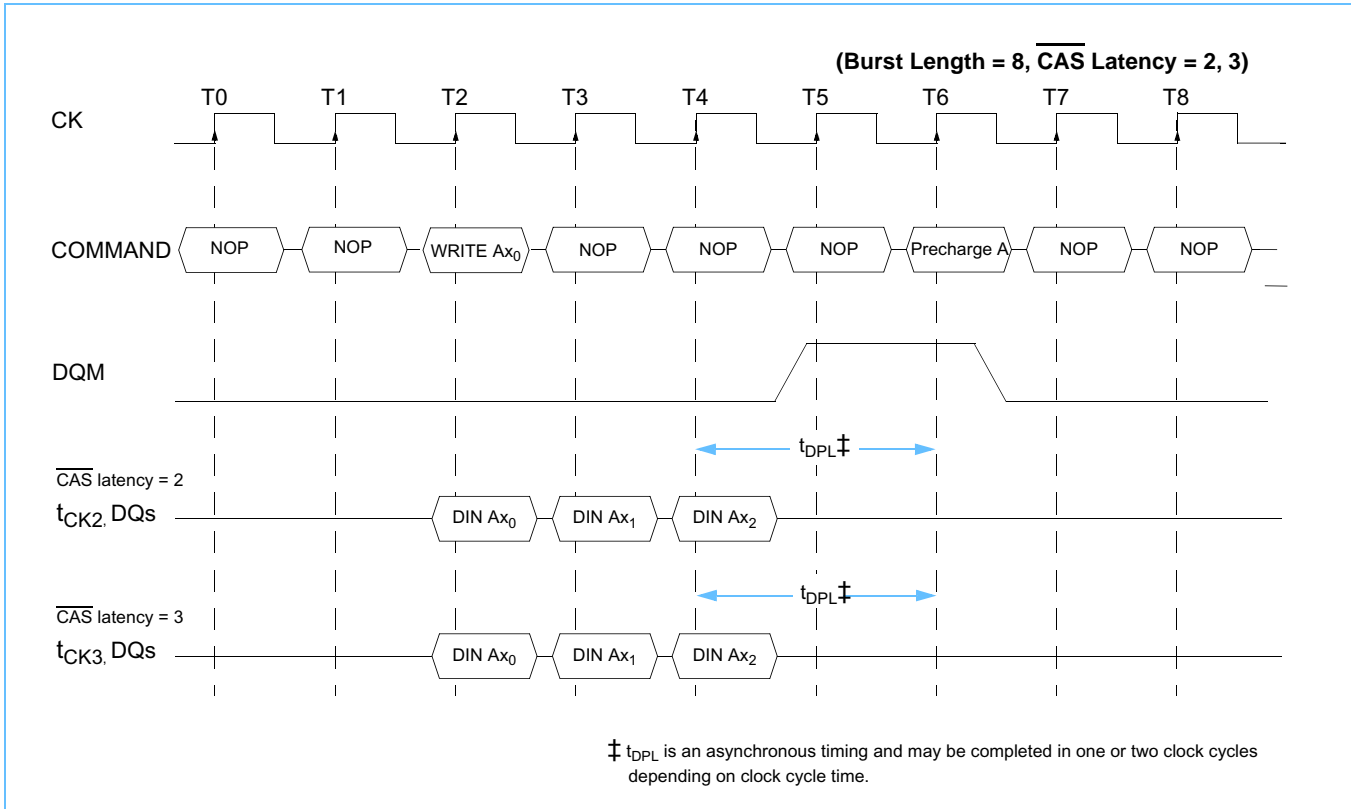
The Precharge Command may be used to terminate either a burst read or burst write operation. When the Precharge command is issued, the burst operation is terminated and bank precharge begins. For burst read operations, valid data will continue to appear on the data bus as a function of CAS Latency.

### Burst Read Interrupted by Precharge



Burst write operations will be terminated by the Precharge command. The last write data that will be properly stored in the device is that write data that is presented to the device a number of clock cycles prior to the Precharge command equal to the Data-in to Precharge delay,  $t_{DPL}$ .

**Precharge Termination of a Burst Write**



## Automatic Refresh Command (CAS before RAS Refresh)

When  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ , and  $\overline{\text{CAS}}$  are held low with  $\overline{\text{CKE}}$  and  $\overline{\text{WE}}$  high at the rising edge of the clock, the chip enters the Automatic Refresh mode (CBR). All banks of the SDRAM must be precharged and idle for a minimum of the Precharge time ( $t_{\text{RP}}$ ) before the Auto Refresh Command (CBR) can be applied. An address counter, internal to the device provides the address during the refresh cycle. No control of the external address pins is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto Refresh Command (CBR) and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the RAS cycle time ( $t_{\text{RC}}$ ).

## Self Refresh Command

The SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , and  $\overline{\text{CKE}}$  held low with  $\overline{\text{WE}}$  high at the rising edge of the clock. All banks must be idle prior to issuing the Self Refresh Command. Once the command is registered,  $\overline{\text{CKE}}$  must be held low to keep the device in Self Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except  $\overline{\text{CKE}}$ , are disabled. The clock is internally disabled during Self Refresh Operation to save power. The user may halt the external clock while the device is in Self Refresh mode, however, the clock must be restarted before the device can exit Self Refresh operation. Once the clock is cycling, the device will exit Self Refresh operation after  $\overline{\text{CKE}}$  is returned high. A minimum delay time is required when the device exits Self Refresh Operation and before the next command can be issued. This delay is equal to the  $\overline{\text{RAS}}$  cycle time ( $t_{\text{RC}}$ ) plus the Self Refresh exit time ( $t_{\text{SREX}}$ ).

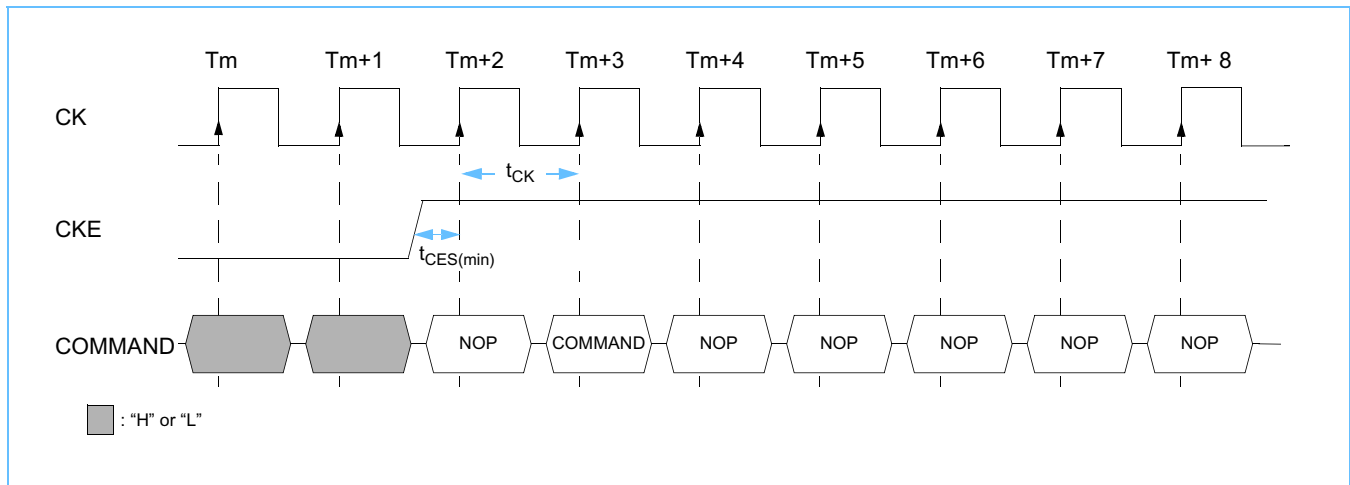


### Power Down Mode

In order to reduce standby power consumption, two power down modes are available: Precharge and Active Power Down mode. To enter Precharge Power Down mode, all banks must be precharged and the necessary precharge delay ( $t_{RP}$ ) must occur before the SDRAM can enter the power down mode. If a bank is activated but not performing a Read or Write operation, Active Power Down mode will be entered. (Issuing a Power Down Mode Command when the device is performing a Read or Write operation causes the device to enter Clock Suspend mode. See the following Clock Suspend section.) Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period ( $t_{REF}$ ) of the device.

The Power Down mode is exited by bringing CKE high. When CKE goes high, a No Operation Command (or Device Deselect Command) is required on the next rising clock edge.

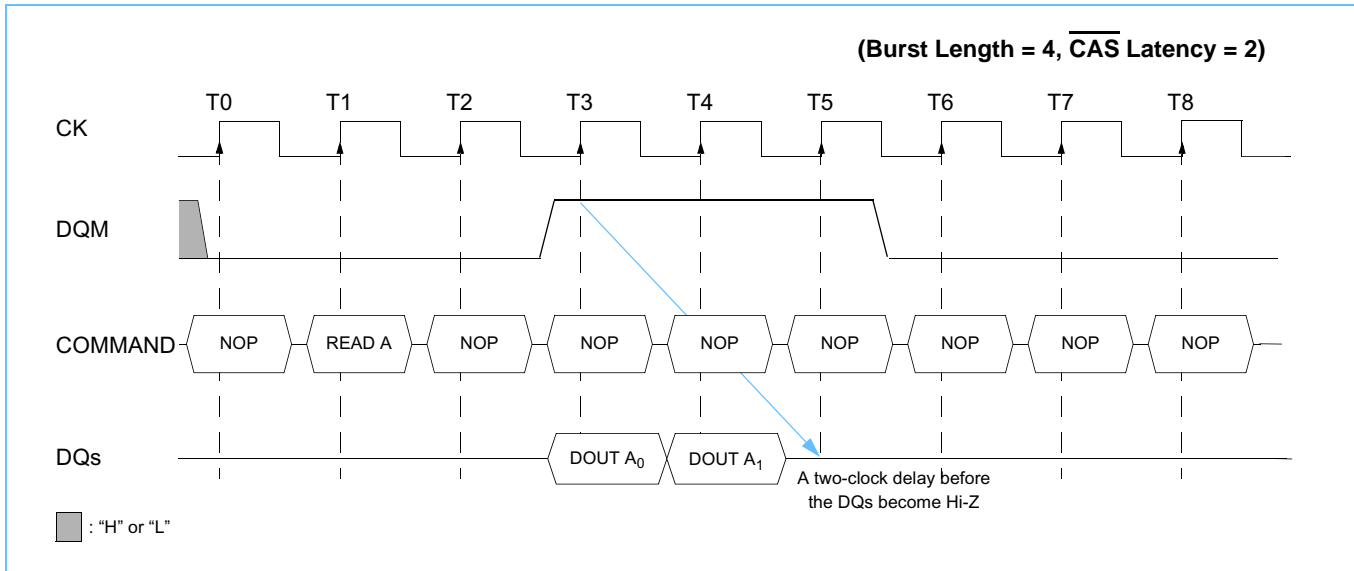
### Power Down Mode Exit Timing



## Data Mask

The SDRAM has a Data Mask function that can be used in conjunction with data read and write cycles. When the Data Mask is activated (DQM high) during a write cycle, the write operation is prohibited immediately (zero clock latency). If the Data Mask is activated during a read cycle, the data outputs are disabled and become high impedance after a two-clock delay, independent of CAS latency.

### Data Mask Activated during a Read Cycle



## No Operation Command

The No Operation Command should be used in cases when the SDRAM is in an idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when  $\overline{\text{CS}}$  is low with  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , and  $\overline{\text{WE}}$  held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

## Deselect Command

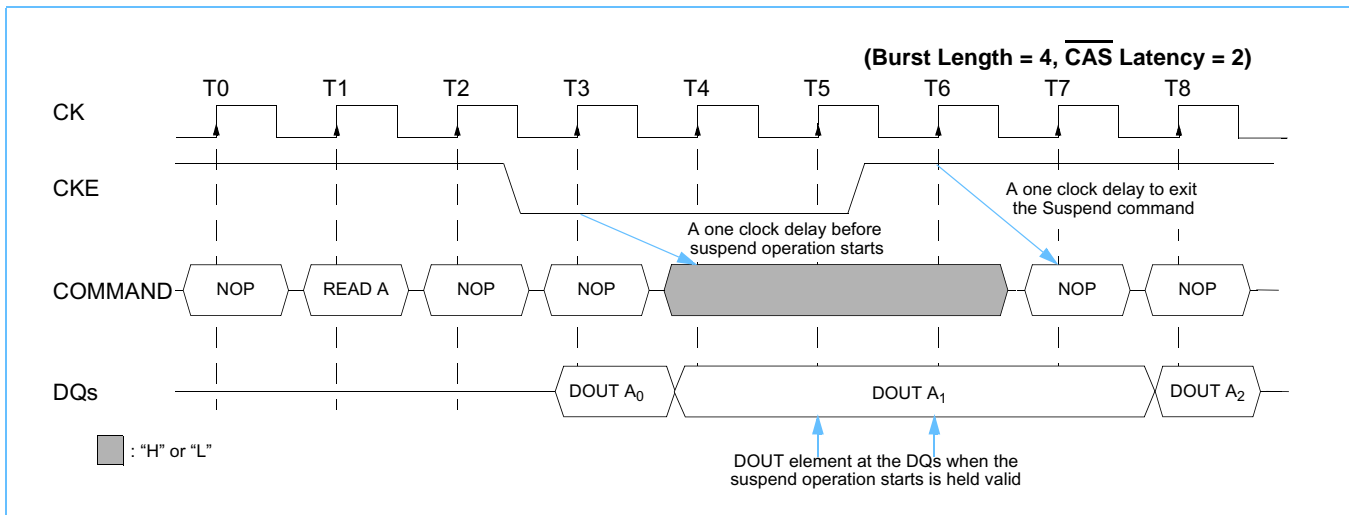
The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when  $\overline{\text{CS}}$  is brought high, the  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , and  $\overline{\text{WE}}$  signals become don't cares.

### Clock Suspend Mode

During normal access mode, CKE is held high, enabling the clock. When CKE is registered low while at least one of the banks is active, Clock Suspend Mode is entered. The Clock Suspend mode deactivates the internal clock and suspends or “freezes” any clocked operation that was currently being executed. There is a one-clock delay between the registration of CKE low and the time at which the SDRAM’s operation suspends. While in Clock Suspend mode, the SDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

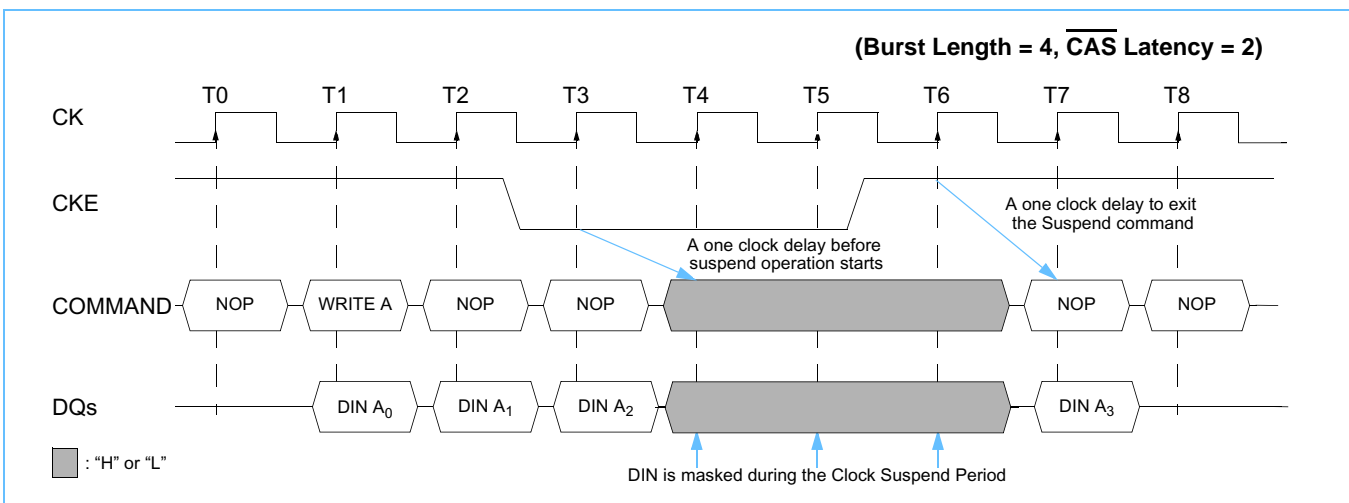
When the operation of the SDRAM is suspended during the execution of a Burst Read operation, the last valid data output onto the DQ pins will be actively held valid until Clock Suspend mode is exited.

### Clock Suspend during a Read Cycle



If Clock Suspend mode is initiated during a burst write operation, the input data is masked and is ignored until the Clock Suspend mode is exited.

### Clock Suspend during a Write Cycle



**Command Truth Table** (See note 1)

Function	Device State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0, BA1	A10	A11, A9-A0	Notes
		Previous Cycle	Current Cycle									
Mode Register Set	Idle	H	X	L	L	L	L	X	OP Code			
Auto (CBR) Refresh	Idle	H	H	L	L	L	H	X	X	X	X	
Entry Self Refresh	Idle	H	L	L	L	L	H	X	X	X	X	
Exit Self Refresh	Idle (Self-Refresh)	L	H	H	X	X	X	X	X	X	X	
				L	H	H	H					
Single Bank Precharge	See Current State Table	H	X	L	L	H	L	X	BS	L	X	2
Precharge all Banks	See Current State Table	H	X	L	L	H	L	X	X	H	X	
Bank Activate	Idle	H	X	L	L	H	H	X	BS	Row Address		2
Write	Active	H	X	L	H	L	L	X	BS	L	Column	2
Write with Auto-Precharge	Active	H	X	L	H	L	L	X	BS	H	Column	2
Read	Active	H	X	L	H	L	H	X	BS	L	Column	2
Read with Auto-Precharge	Active	H	X	L	H	L	H	X	BS	H	Column	2
Reserved		H	X	L	H	H	L	X	X	X	X	
No Operation	Any	H	X	L	H	H	H	X	X	X	X	
Device Deselect	Any	H	X	H	X	X	X	X	X	X	X	
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X	4
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X	
Data Write/Output Enable	Active	H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable	Active	H	X	X	X	X	X	H	X	X	X	
Power Down Mode Entry	Idle/Active	H	L	H	X	X	X	X	X	X	X	6, 7
				L	H	H	H					
Power Down Mode Exit	Any (Power Down)	L	H	H	X	X	X	X	X	X	X	6, 7
				L	H	H	H					

- All of the SDRAM operations are defined by states of  $\overline{CS}$ ,  $\overline{WE}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ , and DQM at the positive rising edge of the clock. Refer to the Current State Truth Table.
- Bank Select (BA0, BA1): BA0, BA1 = 0,0 selects bank 0; BA0, BA1 = 1,0 selects bank 1; BA0, BA1 = 0,1 selects bank 2; BA0, BA1 = 1,1 selects bank 3.
- Not applicable.
- During normal access mode, CKE is held high and CK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
- The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two-clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
- All banks must be precharged before entering the Power Down Mode. (If this command is issued during a burst operation, the device state will be Clock Suspend Mode.) The Power Down Mode does not perform any refresh operations; therefore the device can't remain in this mode longer than the Refresh period ( $t_{REF}$ ) of the device. One clock delay is required for mode entry and exit.
- A No Operation or Device Deselect Command is required on the next clock edge following CKE going high.

## Clock Enable (CKE) Truth Table

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0, BA1	A11 - A0		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down mode exit, all banks idle	2
	L	H	L	X	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	CBR Refresh	
	H	H	L	L	L	L	OP Code		Mode Register Set	4
	H	L	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L	OP Code		Mode Register Set	
L	X	X	X	X	X	X	X	Power Down	4	
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to operations in the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	5
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

1. For the given Current State CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE ( $t_{\text{CES}}$ ) must be satisfied. When exiting power down mode, a NOP command (or Device Deselect Command) is required on the first rising clock after CKE goes high.
3. The address inputs depend on the command that is issued. See the Idle State section of the Current State Truth Table for more information.
4. The Precharge Power Down Mode, the Self Refresh Mode, and the Mode Register Set can only be entered from the all banks idle state.
5. Must be a legal command as defined in the Current State Truth Table.

**Current State Truth Table** (Part 1 of 3)(See note 1)

Current State	Command						Action	Notes	
	CS	RAS	CAS	WE	BA0,BA1	A11 - A0			Description
Idle	L	L	L	L		OP Code	Mode Register Set	Set the Mode Register	2
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	2, 3
	L	L	H	L	BS	X	Precharge	No Operation	
	L	L	H	H	BS	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BS	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BS	Column	Read w/o Precharge	ILLEGAL	4
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	5
Row Active	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Precharge	6
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Start Write; Determine if Auto Precharge	7, 8
	L	H	L	H	BS	Column	Read	Start Read; Determine if Auto Precharge	7, 8
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Terminate Burst; Start the Write cycle	8, 9
	L	H	L	H	BS	Column	Read	Terminate Burst; Start a new Read cycle	8, 9
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Terminate Burst; Start a new Write cycle	8, 9
	L	H	L	H	BS	Column	Read	Terminate Burst; Start the Read cycle	8, 9
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. All Banks must be idle; otherwise, it is an illegal action.
3. If CKE is active (high) the SDRAM will start the Auto (CBR) Refresh operation, if CKE is inactive (low) than the Self Refresh mode is entered.
4. The Current State refers to only one of the banks. If BS selects this bank then the action is illegal. If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6. The minimum and maximum Active time ( $t_{RAS}$ ) must be satisfied.
7. The RAS to CAS Delay ( $t_{RCD}$ ) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time ( $t_{RRD}$ ) is not satisfied.

## Current State Truth Table (Part 2 of 3)(See note 1)

Current State	Command						Action	Notes	
	CS	RAS	CAS	WE	BA0,BA1	A11 - A0			Description
Read with Auto Pre-charge	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	H	X	X	No Operation	Continue the Burst	
Write with Auto Precharge	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
Precharging	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	No Operation; Bank(s) idle after $t_{RP}$	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4
Row Activating	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after $t_{RP}$	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after $t_{RP}$	
	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4, 10
Row Activating	L	H	L	L	BS	Column	Write	ILLEGAL	4
	L	H	L	H	BS	Column	Read	ILLEGAL	4
	L	H	H	H	X	X	No Operation	No Operation; Row Active after $t_{RCD}$	
	H	X	X	X	X	X	Device Deselect	No Operation; Row Active after $t_{RCD}$	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. All Banks must be idle; otherwise, it is an illegal action.
3. If CKE is active (high) the SDRAM will start the Auto (CBR) Refresh operation, if CKE is inactive (low) then the Self Refresh mode is entered.
4. The Current State refers to only one of the banks. If BS selects this bank then the action is illegal. If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6. The minimum and maximum Active time ( $t_{RAS}$ ) must be satisfied.
7. The  $\overline{RAS}$  to  $\overline{CAS}$  Delay ( $t_{RCD}$ ) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time ( $t_{RRD}$ ) is not satisfied.

## Current State Truth Table (Part 3 of 3)(See note 1)

Current State	Command							Action	Notes
	CS	RAS	CAS	WE	BA0,BA1	A11 - A0	Description		
Write Recovering	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Start Write; Determine if Auto Precharge	9
	L	H	L	H	BS	Column	Read	Start Read; Determine if Auto Precharge	9
	L	H	H	H	X	X	No Operation	No Operation; Row Active after $t_{DPL}$	
	H	X	X	X	X	X	Device Deselect	No Operation; Row Active after $t_{DPL}$	
Write Recovering with Auto Pre-charge	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4, 9
	L	H	L	H	BS	Column	Read	ILLEGAL	4, 9
	L	H	H	H	X	X	No Operation	No Operation; Precharge after $t_{DPL}$	
	H	X	X	X	X	X	Device Deselect	No Operation; Precharge after $t_{DPL}$	
Refreshing	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after $t_{RC}$	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after $t_{RC}$	
Mode Register Accessing	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. All Banks must be idle; otherwise, it is an illegal action.
3. If CKE is active (high) the SDRAM will start the Auto (CBR) Refresh operation, if CKE is inactive (low) than the Self Refresh mode is entered.
4. The Current State refers to only one of the banks. If BS selects this bank then the action is illegal. If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6. The minimum and maximum Active time ( $t_{RAS}$ ) must be satisfied.
7. The RAS to CAS Delay ( $t_{RCD}$ ) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time ( $t_{RRD}$ ) is not satisfied.



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V <sub>DD</sub>	Power Supply Voltage	-1.0 to +4.6	V	1
V <sub>DDQ</sub>	Power Supply Voltage for Output	-1.0 to +4.6	V	1
V <sub>IN</sub>	Input Voltage	-0.3 to V <sub>DD</sub> +0.3	V	1
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>DD</sub> +0.3	V	1
T <sub>A</sub>	Operating Temperature (ambient)	0 to +70	°C	1
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C	1
P <sub>D</sub>	Power Dissipation	1.0	W	1
I <sub>OUT</sub>	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions (T<sub>A</sub> = 0°C to 70°C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V <sub>DD</sub>	Supply Voltage	3.0	3.3	3.6	V	1
V <sub>DDQ</sub>	Supply Voltage for Output	3.0	3.3	3.6	V	1
V <sub>IH</sub>	Input High Voltage	2.0	3.0	V <sub>DD</sub> + 0.3	V	1, 2
V <sub>IL</sub>	Input Low Voltage	-1.0	—	0.8	V	1, 3
V <sub>oH</sub>	Output Logic High Voltage	2.4	—	—	V	I <sub>oH</sub> = -2mA
V <sub>IL</sub>	Output Logic Low Voltage	—	—	0.4	V	I <sub>oL</sub> = 2mA

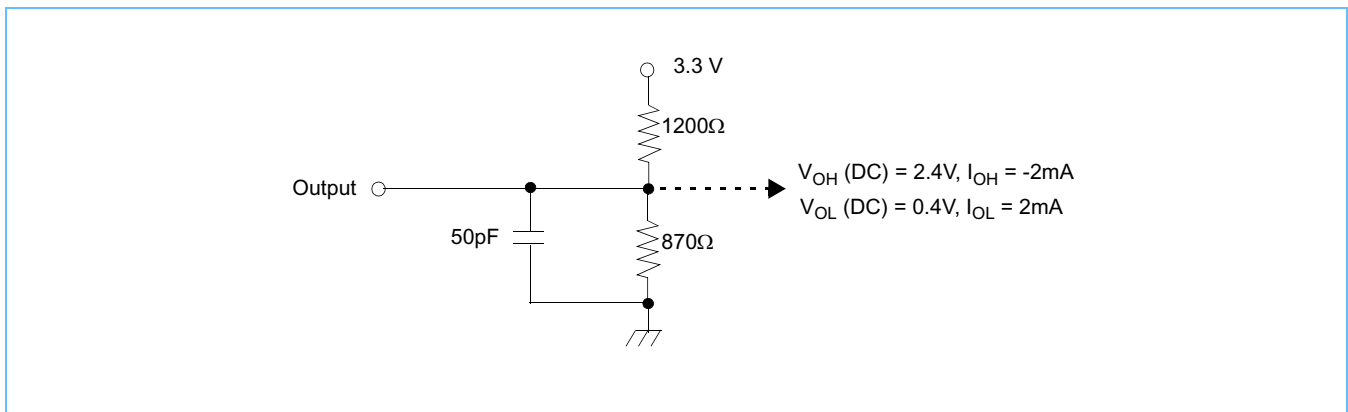
1. All voltages referenced to V<sub>SS</sub> and V<sub>SSQ</sub>.  
 2. V<sub>IH</sub> (max) = V<sub>DD</sub> + 2.3V for pulse width ≤ 3ns.  
 3. V<sub>IL</sub> (min) = V<sub>SS</sub> - 2.0V for pulse width ≤ 3ns.

## Capacitance (T<sub>A</sub> = 25°C, f = 1MHz, V<sub>DD</sub> = 3.3V ± 0.3V)

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
C <sub>I</sub>	Input Capacitance (A0-A11, BA0, BA1, $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{CKE}}$ , DQM)	2.5	3.0	3.8	pF	
	Input Capacitance (CK)	2.5	2.8	3.5	pF	
C <sub>O</sub>	Output Capacitance (DQ0 - DQ15)	4.0	4.5	6.5	pF	

**DC Electrical Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

Symbol	Parameter	Min.	Max.	Units
$I_{I(L)}$	Input Leakage Current, any input ( $0.0\text{V} \leq V_{IN} \leq V_{DD}$ ), All Other Pins Not Under Test = $0\text{V}$	-1	+1	$\mu\text{A}$
$I_{O(L)}$	Output Leakage Current ( $D_{OUT}$ is disabled, $0.0\text{V} \leq V_{OUT} \leq V_{DDQ}$ )	-1	+1	$\mu\text{A}$
$V_{OH}$	Output Level (LVTTL) Output "H" Level Voltage ( $I_{OUT} = -2.0\text{mA}$ )	2.4	—	V
$V_{OL}$	Output Level (LVTTL) Output "L" Level Voltage ( $I_{OUT} = +2.0\text{mA}$ )	—	0.4	V

**DC Output Load Circuit**

dc

**Operating, Standby, and Refresh Currents**(T<sub>A</sub> = 0 to +70°C)

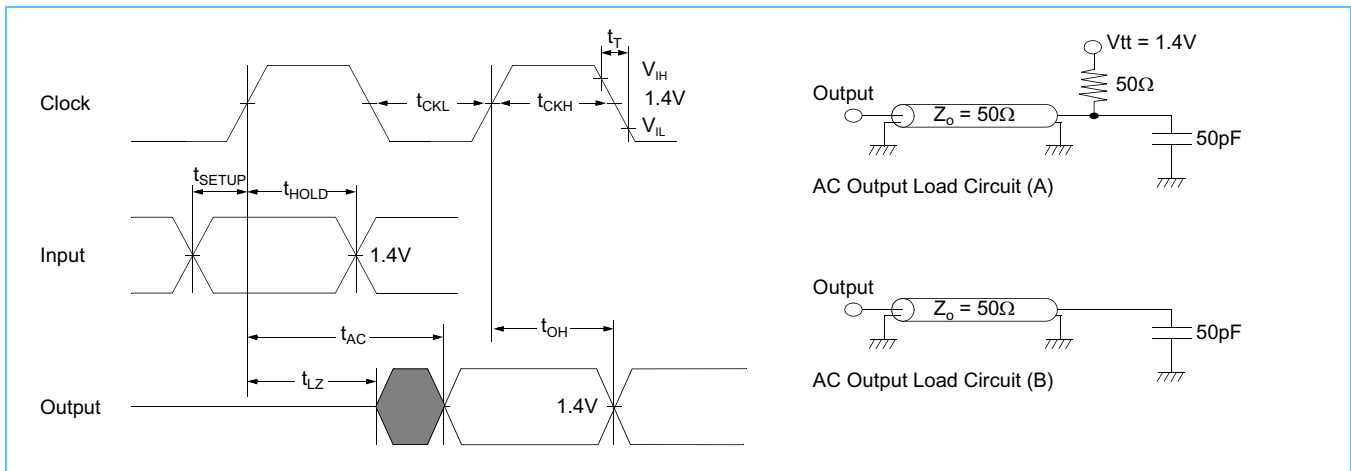
Parameter	Symbol	Test Condition	Speed (3.3V)		Units	Notes
			-7	-75		
Operating Current	I <sub>CC1</sub>	1 bank operation t <sub>RC</sub> = t <sub>RC</sub> (min), t <sub>CK</sub> = min Active-Precharge command cycling without burst operation	95	85	mA	1, 2, 3
Precharge Standby Current in Power Down Mode	I <sub>CC2P</sub>	$\overline{CKE} \leq V_{IL}(\text{max}), t_{CK} = \text{min},$ $\overline{CS} = V_{IH}(\text{min})$	2.5	2.5	mA	1
	I <sub>CC2PS</sub>	$\overline{CKE} \leq V_{IL}(\text{max}), t_{CK} = \text{Infinity},$ $\overline{CS} = V_{IH}(\text{min})$	2.5	2.5	mA	1
Precharge Standby Current in Non-Power Down Mode	I <sub>CC2N</sub>	$CKE \geq V_{IH}(\text{min}), t_{CK} = \text{min},$ $\overline{CS} = V_{IH}(\text{min})$	35	45	mA	1, 5
	I <sub>CC2NS</sub>	$CKE \geq V_{IH}(\text{min}), t_{CK} = \text{Infinity},$	9	9	mA	1, 7
No Operating Current (Active state: 4 bank)	I <sub>CC3N</sub>	$CKE \geq V_{IH}(\text{min}), t_{CK} = \text{min},$ $\overline{CS} = V_{IH}(\text{min})$	40	50	mA	1, 5
	I <sub>CC3P</sub>	$CKE \leq V_{IL}(\text{max}), t_{CK} = \text{min},$	9	9	mA	1, 6
Operating Current (Burst Mode)	I <sub>CC4</sub>	t <sub>CK</sub> = min, Read/ Write command cycling, Multiple banks active, gapless data, BL = 4	90	120	mA	1, 3, 4
Auto (CBR) Refresh Current	I <sub>CC5</sub>	t <sub>CK</sub> = min, t <sub>RC</sub> = t <sub>RC</sub> (min) CBR command cycling	170	190	mA	1
Self Refresh Current	I <sub>CC6</sub>	CKE ≤ 0.2V	3	3	mA	1

1. Currents given are valid for a single device. .
2. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t<sub>CK</sub> and t<sub>RC</sub>. Input signals are changed up to three times during t<sub>RC</sub>(min).
3. The specified values are obtained with the output open.
4. Input signals are changed once during t<sub>CK</sub>(min).
5. Input signals are changed once during three clock cycles.
6. Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).
7. Input signals are stable.

**AC Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

1. An initial pause of  $200\mu\text{s}$ , with DQM and CKE held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of two Auto (CBR) Refresh cycles before or after the Mode Register Set operation.
2. The Transition time is measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ )
3. In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
4. Load Circuit A: AC timing tests have  $V_{IL} = 0.4\text{V}$  and  $V_{IH} = 2.4\text{V}$  with the timing referenced to the  $1.40\text{V}$  crossover point
5. Load Circuit A: AC measurements assume  $t_T = 1.0\text{ns}$ .
6. Load Circuit B: AC timing tests have  $V_{IL} = 0.8\text{V}$  and  $V_{IH} = 2.0\text{V}$  with the timing referenced to the  $1.40\text{V}$  crossover point
7. Load Circuit B: AC measurements assume  $t_T = 1.2\text{ns}$ .

**AC Characteristics Diagrams**



## Clock and Clock Enable Parameters

Symbol	Parameter	-7		-75		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{CK3}$	Clock Cycle Time, CAS Latency = 3	7.0	1000	7.5	1000	ns	
$t_{CK2}$	Clock Cycle Time, CAS Latency = 2	7.5	1000	10	1000	ns	
$t_{AC3(A)}$	Clock Access Time, CAS Latency = 3	—	—	—	—	ns	1
$t_{AC2(A)}$	Clock Access Time, CAS Latency = 2	—	—	—	—	ns	1
$t_{AC3(B)}$	Clock Access Time, CAS Latency = 3	—	5	—	5.4	ns	2
$t_{AC2(B)}$	Clock Access Time, CAS Latency = 2	—	5.4	—	6	ns	2
$t_{CKH}$	Clock High Pulse Width	2	—	2.5	—	ns	
$t_{CKL}$	Clock Low Pulse Width	2	—	2.5	—	ns	
$t_{CES}$	Clock Enable Set-up Time	1.5	—	1.5	—	ns	
$t_{CEH}$	Clock Enable Hold Time	1.0	—	0.8	—	ns	
$t_{SB}$	Power down mode Entry Time	0	6	0	7.5	ns	
$t_T$	Transition Time (Rise and Fall)	0.3	8	0.5	10	ns	

1. Access time is measured at 1.4V. See AC Characteristics: notes 1, 2, 3, 4, 5 and load circuit A.
2. Access time is measured at 1.4V. See AC Characteristics: notes 1, 2, 3, 6, 7 and load circuit B.

## Common Parameters

Symbol	Parameter	-7		-75		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{CS}$	Command Setup Time	1.5	—	1.5	—	ns	
$t_{CH}$	Command Hold Time	0.8	—	0.8	—	ns	
$t_{AS}$	Address and Bank Select Set-up Time	1.5	—	1.5	—	ns	
$t_{AH}$	Address and Bank Select Hold Time	0.8	—	0.8	—	ns	
$t_{RCD}$	RAS to CAS Delay	16	—	20	—	ns	1
$t_{RC}$	Bank Cycle Time	54	—	67.5	—	ns	1
$t_{RAS}$	Active Command Period	36	100K	45	100K	ns	1
$t_{RP}$	Precharge Time	16	—	20	—	ns	1
$t_{RRD}$	Bank to Bank Delay Time	12	—	15	—	ns	1
$t_{CCD}$	CAS to CAS Delay Time	1	—	1	—	CK	

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows:  
the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

## Mode Register Set Cycle

Symbol	Parameter	-7		-75		Units
		Min.	Max.	Min.	Max.	
$t_{RSC}$	Mode Register Set Cycle Time	12	—	15	—	ns

## Read Cycle

Symbol	Parameter	-7		-75		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{OH}$	Data Out Hold Time	—	—	—	—	ns	1
		2.5	—	2.7	—	ns	2, 4
$t_{LZ}$	Data Out to Low Impedance Time	0	—	0	—	ns	
$t_{HZ}$	Data Out to High Impedance Time	3	6	3	7	ns	3
$t_{DQZ}$	DQM Data Out Disable Latency	2	—	2	—	CK	

1. AC Output Load Circuit A.
2. AC Output Load Circuit B.
3. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.
4. Data Out Hold Time with no load must meet 1.8ns (-75H, -75D, -75A).

## Refresh Cycle

Symbol	Parameter	-7		-75		Units	Notes
		Min.	Max.	Min.	Max.		
$t_{REF}$	Refresh Period	—	64	—	64	ms	1
$t_{SREX}$	Self Refresh Exit Time	1	—	1	—	CK	

1. 4096 auto refresh cycles.

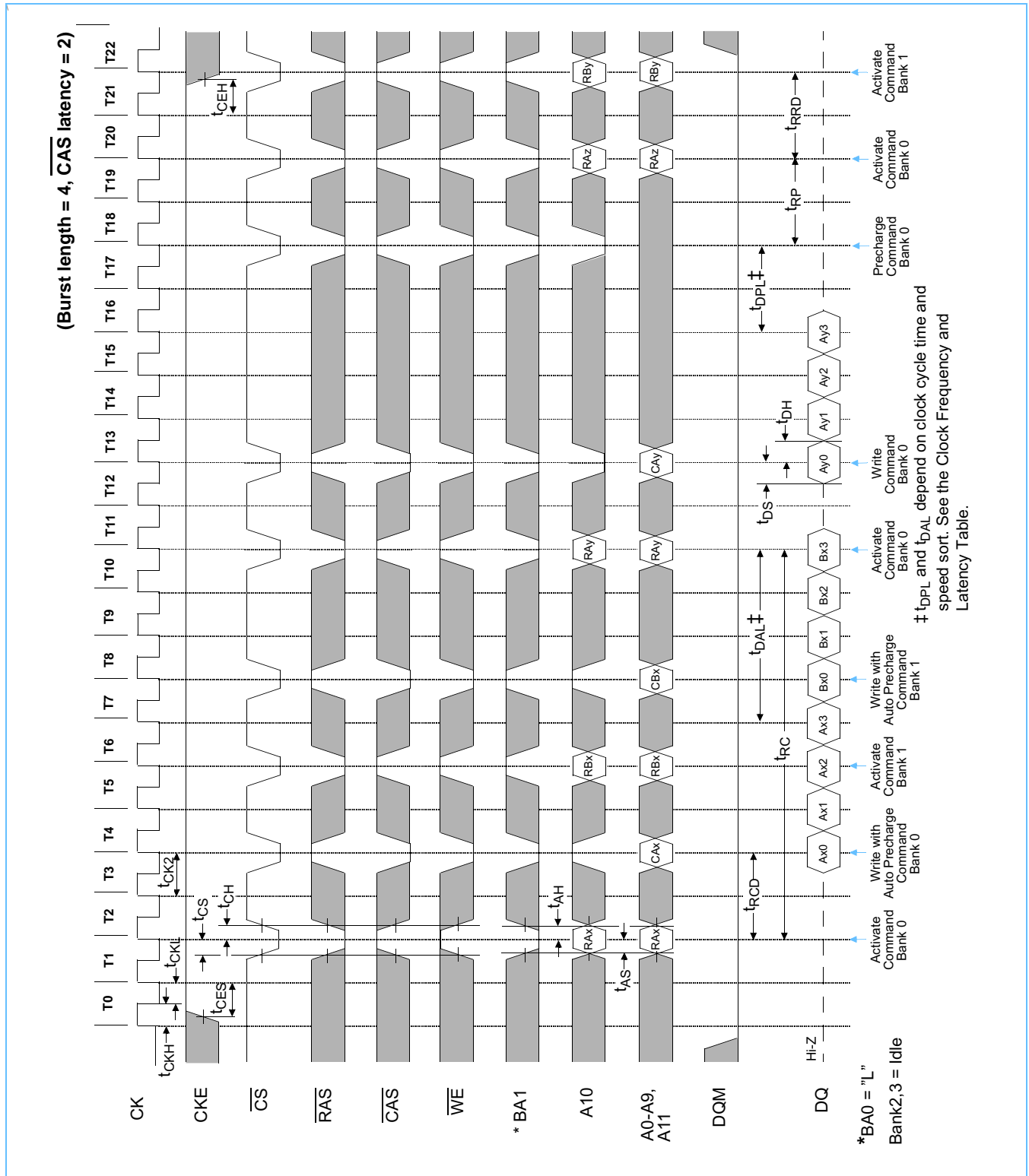
## Write Cycle

Symbol	Parameter	-7		-75		Units
		Min.	Max.	Min.	Max.	
$t_{DS}$	Data In Set-up Time	1.5	—	1.5	—	ns
$t_{DH}$	Data In Hold Time	0.8	—	0.8	—	ns
$t_{DPL}$	Data input to Precharge	12	—	15	—	ns
$t_{WR}$	Write Recovery Time	12	—	15	—	ns
$t_{DAL3}$	Data In to Active Delay CAS Latency = 3	5	—	5	—	CK
$t_{DAL2}$	Data In to Active Delay CAS Latency = 2	4	—	4	—	CK
$t_{DQW}$	DQM Write Mask Latency	0	—	0	—	CK

## Clock Frequency and Latency

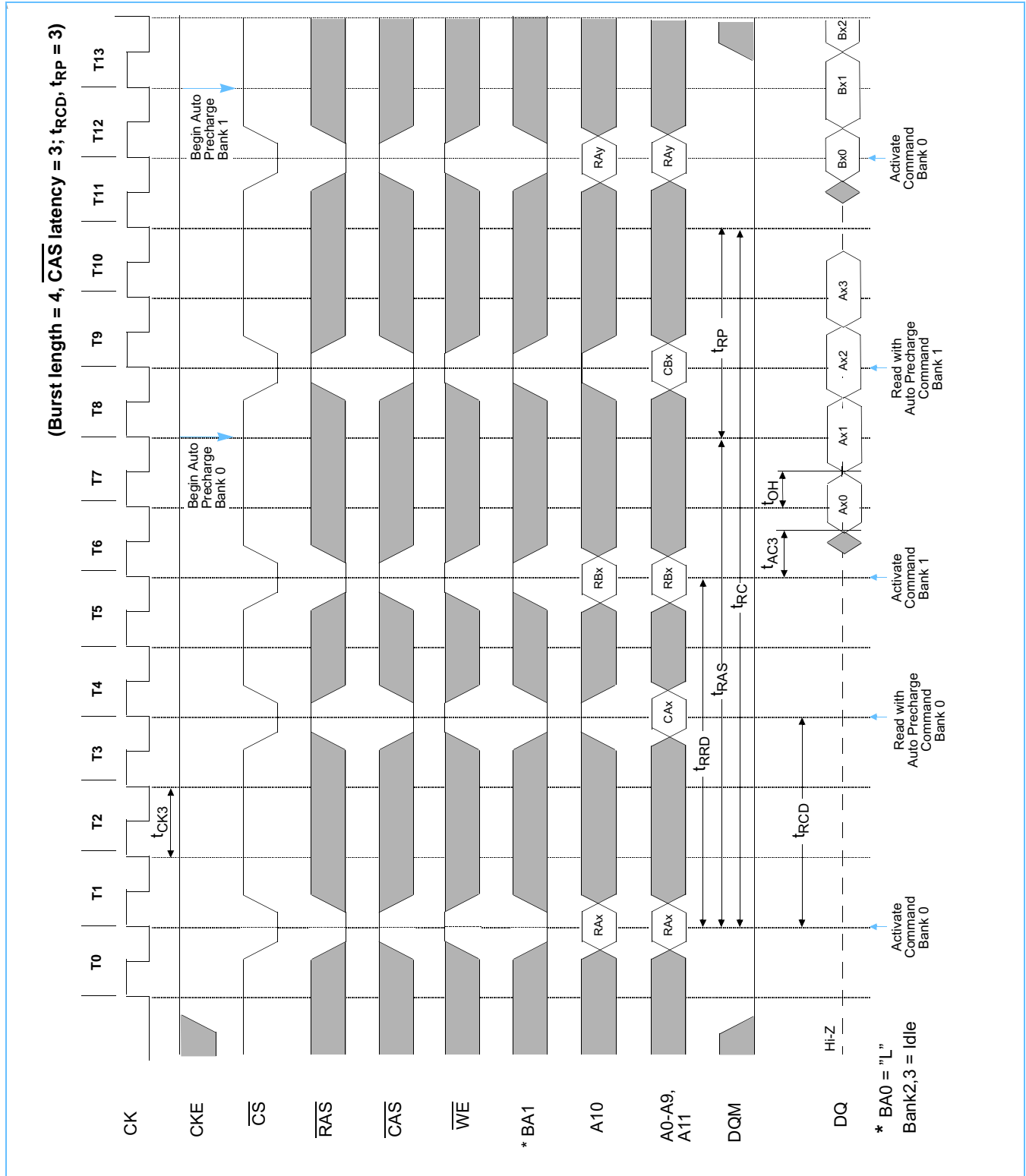
Symbol	Parameter	-7	-75	Units
$f_{CK}$	Clock Frequency	143	133	MHz
$t_{CK}$	Clock Cycle Time	7.0	7.5	ns
$t_{AA}$	$\overline{CAS}$ Latency	3	3	CK
$t_{RP}$	Precharge Time	3	3	CK
$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay	3	3	CK
$t_{RC}$	Bank Cycle Time	9	9	CK
$t_{RAS}$	Minimum Bank Active Time	6	6	CK
$t_{DPL}$	Data In to Precharge	2	2	CK
$t_{DAL}$	Data In to Active/Refresh	5	5	CK
$t_{RRD}$	Bank to Bank Delay Time	2	2	CK
$t_{CCD}$	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	1	CK
$t_{WL}$	Write Latency	0	0	CK
$t_{DQW}$	DQM Write Mask Latency	0	0	CK
$t_{DQZ}$	DQM Data Disable Latency	2	2	CK
$t_{CSL}$	Clock Suspend Latency	1	1	CK

AC Parameters for Write Timing

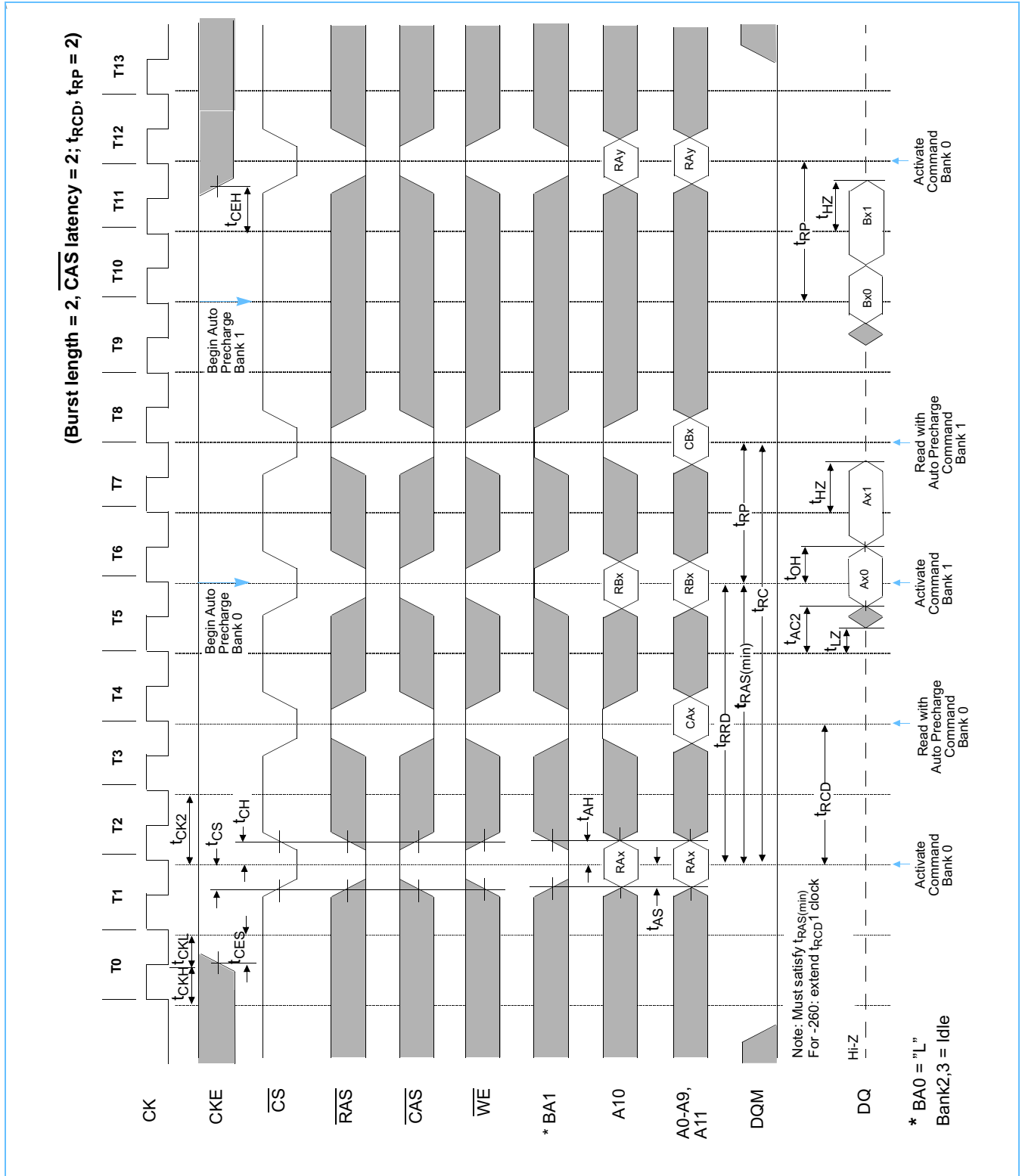




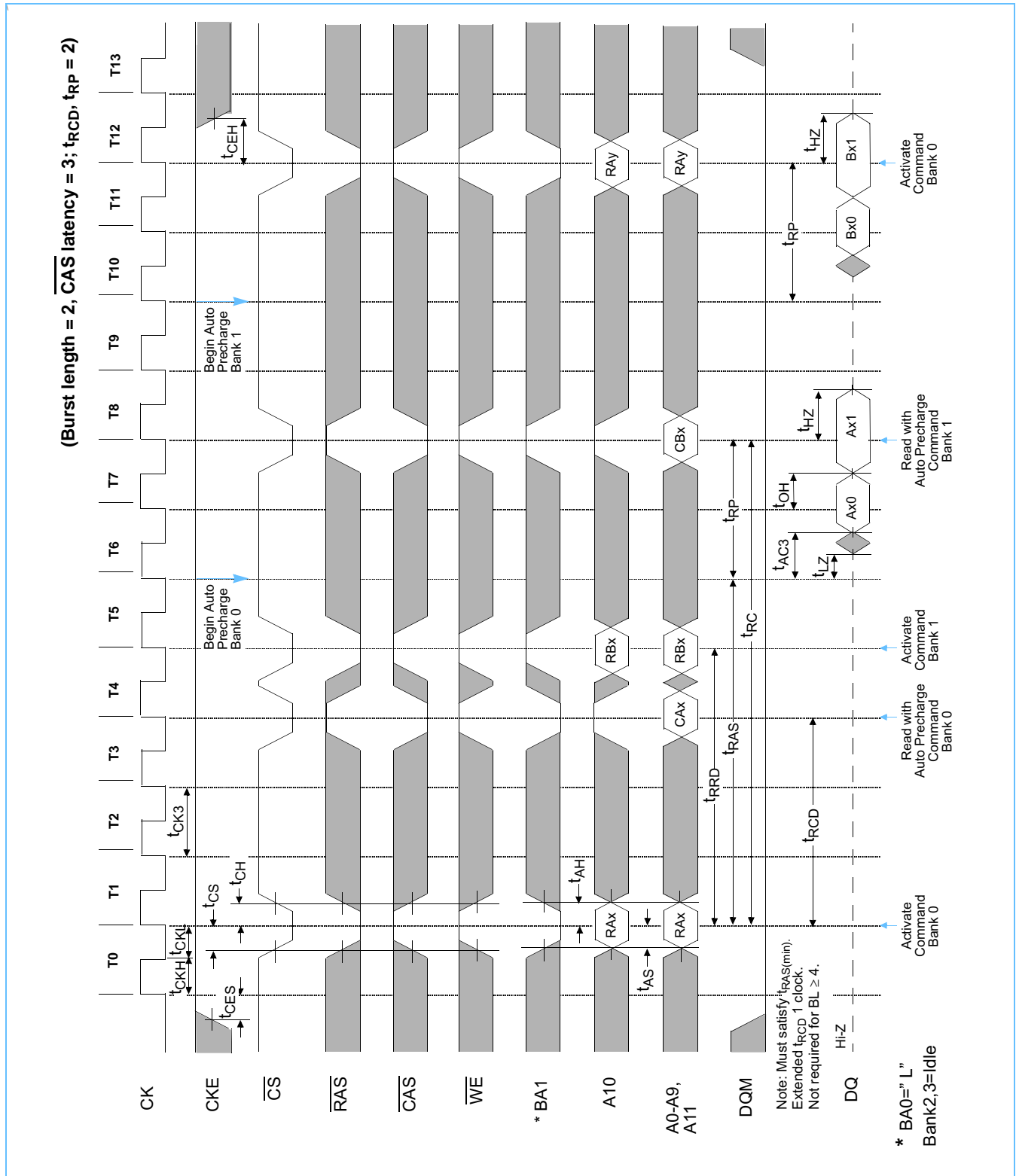
AC Parameters for Read Timing (3/3/3)



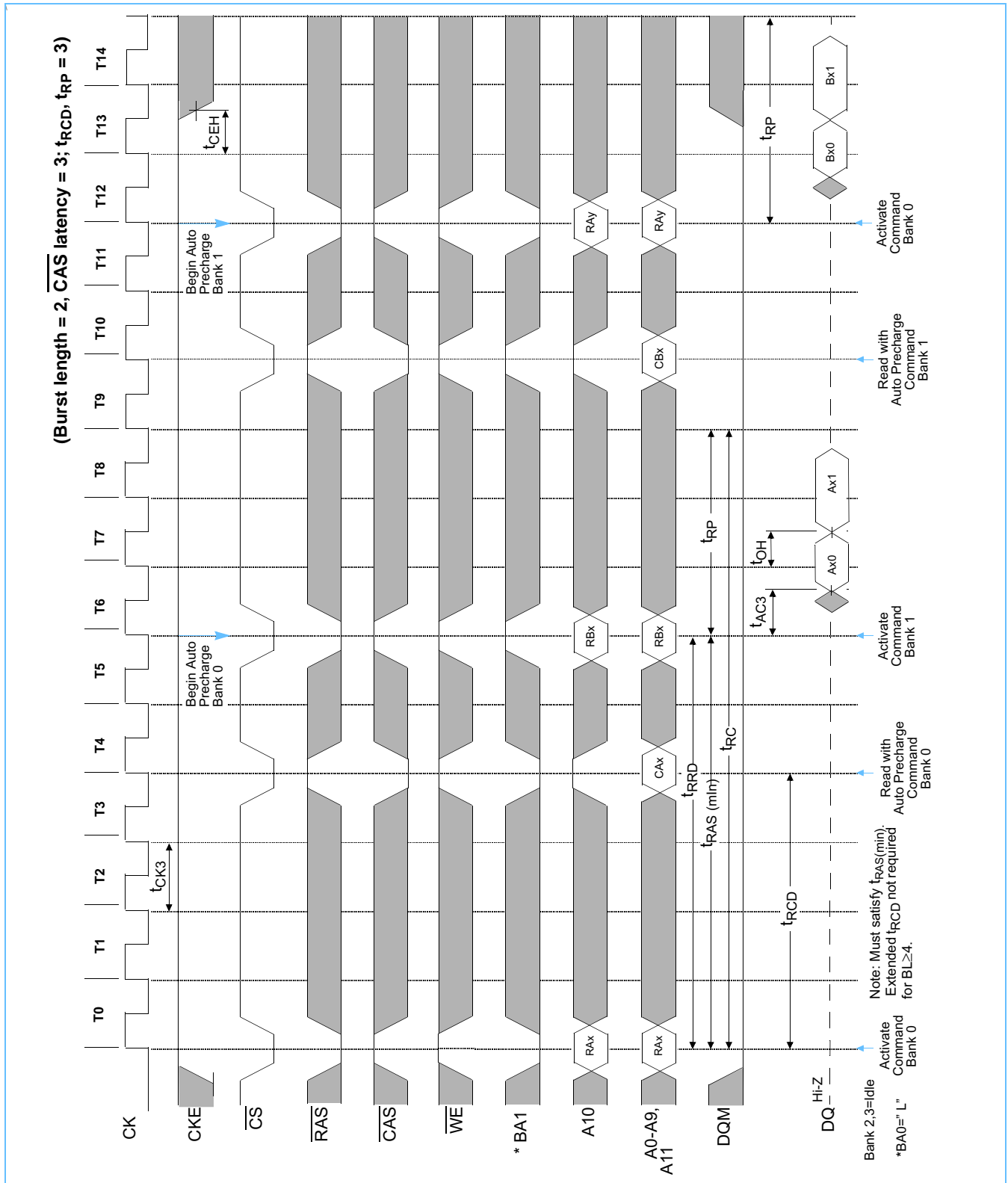
AC Parameters for Read Timing (2/2/2)



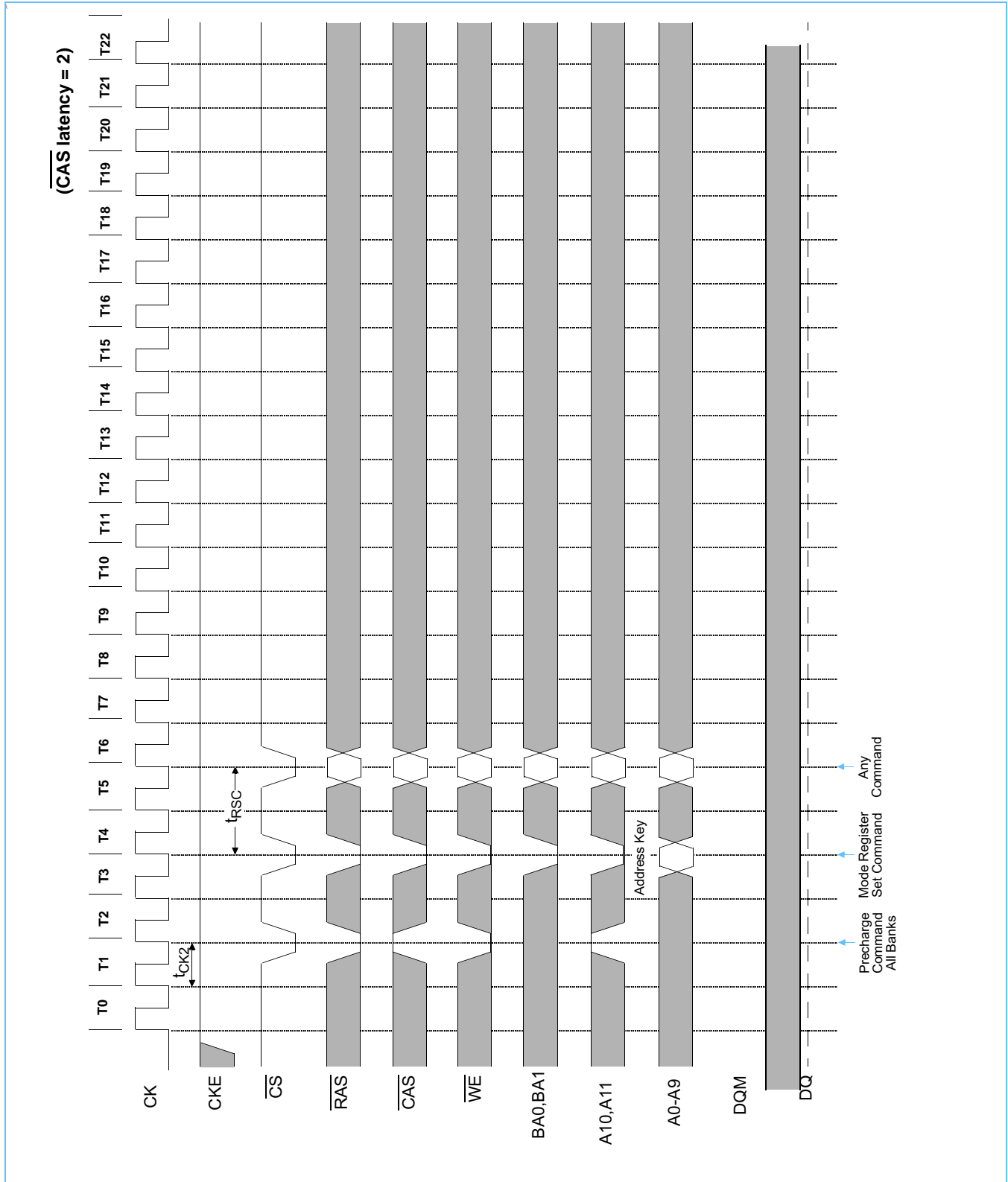
AC Parameters for Read Timing (3/2/2)



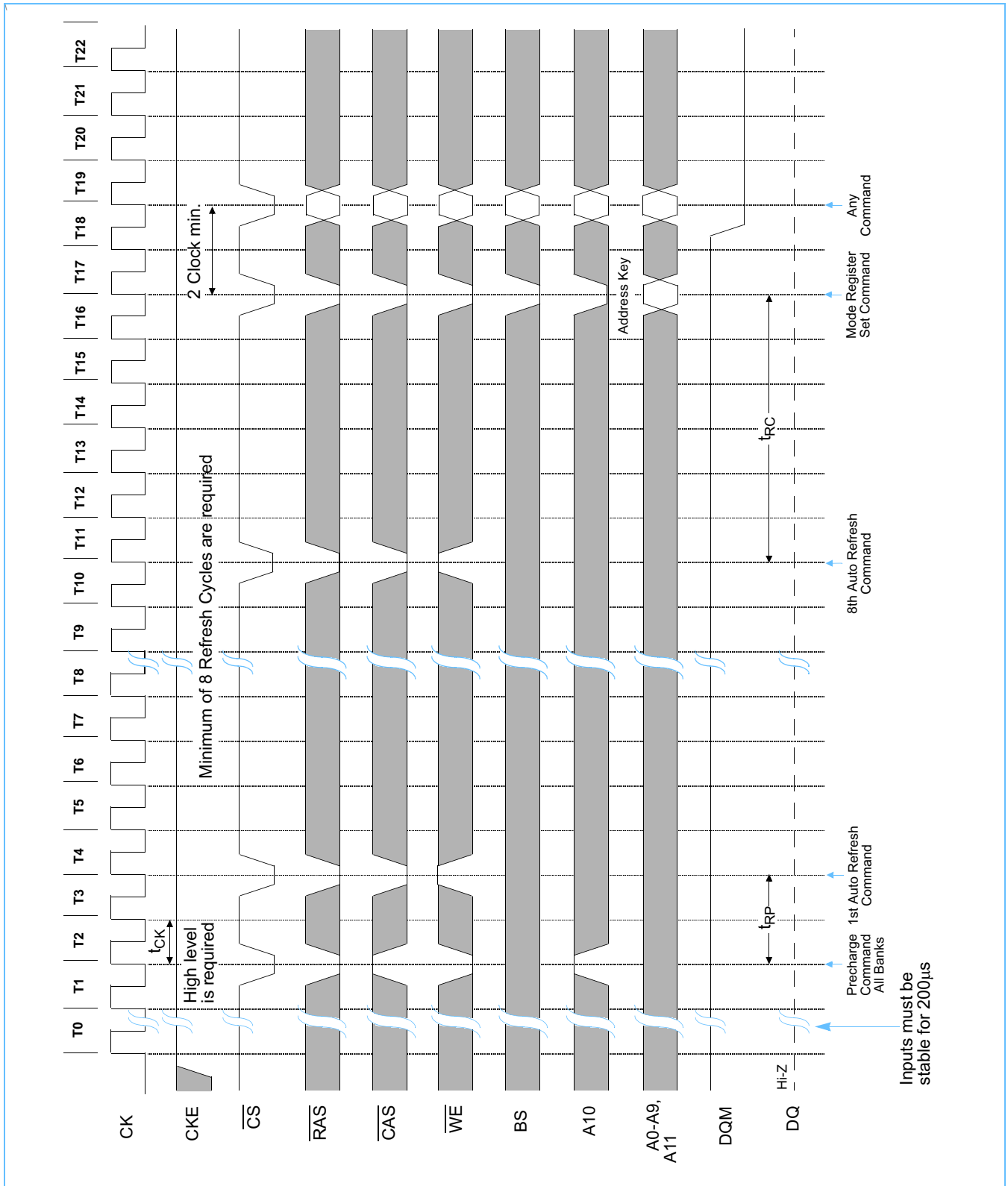
AC Parameters for Read Timing (3/3/3)



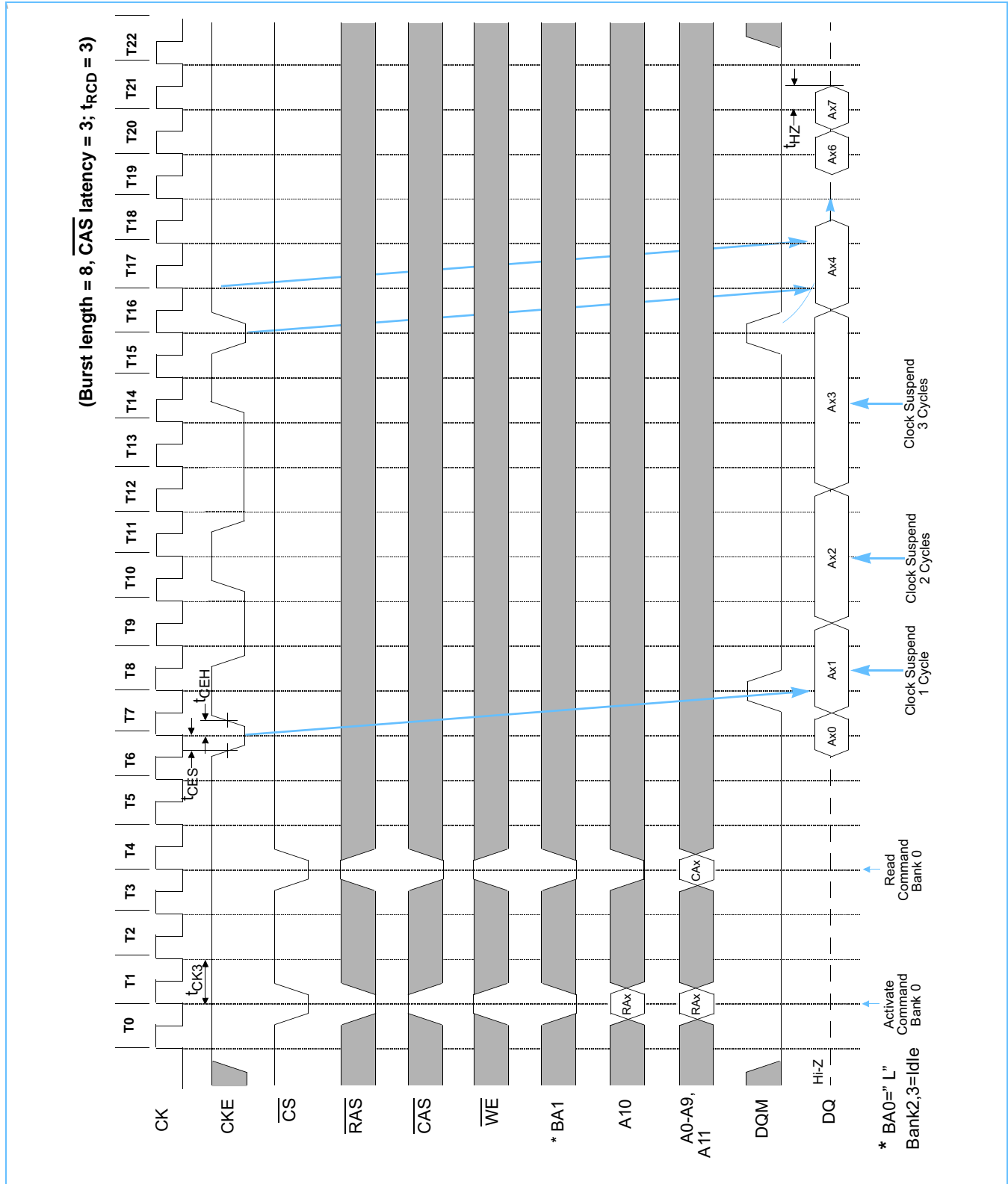
Mode Register Set



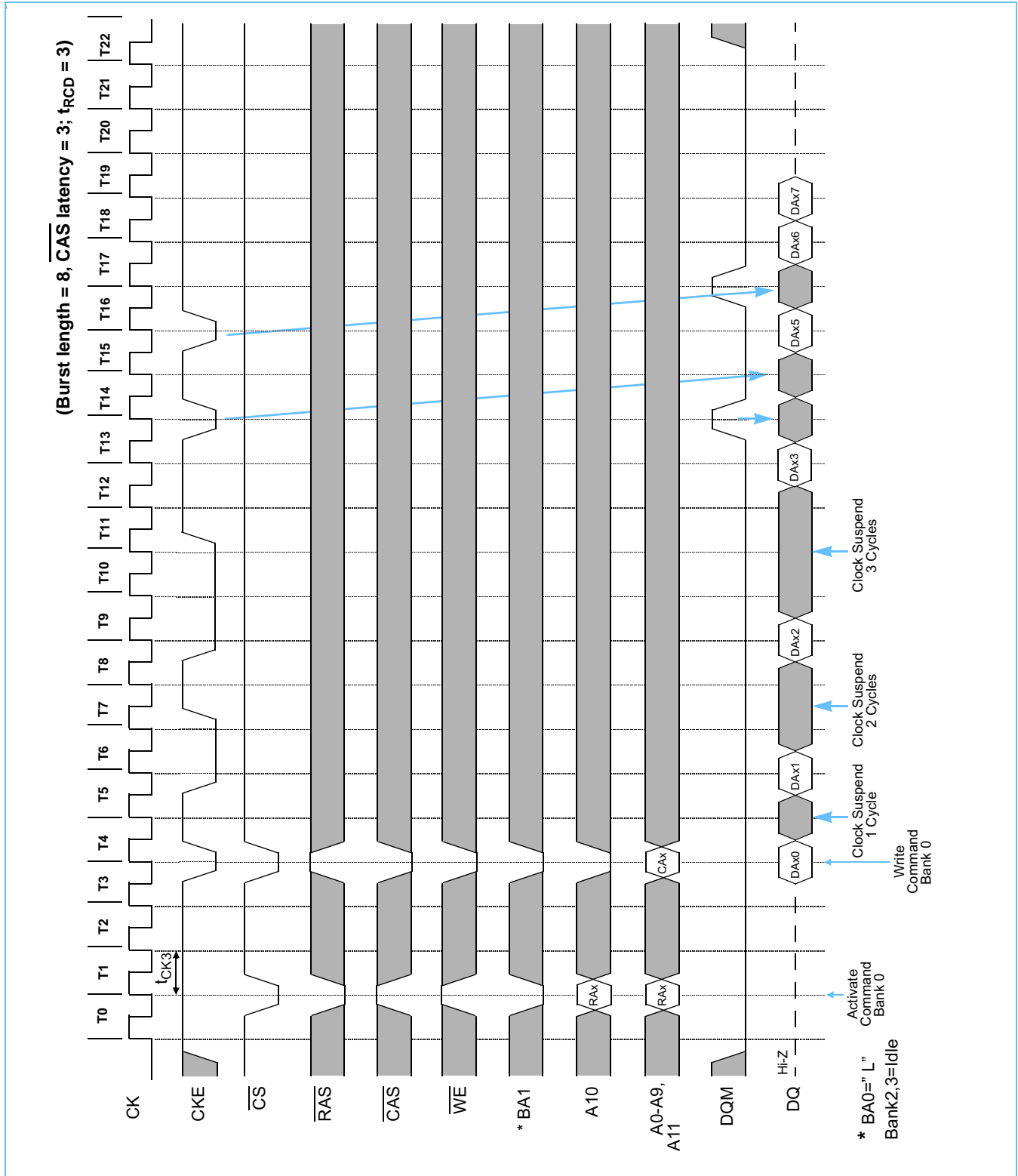
Power-On Sequence and Auto Refresh (CBR)



Clock Suspension / DQM During Burst Read

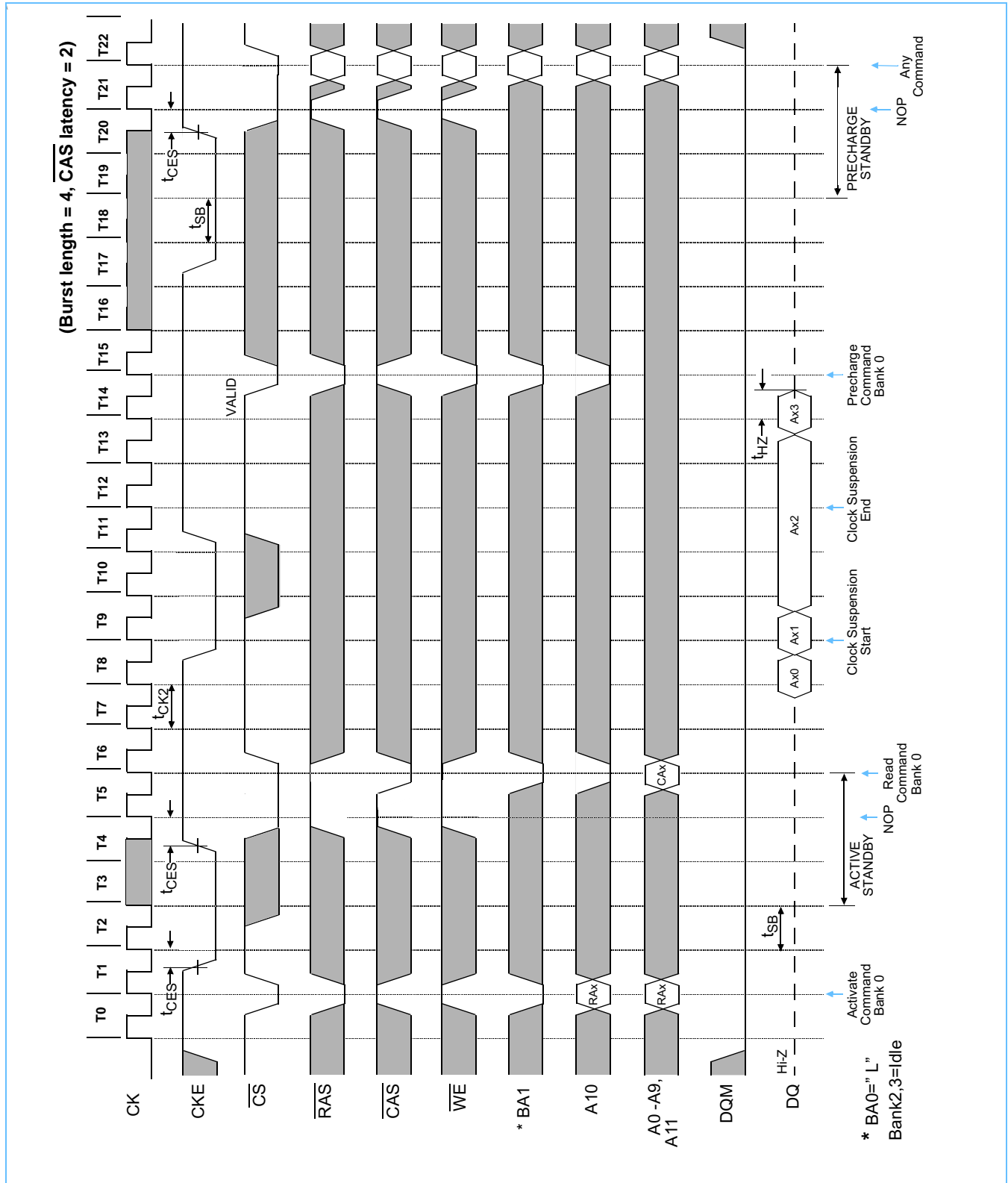


**Clock Suspension / DQM During Burst Write**

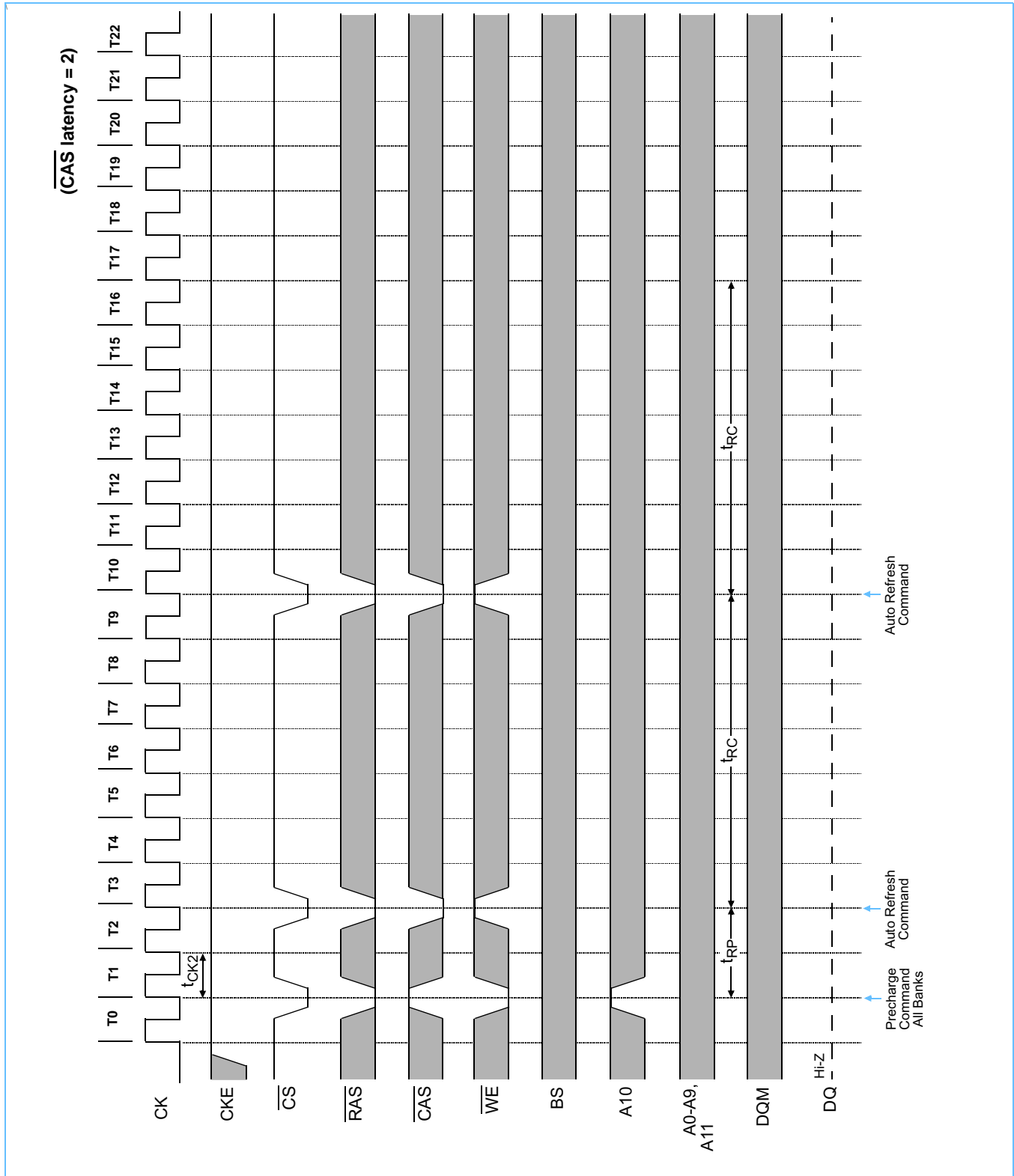




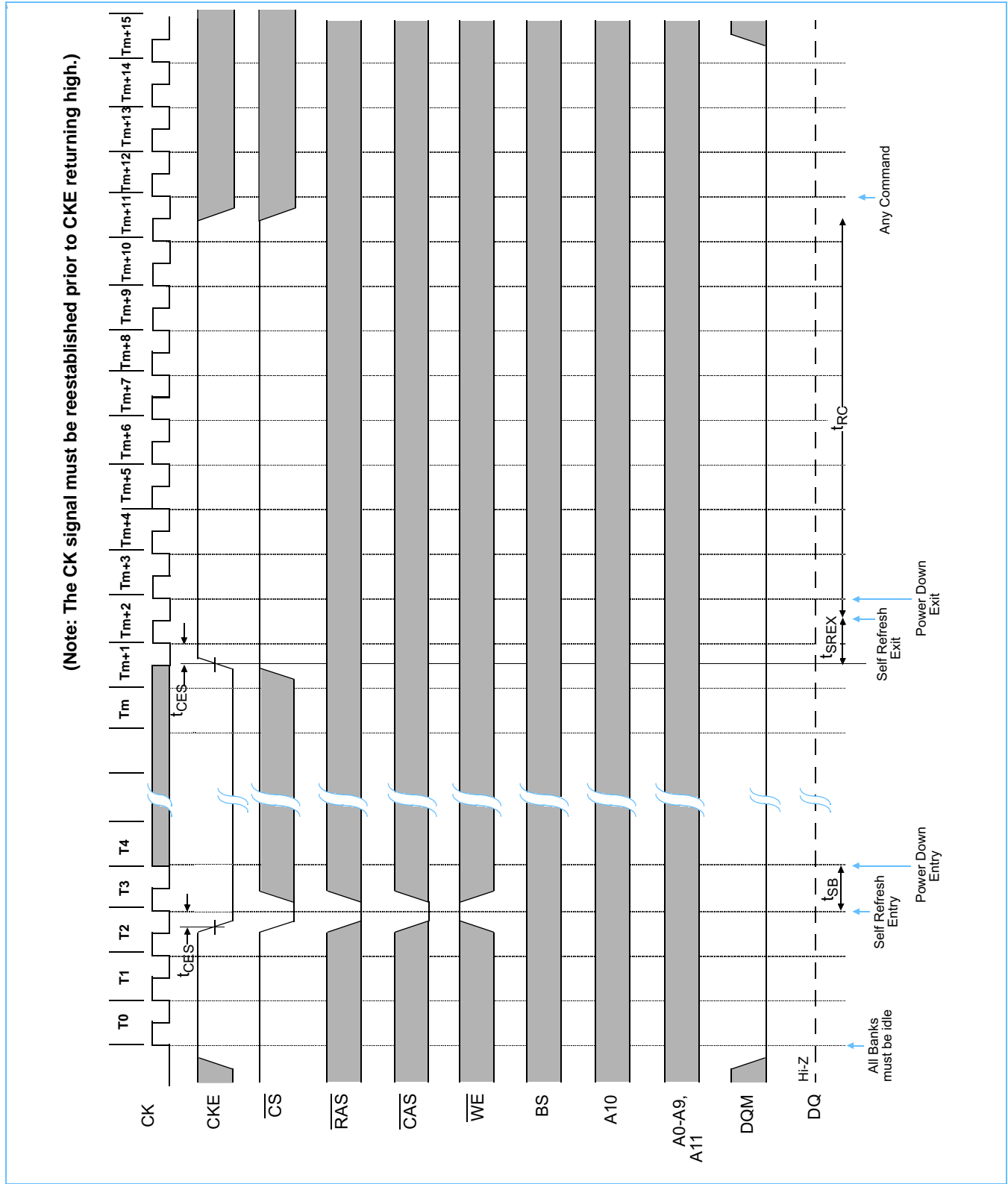
Power Down Mode and Clock Suspend



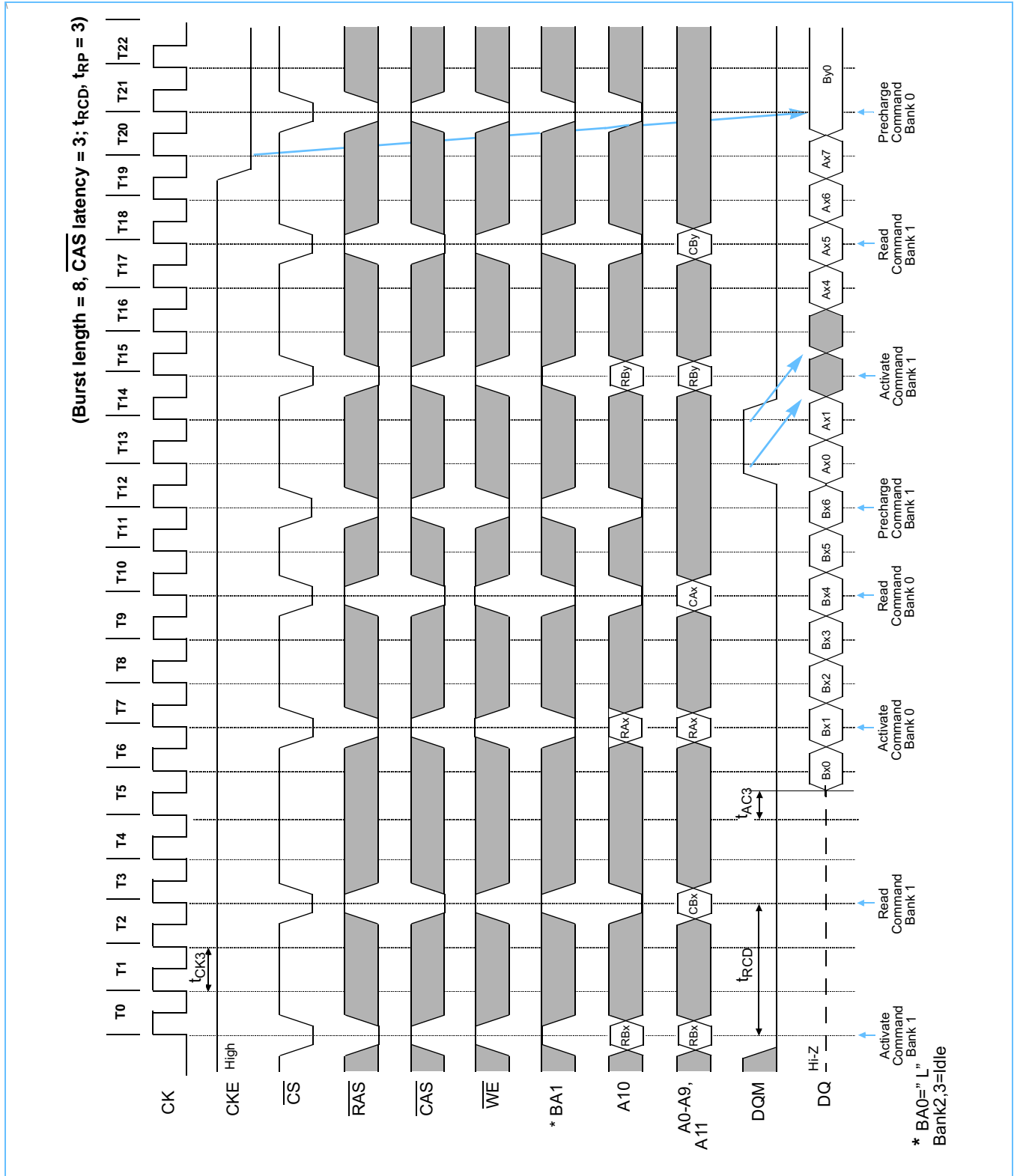
Auto Refresh (CBR)



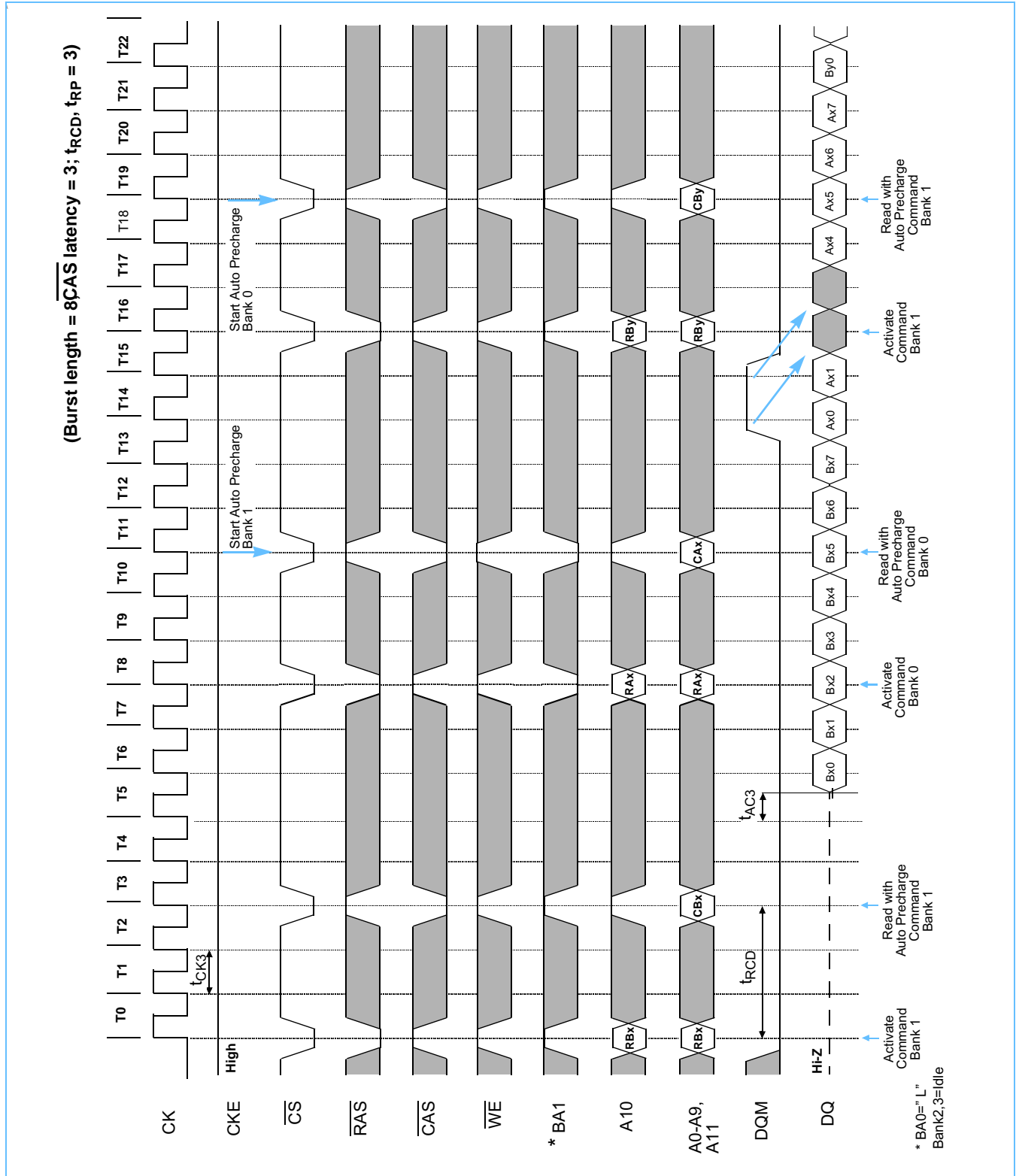
Self Refresh (Entry and Exit)



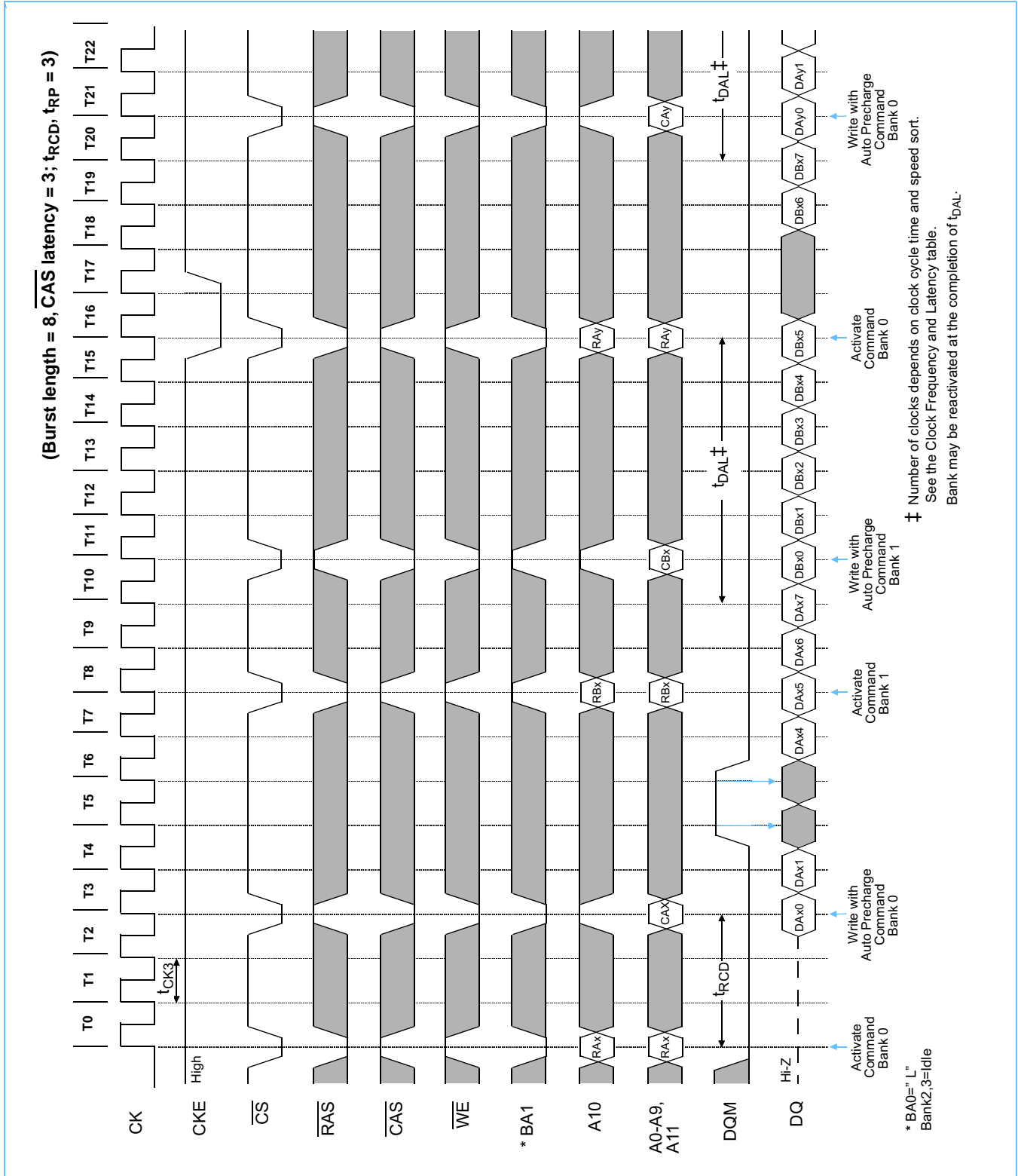
Random Row Read (Interleaving Banks) with Precharge



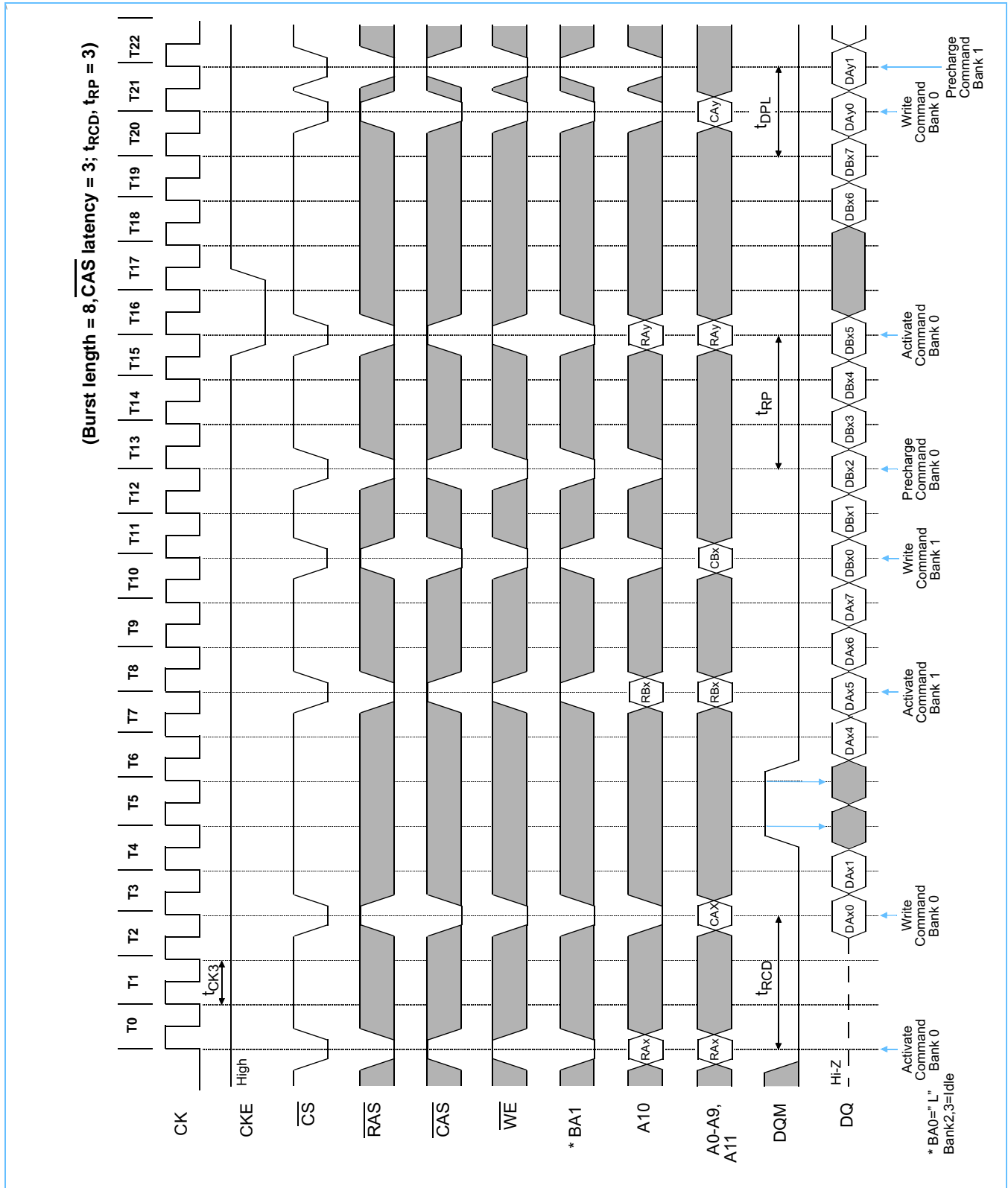
Random Row Read (Interleaving Banks) with Auto-Precharge



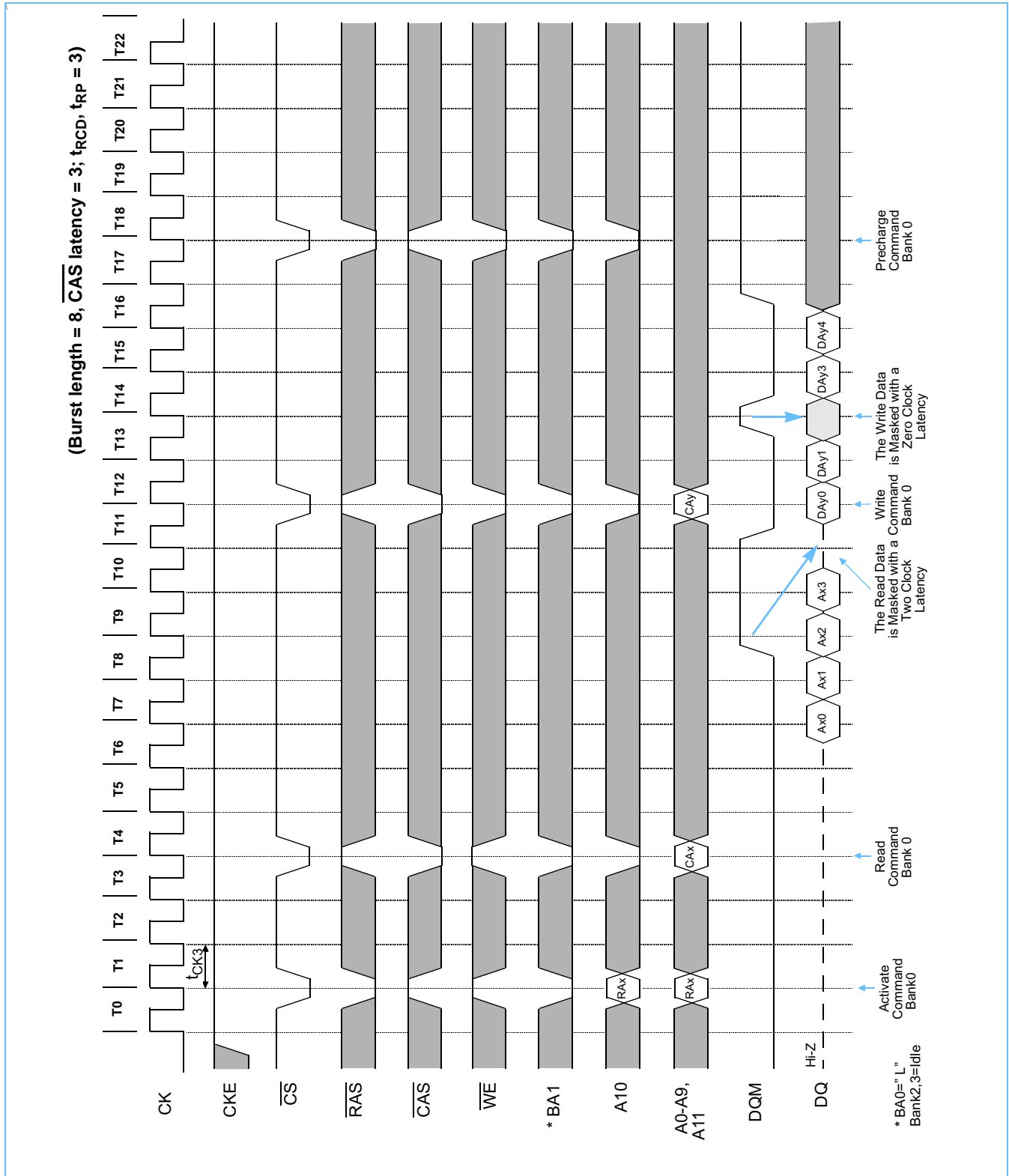
Random Row Write (Interleaving Banks) with Auto-Precharge



Random Row Write (Interleaving Banks) with Precharge

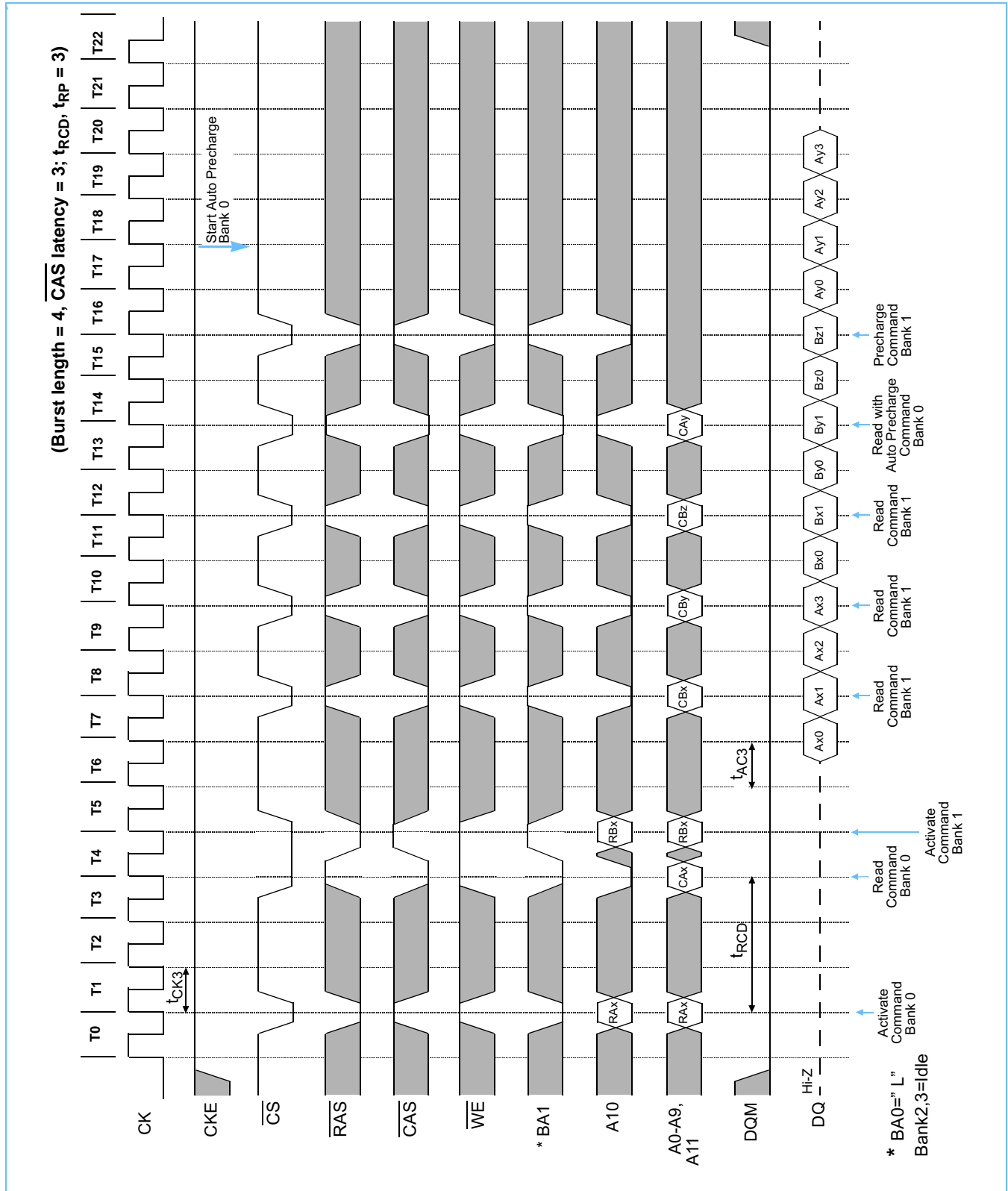


Read / Write Cycle

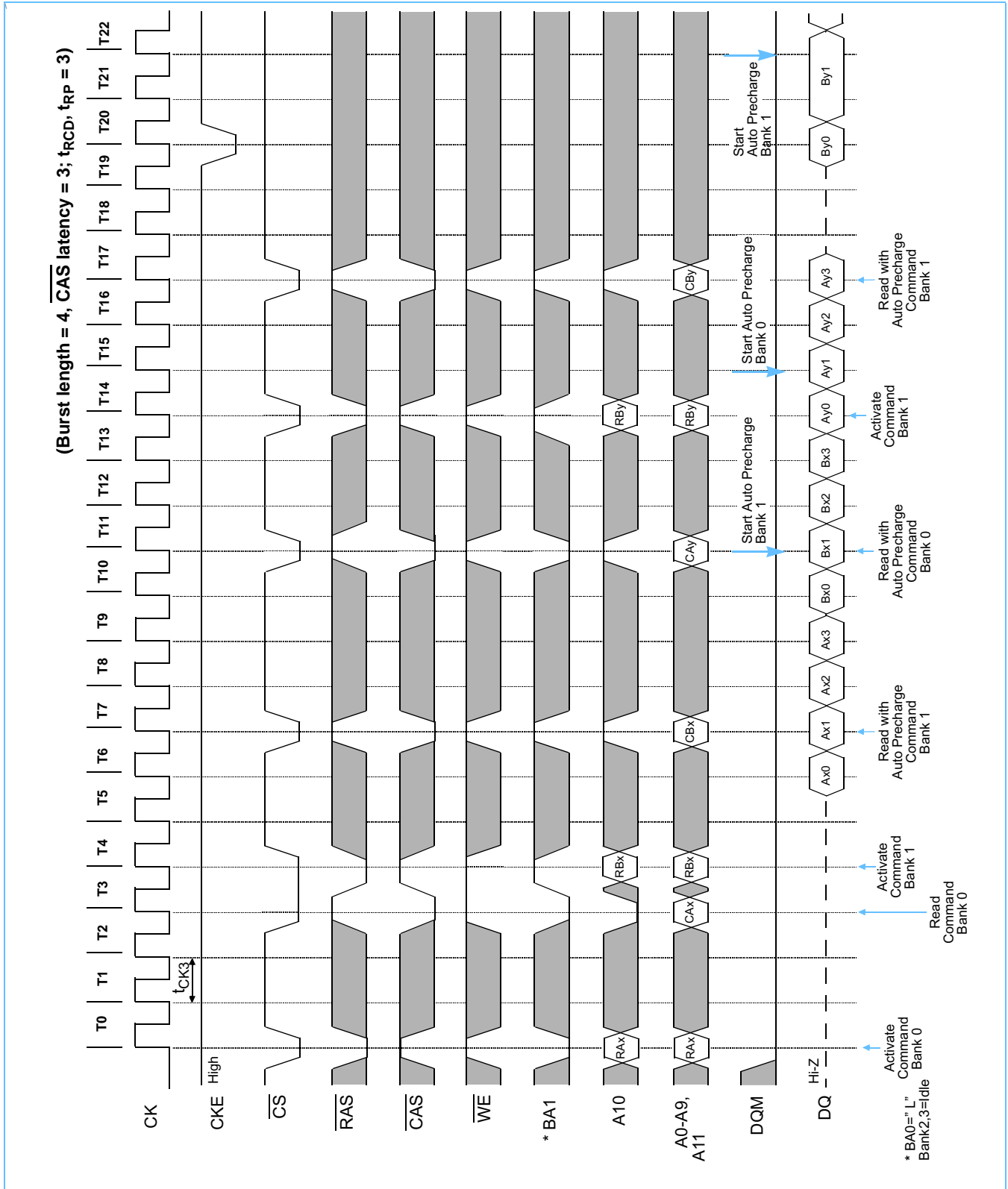




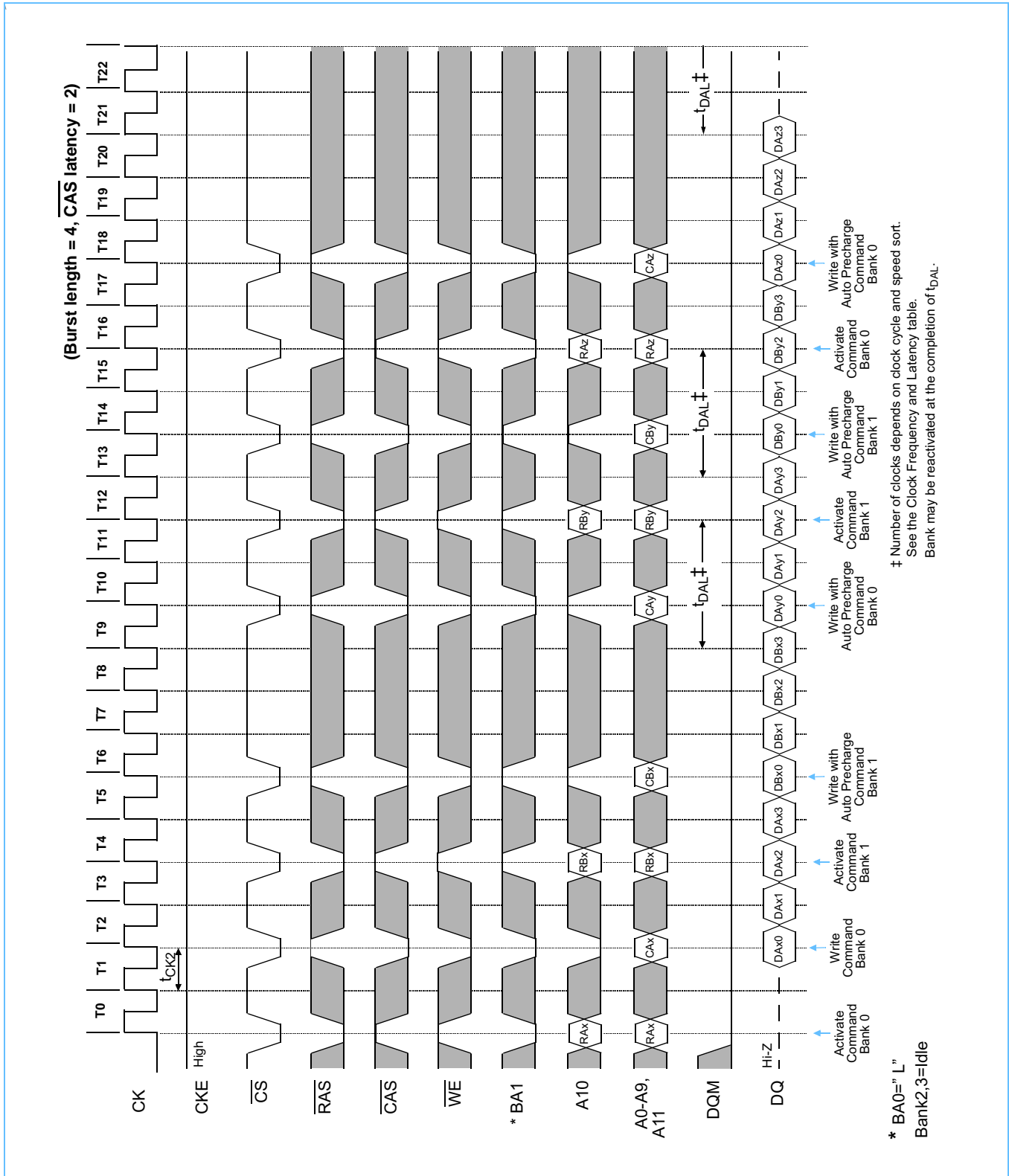
Interleaved Column Read Cycle



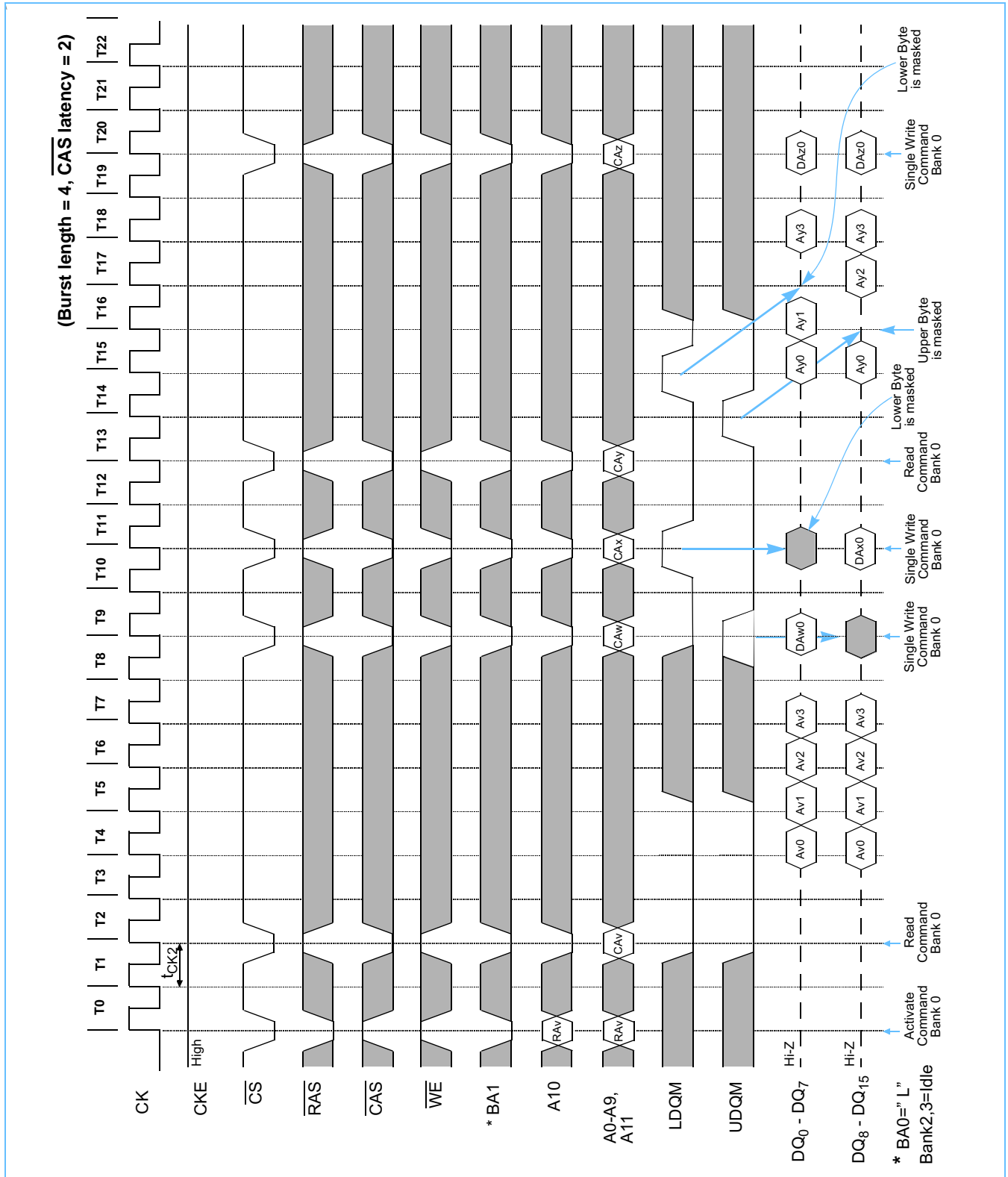
Auto Precharge after Read Burst



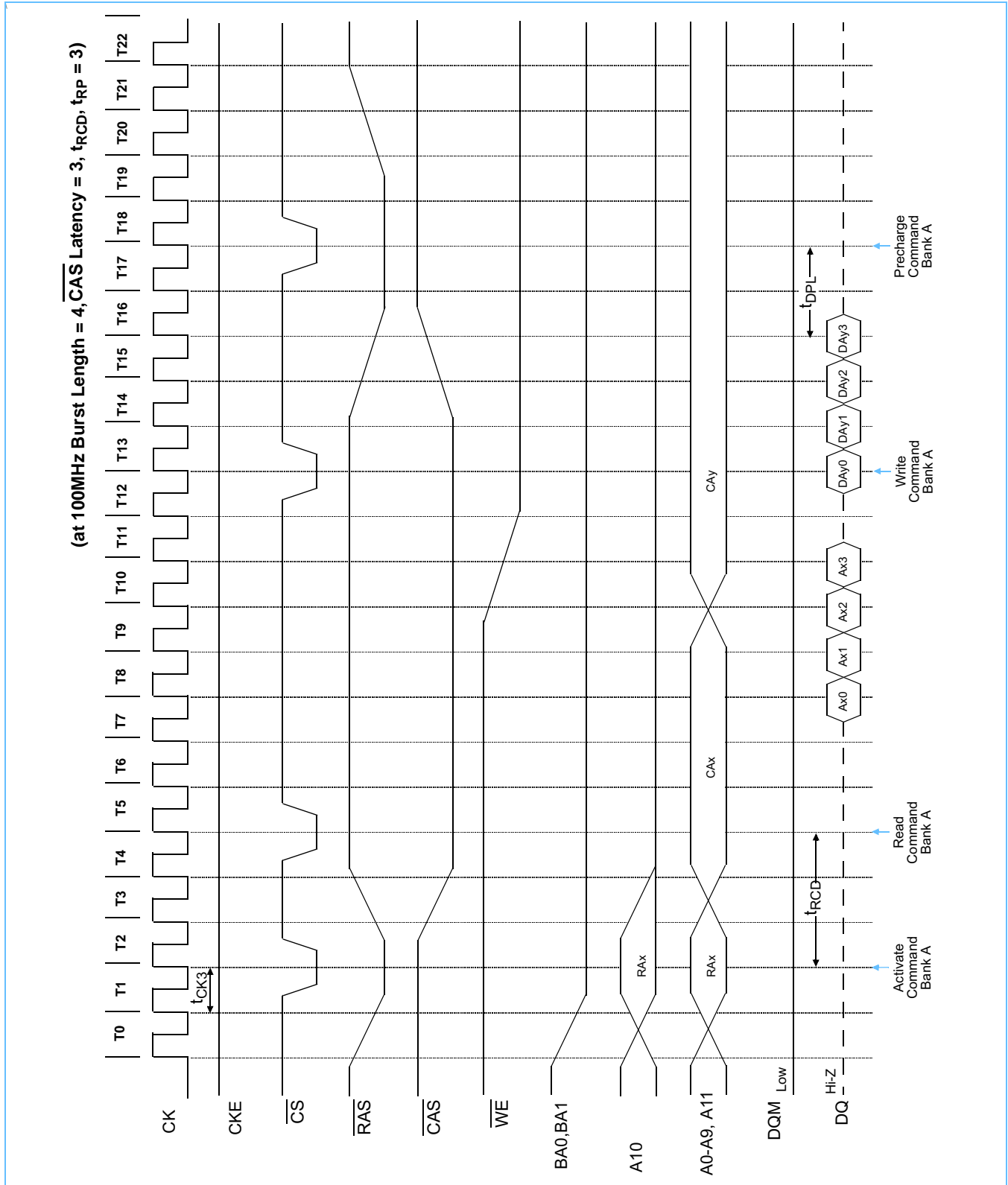
Auto Precharge after Write Burst



Burst Read and Single Write Operation



CS Function (Only CS signal needs to be asserted at minimum rate)



**ORDERING INFORMATION - V<sub>DD</sub> = 3.3V**

**Commercial Range: 0°C to 70°C**

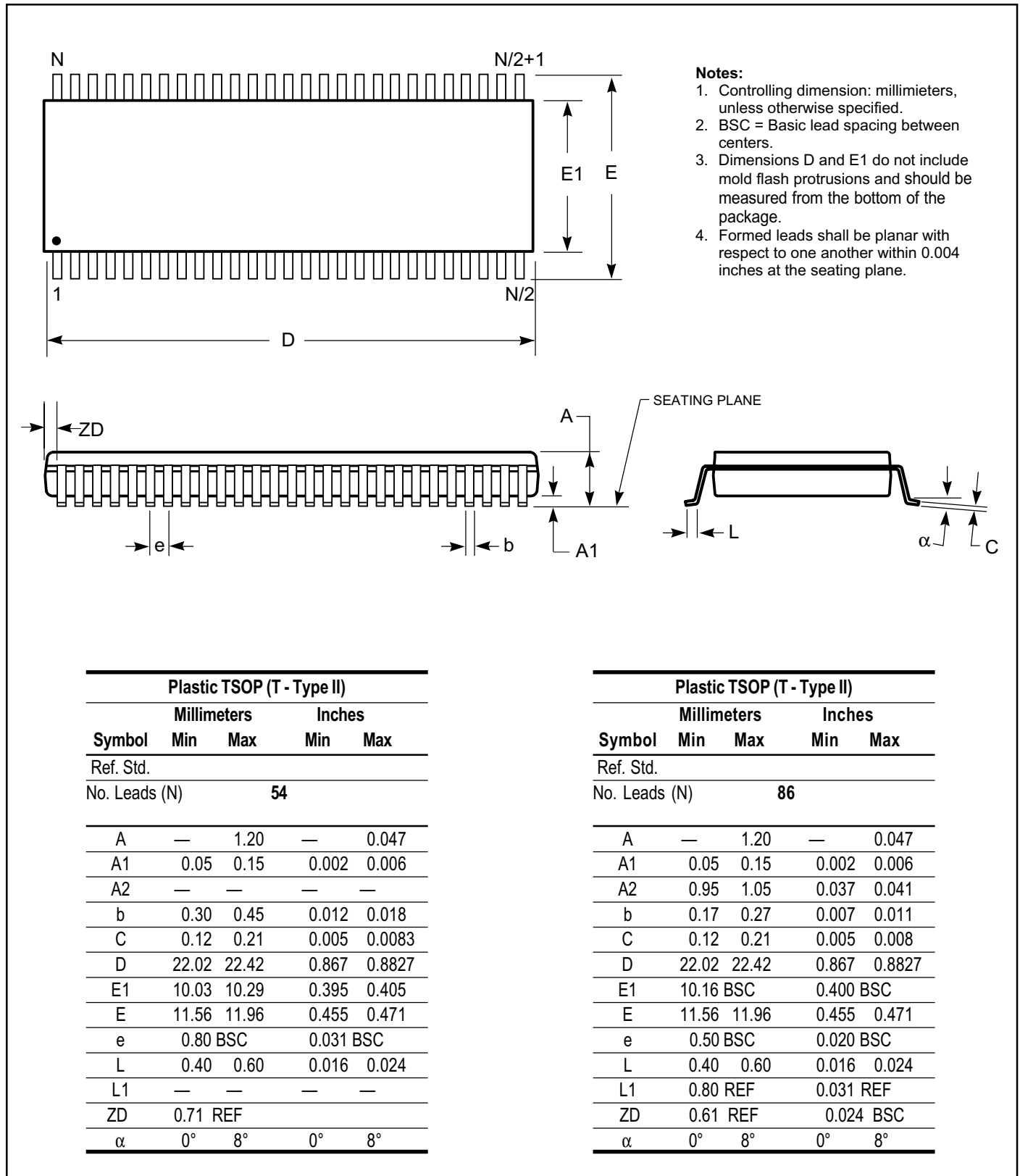
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<b>Frequency</b>	<b>Speed (ns)</b>	<b>Order Part No.</b>	<b>Package</b>
143 MHz	7	IS42S16800A1-7TL	54-Pin TSOPII, Lead-free

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## PACKAGING INFORMATION

Plastic TSOP 54-Pin, 86-Pin  
 Package Code: T (Type II)



Plastic TSOP (T - Type II)				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
Ref. Std.				
No. Leads (N)	54			
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	—	—	—	—
b	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.0083
D	22.02	22.42	0.867	0.8827
E1	10.03	10.29	0.395	0.405
E	11.56	11.96	0.455	0.471
e	0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024
L1	—	—	—	—
ZD	0.71 REF			
$\alpha$	0°	8°	0°	8°

Plastic TSOP (T - Type II)				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
Ref. Std.				
No. Leads (N)	86			
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.95	1.05	0.037	0.041
b	0.17	0.27	0.007	0.011
C	0.12	0.21	0.005	0.008
D	22.02	22.42	0.867	0.8827
E1	10.16 BSC		0.400 BSC	
E	11.56	11.96	0.455	0.471
e	0.50 BSC		0.020 BSC	
L	0.40	0.60	0.016	0.024
L1	0.80 REF		0.031 REF	
ZD	0.61 REF		0.024 BSC	
$\alpha$	0°	8°	0°	8°