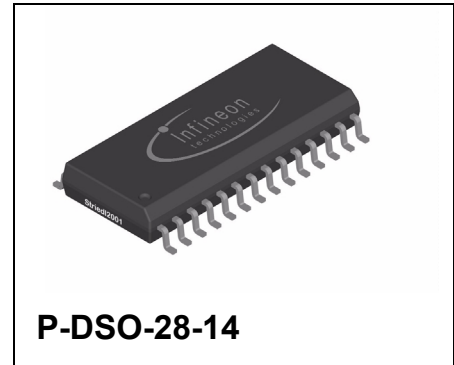


**Data Sheet**

**1 Overview**

**1.1 Features**

- Quad D-MOS switch driver
- Free configurable as bridge or quad-switch
- Optimized for DC motor management applications
- Low  $R_{DS\ ON}$ : 70 m $\Omega$  high-side switch, 45 m $\Omega$  low-side switch (typical values @ 25 °C)
- Maximum peak current: typ. 14 A @ 25 °C
- Very low quiescent current: typ. 5  $\mu$ A @ 25 °C
- Small outline, enhanced power P-DSO-package
- Full short-circuit-protection
- Operates up to 40 V
- Status flag diagnosis
- Overtemperature shut down with hysteresis
- Internal clamp diodes
- Open load detection in Off-mode
- Under-voltage detection with hysteresis
- PWM frequencies up to 1 kHz



Type	Ordering Code	Package
BTS 7751 G	Q67007-A9553	P-DSO-28-14

**1.2 Description**

The **BTS 7751 G** is part of the **TrilithIC** family containing three dies in one package: One double high-side switch and two low-side switches. The drains of these three vertical DMOS chips are mounted on separated lead frames. The sources are connected to individual pins, so the **BTS 7751 G** can be used in H-bridge- as well as in any other configuration. Both the double high-side and the two low-side switches of the **BTS 7751 G** are manufactured in **SMART SIPMOS<sup>®</sup>** technology which combines low  $R_{DS\ ON}$  vertical DMOS power stages with CMOS control circuitry. The high-side switch is fully protected and contains the control and diagnosis circuitry. Also the low-side switches are fully protected, the equivalent standard product is the **BSP 78**.

In contrast to the **BTS 7750 G**, the **BTS 7751 G** offers an open load in Off-mode detection and slightly increased current limitation.

### 1.3 Pin Configuration (top view)

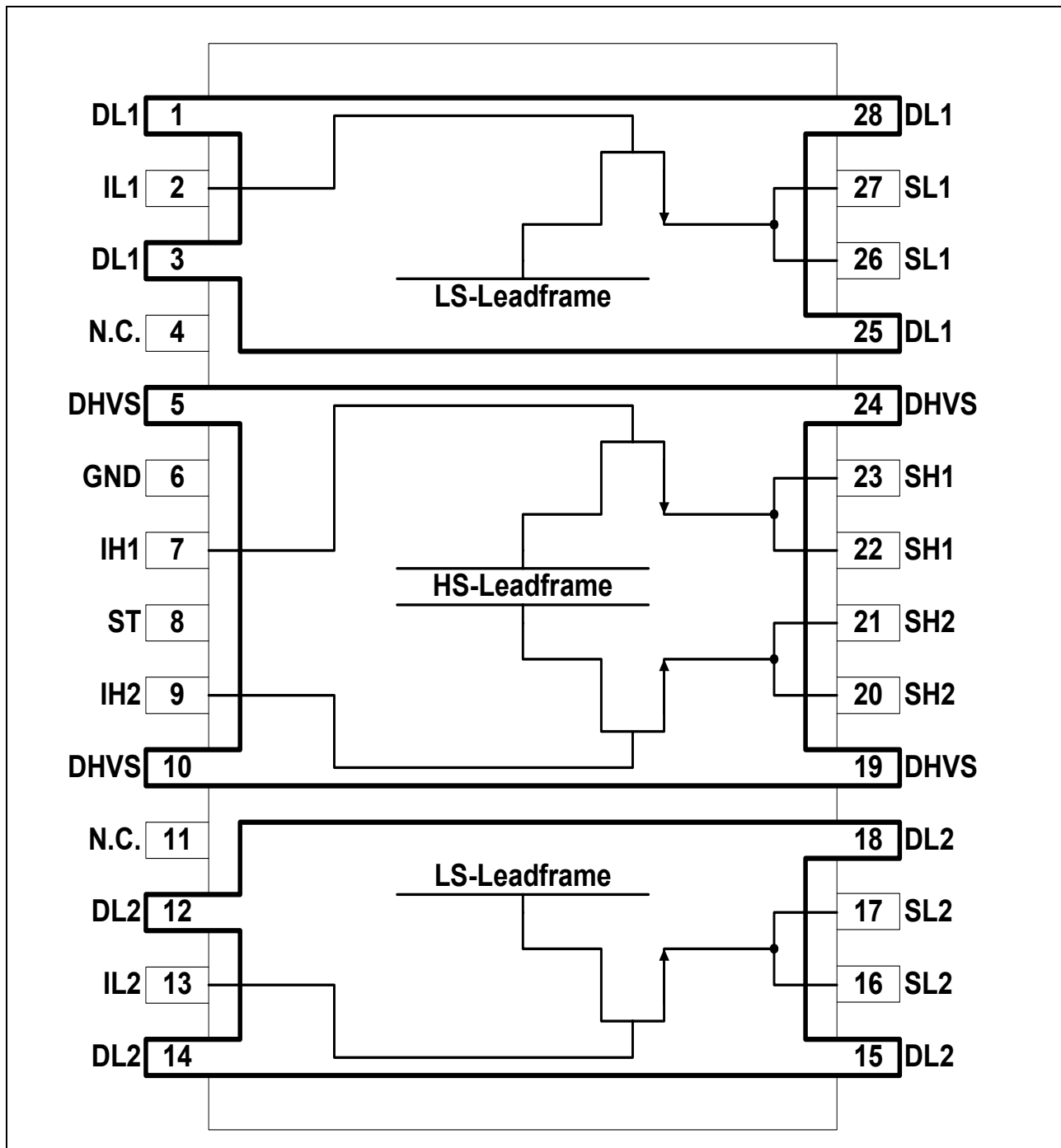


Figure 1

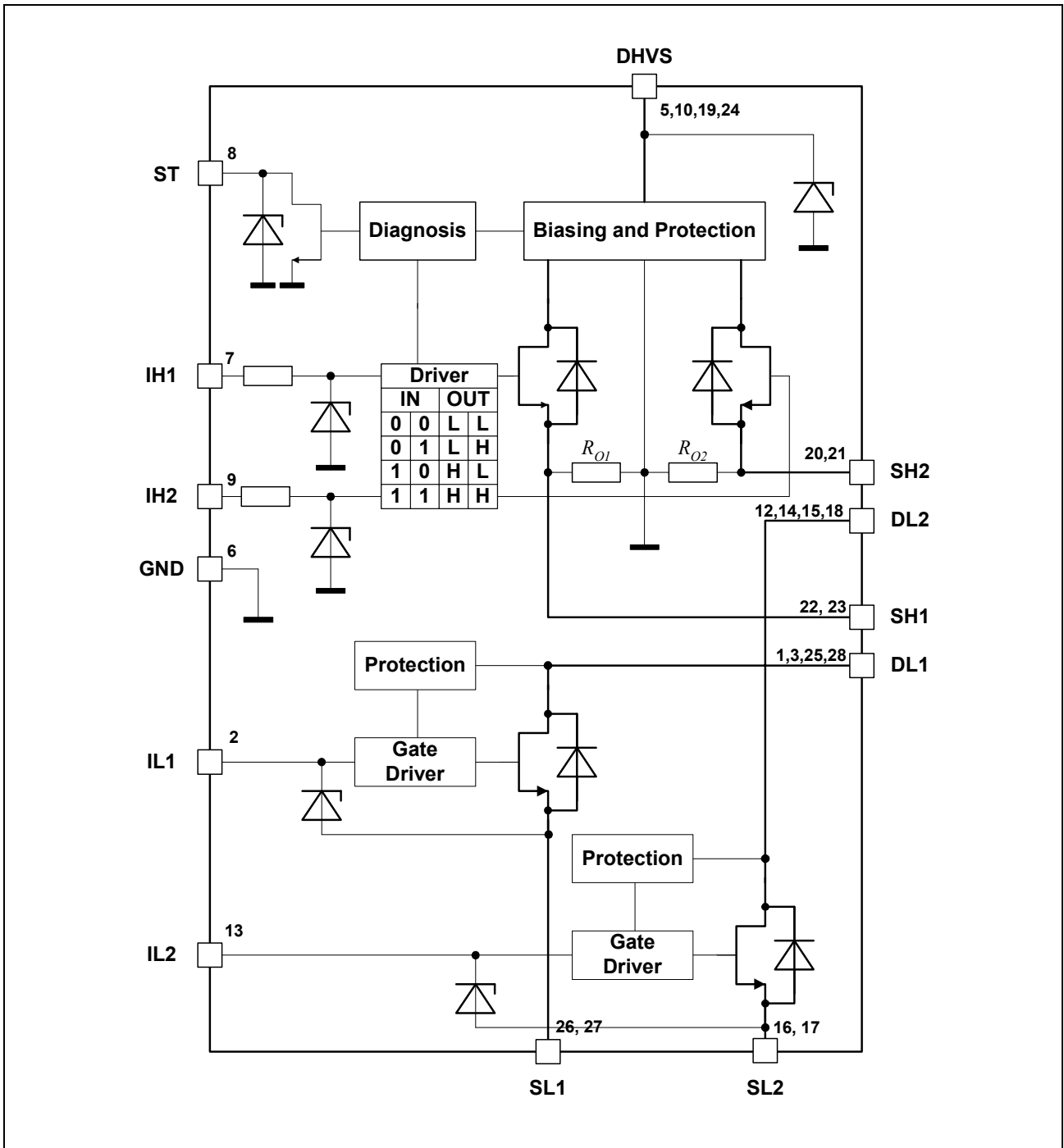
**1.4 Pin Definitions and Functions**

Pin No.	Symbol	Function
<b>1, 3, 25, 28</b>	<b>DL1</b>	<b>Drain of low-side switch1, lead frame 1 <sup>1)</sup></b>
2	IL1	Analog input of low-side switch1
4	N.C.	not connected
<b>5, 10, 19, 24</b>	<b>DHVS</b>	<b>Drain of high-side switches and power supply voltage, lead frame 2 <sup>1)</sup></b>
6	GND	Ground
7	IH1	Digital input of high-side switch1
8	ST	Status of high-side switches; open Drain output
9	IH2	Digital input of high-side switch2
11	N.C.	not connected
<b>12, 14, 15, 18</b>	<b>DL2</b>	<b>Drain of low-side switch2, lead frame 3 <sup>1)</sup></b>
13	IL2	Analog input of low-side switch2
<b>16,17</b>	<b>SL2</b>	<b>Source of low-side switch2</b>
<b>20,21</b>	<b>SH2</b>	<b>Source of high-side switch2</b>
<b>22,23</b>	<b>SH1</b>	<b>Source of high-side switch1</b>
<b>26,27</b>	<b>SL1</b>	<b>Source of low-side switch1</b>

<sup>1)</sup> To reduce the thermal resistance these pins are direct connected via metal bridges to the lead frame.

Pins written in **bold type** need power wiring.

### 1.5 Functional Block Diagram



**Figure 2**  
**Block Diagram**

## 1.6 Circuit Description

### Input Circuit

The control inputs IH1,2 consist of TTL/CMOS compatible Schmitt-Triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages. The inputs are protected by ESD clamp-diodes.

The inputs IL1 and IL2 are connected to the internal gate-driving units of the N-channel vertical power-MOS-FETs.

### Output Stages

The output stages consist of an low  $R_{DS\ ON}$  Power-MOS H-bridge. In H-bridge configuration, the D-MOS body diodes can be used for freewheeling when commutating inductive loads. If the high-side switches are used as single switches, positive and negative voltage spikes which occur when driving inductive loads are limited by integrated power clamp diodes.

### Short Circuit Protection

The outputs are protected against

- output short circuit to ground
- output short circuit to the supply voltage, and
- overload (load short circuit).

An internal OP-Amp controls the Drain-Source-Voltage by comparing the DS-Voltage-Drop with an internal reference voltage. Above this trippoint the OP-Amp reduces the output current depending on the junction temperature and the drop voltage.

In the case of overloaded high-side switches the status output is set to low.

The fully protected low-side switches have no status output.

### Overtemperature Protection

The high-side and the low-side switches also incorporate an overtemperature protection circuit with hysteresis which switches off the output transistors. In the case of the high-side switches, the status output is set to low.

### Under voltage-Lockout (UVLO)

When  $V_S$  reaches the switch-on voltage  $V_{UVON}$  the IC becomes active with a hysteresis. The High-Side output transistors are switched off if the supply voltage  $V_S$  drops below the switch off value  $V_{UVOFF}$ .

## Open Load Detection

Open load is detected by voltage measurement in Off state. If the output voltage exceeds a specified level the error flag is set with a delay.

## Status Flag

The status flag output is an open drain output with Zener-diode which requires a pull-up resistor, c.f. the application circuit on page 14. Various errors as listed in the table "Diagnosis" are detected by switching the open drain output ST to low. Forward current in the integrated body diode of the high-side switch may cause undefined voltage levels at the corresponding status output. The open load detection can be used to detect a short to  $V_s$  as long as both low-side switches are off and  $R_{OL}$  is disconnected from 5V by BCR192W.

## 2 Truth table and Diagnosis (valid only for the High-Side-Switches)

Flag	IH1	IH2	SH1	SH2	ST	Remarks
	Inputs		Outputs			
Normal operation; identical with functional truth table	0	0	L	L	1	stand-by mode switch2 active switch1 active both switches active
	0	1	L	H	1	
	1	0	H	L	1	
	1	1	H	H	1	
Open load at high-side switch 1	0	X	Z	X	0	detected
	1	X	H	X	1	
Open load at high-side switch 2	X	0	X	Z	0	detected
	X	1	X	H	1	
Overtemperature high-side switch1	0	X	L	X	1	detected
	1	X	L	X	0	
Overtemperature high-side switch2	X	0	X	L	1	detected
	X	1	X	L	0	
Overtemperature both high-side switches	0	0	L	L	1	detected detected
	X	1	L	L	0	
	1	X	L	L	0	
Under voltage	X	X	L	L	1	not detected

### Inputs:

0 = Logic LOW

1 = Logic HIGH

X = don't care

### Outputs:

Z = Output in tristate condition

L = Output in sink condition

H = Output in source condition

X = Voltage level undefined

### Status:

1 = No error

0 = Error

### 3 Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

$$-40\text{ °C} < T_j < 150\text{ °C}$$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

#### High-Side-Switches (Pins DHVS, IH1,2 and SH1,2)

Supply voltage	$V_S$	- 0.3	42	V	-
Supply voltage for full short circuit protection	$V_{S(SCP)}$		28	V	
HS-drain current*	$I_S$	- 7.5	**	A	$T_A = 25\text{ °C}; t_P < 100\text{ ms}$
HS-input current	$I_{IH}$	- 5	5	mA	Pin IH1 and IH2
HS-input voltage	$V_{IH}$	- 10	16	V	Pin IH1 and IH2

Note: \* single pulse      \*\* internally limited

#### Status Output ST

Status pull up voltage	$V_{ST}$	- 0.3	5.4	V	
Status Output current	$I_{ST}$	- 5	5	mA	Pin ST

#### Low-Side-Switches (Pins DL1,2, IL1,2 and SL1,2)

Drain-Source-Clamp voltage	$V_{DSL}$	42	-	V	$V_{IL} = 0\text{ V}; I_D \leq 1\text{ mA}$
Supply voltage for short circuit protection	$V_{DSL(SCP)}$		30	V	$V_{IL} = 5\text{ V}$
			20	V	$V_{IL} = 10\text{ V}$
LS-drain current*	$I_{DL}$	- 7.5	**	A	$T_A = 25\text{ °C}; t_P < 100\text{ ms}$
LS-input voltage	$V_{IL}$	- 0.3	10	V	-

Note: \* single pulse      \*\* internally limited

#### Temperatures

Junction temperature	$T_j$	- 40	150	°C	-
Storage temperature	$T_{stg}$	- 55	150	°C	-

### 3.1 Absolute Maximum Ratings (cont'd)

$$-40\text{ °C} < T_j < 150\text{ °C}$$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

#### Thermal Resistances (one HS-LS-Path active)

LS-junction case	$R_{thjCL}$	–	20	K/W	measured to pin 3 or 12
HS-junction case	$R_{thjCH}$	–	20	K/W	measured to pin 19
Junction ambient $R_{thja} = T_{j(HS)}/(P_{(HS)}+P_{(LS)})$	$R_{thja}$	–	60	K/W	device soldered to reference PCB with 6 cm <sup>2</sup> cooling area

**ESD Protection** (Human Body Model acc. MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993)

Input LS-Switch	$V_{ESD}$	–	2	kV	
Input HS-Switch	$V_{ESD}$	–	1	kV	
Status HS-Switch	$V_{ESD}$	–	2	kV	
Output LS and HS-Switch	$V_{ESD}$	–	8	kV	all other pins connected to Ground

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.*

### 3.2 Operating Range

$$-40\text{ °C} < T_j < 150\text{ °C}$$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_S$	$V_{UVOFF}$	42	V	After $V_S$ rising above $V_{UVON}$
Input voltages	$V_{IH}$	– 0.3	15	V	–
Input voltages	$V_{IL}$	– 0.3	10	V	–
Output current	$I_{ST}$	0	2	mA	–
Junction temperature	$T_j$	– 40	150	°C	–

*Note: In the operating range the functions given in the circuit description are fulfilled.*



### 3.3 Electrical Characteristics

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$ ;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ;  $8 \text{ V} < V_S < 18 \text{ V}$   
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### Current Consumption HS-switch

Quiescent current	$I_S$	–	5	8	$\mu\text{A}$	$I_{H1} = I_{H2} = 0 \text{ V}$ $T_j = 25 \text{ }^\circ\text{C}$
		–	–	12	$\mu\text{A}$	$I_{H1} = I_{H2} = 0 \text{ V}$
Supply current	$I_S$	–	2.2	4.2	$\text{mA}$	$I_{H1}$ or $I_{H2} = 5 \text{ V}$ $V_S = 12 \text{ V}$
		–	4.4	8.4	$\text{mA}$	$I_{H1}$ and $I_{H2} = 5 \text{ V}$ $V_S = 12 \text{ V}$
Leakage current of high-side switch	$I_{SHLK}$	–	–	6	$\mu\text{A}$	$V_{IH} = V_{SH} = 0 \text{ V}$
Leakage current through logic GND in free wheeling condition	$I_{LKCL} = I_{FH} + I_{SH}$	–	–	10	$\text{mA}$	$I_{FH} = 3 \text{ A}$

#### Current Consumption LS-switch

Input current	$I_{IL}$	–	8	30	$\mu\text{A}$	$V_{IL} = 5 \text{ V}$ ; normal operation
		–	160	300	$\mu\text{A}$	$V_{IL} = 5 \text{ V}$ ; failure mode
Leakage current of low-side switch	$I_{DLK}$	–	2	10	$\mu\text{A}$	$V_{IL} = 0 \text{ V}$

#### Under Voltage Lockout (UVLO) HS-switch

Switch-ON voltage	$V_{UVON}$	–	–	4.8	$\text{V}$	$V_S$ increasing
Switch-OFF voltage	$V_{UVOFF}$	1.8	–	3.5	$\text{V}$	$V_S$ decreasing
Switch ON/OFF hysteresis	$V_{UVHY}$	–	1	–	$\text{V}$	$V_{UVON} - V_{UVOFF}$

### 3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$ ;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ;  $8 \text{ V} < V_s < 18 \text{ V}$   
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### Output stages

Inverse diode of high-side switch; Forward-voltage	$V_{FH}$	–	0.8	1.2	V	$I_{FH} = 3 \text{ A}$
Inverse diode of low-side switch; Forward-voltage	$V_{FL}$	–	0.8	1.2	V	$I_{FL} = 3 \text{ A}$
Static drain-source on-resistance of high-side switch	$R_{DS\ ON\ H}$	–	70	90	m $\Omega$	$I_{SH} = 1 \text{ A}$ $T_j = 25 \text{ }^\circ\text{C}$
Static drain-source on-resistance of low-side switch	$R_{DS\ ON\ L}$	–	45	60	m $\Omega$	$I_{SL} = 1 \text{ A}$ ; $V_{GL} = 5 \text{ V}$ $T_j = 25 \text{ }^\circ\text{C}$
Static path on-resistance	$R_{DS\ ON}$	–	–	285	m $\Omega$	$R_{DS\ ON\ H} + R_{DS\ ON\ L}$ $I_{SH} = 1 \text{ A}$ ;

#### Short Circuit of high-side switch to GND

Initial peak SC current	$I_{SCP\ H}$	15		23	A	$T_j = -40 \text{ }^\circ\text{C}$
		11.5		18	A	$T_j = +25 \text{ }^\circ\text{C}$
		8		11.5	A	$T_j = +150 \text{ }^\circ\text{C}$

#### Short Circuit of high-side switch to $V_s$

Output pull-down-resistor	$R_O$	8	15	35	k $\Omega$	$V_{DSL} = 3 \text{ V}$
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#### Short Circuit of low-side switch to $V_s$

Initial peak SC current	$I_{SCP\ L}$	23	28	34	A	$T_j = -40 \text{ }^\circ\text{C}$
		18	22	27	A	$T_j = 25 \text{ }^\circ\text{C}$
		11.5	14	18	A	$T_j = 150 \text{ }^\circ\text{C}$

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions. Protection functions are not designed for continuous or repetitive operation.

### 3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$ ;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ;  $8 \text{ V} < V_S < 18 \text{ V}$   
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### Thermal Shutdown

Thermal shutdown junction temperature	$T_{jSD}$	155	180	190	$^\circ\text{C}$	–
Thermal switch-on junction temperature	$T_{jSO}$	150	170	180	$^\circ\text{C}$	–
Temperature hysteresis	$\Delta T$	–	10	–	$^\circ\text{C}$	$\Delta T = T_{jSD} - T_{jSO}$

#### Status Flag Output ST of high-side switch

Low output voltage	$V_{STL}$	–	0.2	0.6	V	$I_{ST} = 1.6 \text{ mA}$
Leakage current	$I_{STLK}$	–	–	10	$\mu\text{A}$	$V_{ST} = 5 \text{ V}$
Zener-limit-voltage	$V_{STZ}$	5.4		–	V	$I_{ST} = 1.6 \text{ mA}$

#### Open load detection in Off condition

Open load detection voltage	$V_{OUT(OL)}$	1.8	2.8	4	V	
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#### Switching times of high-side switch

Turn-ON-time; to 90% $V_{SH}$	$t_{ON}$	–	85	180	$\mu\text{s}$	$R_{Load} = 12 \text{ } \Omega$ $V_S = 12 \text{ V}$
Turn-OFF-time; to 10% $V_{SH}$	$t_{OFF}$	–	80	180	$\mu\text{s}$	$R_{Load} = 12 \text{ } \Omega$ $V_S = 12 \text{ V}$
Slew rate on 10 to 30% $V_{SH}$	$dV/dt_{ON}$	–	–	1.2	V/ $\mu\text{s}$	$R_{Load} = 12 \text{ } \Omega$ $V_S = 12 \text{ V}$
Slew rate off 70 to 40% $V_{SH}$	$-dV/dt_{OFF}$	–	–	1.5	V/ $\mu\text{s}$	$R_{Load} = 12 \text{ } \Omega$ $V_S = 12 \text{ V}$

Note: switching times are not subject to production tests - specified by design

### 3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$ ;  $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$ ;  $8 \text{ V} < V_S < 18 \text{ V}$   
 unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### Switching times of low-side switch

Turn ON time to 10% $V_{DL}$ $V_{IL} = 0 \text{ to } 10 \text{ V}$	$t_{ON}$	–	65	150	$\mu\text{s}$	$R_{Load} = 10 \text{ } \Omega$ $V_S = 12 \text{ V}$
Turn OFF time; to 90% $V_{DL}$	$t_{OFF}$	–	55	150	$\mu\text{s}$	$R_{Load} = 10 \text{ } \Omega$ $V_S = 12 \text{ V}$
Slew rate on 70 to 50% $V_{SH}$ $V_{IL} = 0 \text{ to } 10 \text{ V}$	$-dV/dt_{ON}$	–	–	1.5	$\text{V}/\mu\text{s}$	$R_{Load} = 4.7 \text{ } \Omega$ $V_S = 12 \text{ V}$
Slew rate off 50 to 70% $V_{SH}$ $V_{IL} = 0 \text{ to } 10 \text{ V}$	$dV/dt_{OFF}$	–	–	1.5	$\text{V}/\mu\text{s}$	$R_{Load} = 4.7 \text{ } \Omega$ $V_S = 12 \text{ V}$

Note: switching times are not subject to production tests - specified by design

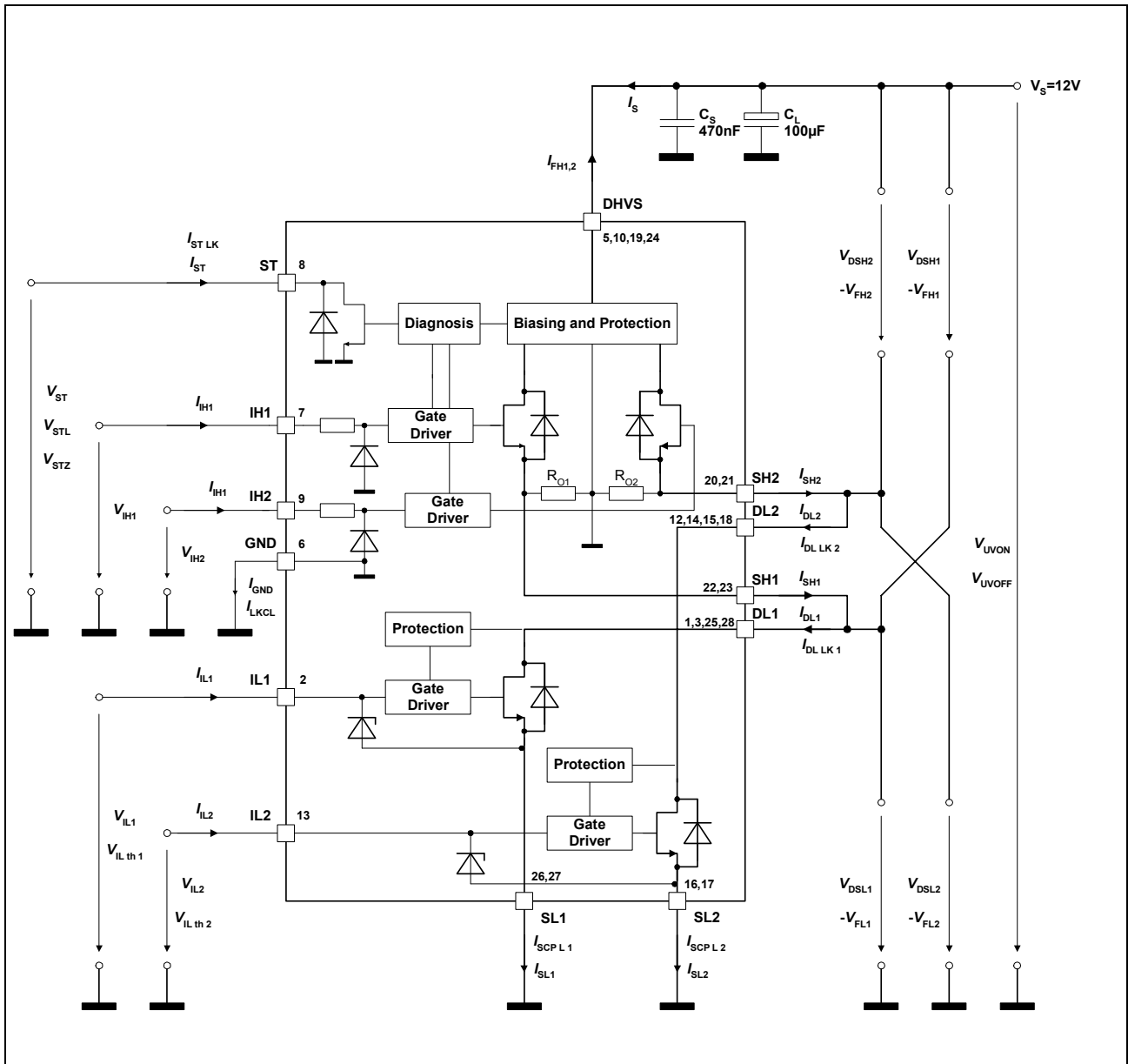
#### Control Inputs of high-side switches GH 1, 2

H-input voltage	$V_{IH \text{ High}}$	–	–	2.5	V	–
L-input voltage	$V_{IH \text{ Low}}$	1	–	–	V	–
Input voltage hysteresis	$V_{IH \text{ HY}}$	–	0.3	–	V	–
H-input current	$I_{IH \text{ High}}$	15	30	60	$\mu\text{A}$	$V_{IH} = 5 \text{ V}$
L-input current	$I_{IH \text{ Low}}$	5	–	20	$\mu\text{A}$	$V_{IH} = 0.4 \text{ V}$
Input series resistance	$R_I$	2.7	4	5.5	$\text{k}\Omega$	–
Zener limit voltage	$V_{IH \text{ Z}}$	5.4	–	–	V	$I_{IH} = 1.6 \text{ mA}$

#### Control Inputs GL1, 2

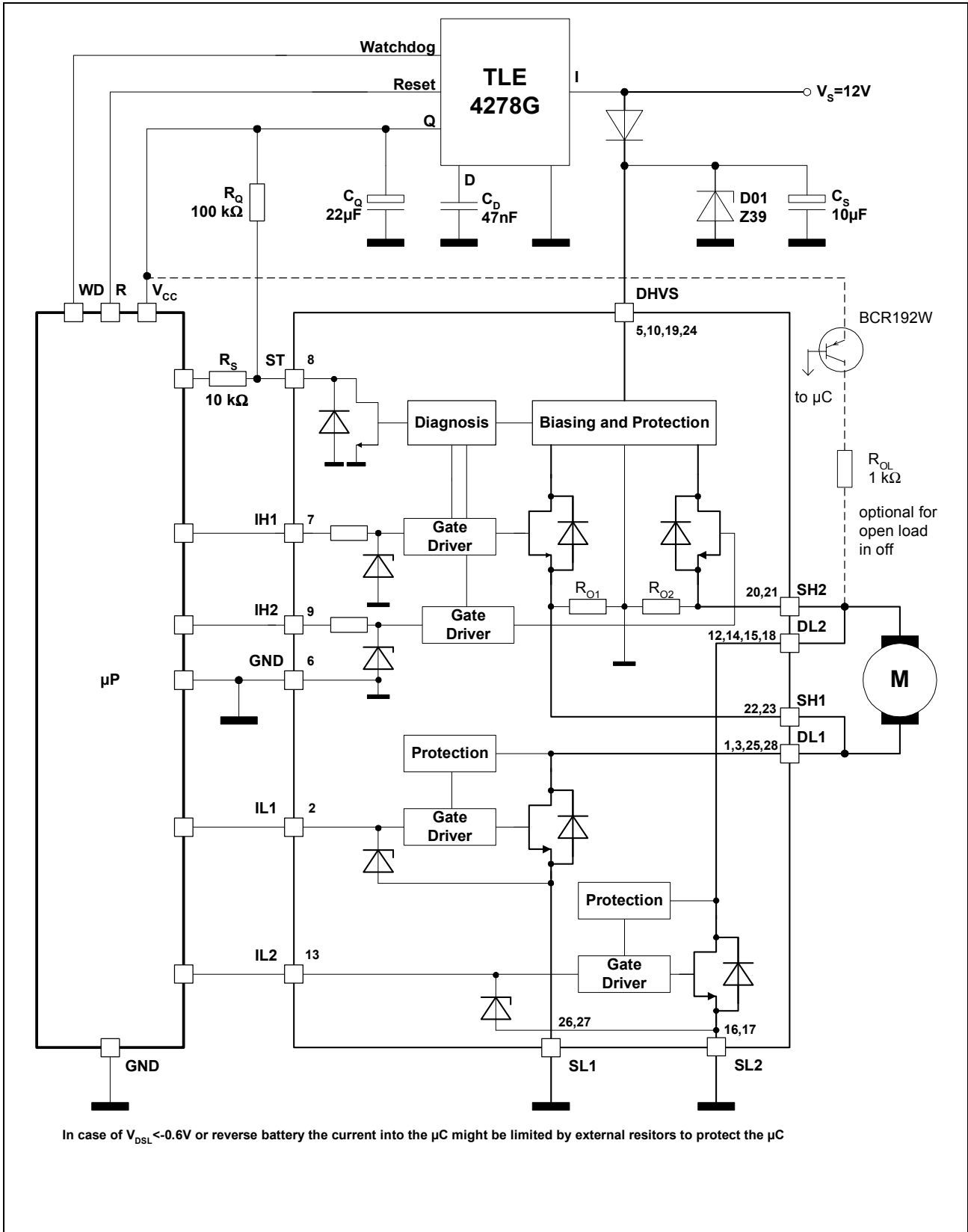
Gate-threshold-voltage	$V_{IL \text{ th}}$	0.9	1.7	2.2	V	$I_{DL} = 2 \text{ mA}$
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Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25 \text{ }^\circ\text{C}$  and the given supply voltage.



**Figure 3**  
**Test Circuit**

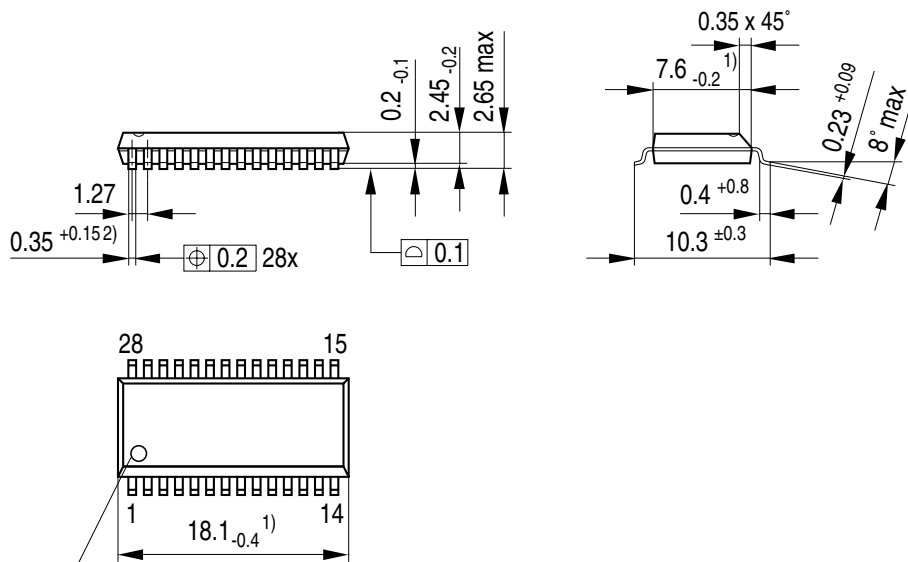
HS-Source-Current	Named during Short Circuit	Named during Leakage-Cond.
$I_{SH1,2}$	$I_{SCP H}$	$I_{DL LK}$



**Figure 4**  
**Application Circuit**

#### 4 Package Outlines

**P-DSO-28-14**  
(Plastic Transistor Single Outline Package)



Index Marking

- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.05 max per side

GPS05123

GPS05123

#### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

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