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NTE949
Integrated Circuit
Dual Audio Operational Amplifier/Preamplifier

Description:

The NTE949 consists of two identical high gain OP Amps constructed on a single 8–Lead Metal Can type package. These three–stage amplifiers use Class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from DC to 10MHz, where two high performance operational amplifiers are required. In addition, the outputs may be wired–OR for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers and peak detectors.

Features:

- Single or Dual Supply Operation
- Low Power Consumption
- High Gain: 25,000 V/V
- Large Common Mode Range: +11V, –13V
- Excellent Gain Stability vs. Supply Voltage
- No Latch–Up
- Output Short Circuit Protected

Absolute Maximum Ratings:

Supply Voltage, V+, V– . . . . ±18V
Internal Power Dissipation (T_A = +70°C), P_D 500mW
Derate Above 70°C . . . . 6.8mW/°C
Input Differential Voltage, V_{ID} . . . . ±5V
Input Common–Mode Range (Note 1), V_{ICR} . . . . ±15V
Storage Temperature Range, T_{stg} . . . . –65° to +150°C
Operating Temperature Range, T_{opr} . . . . 0° to +70°C
Lead Temperature (During Soldering, 60s), T_L . . . . +300°C
Output Short–Circuit Duration (T_A = +25°C, Note 2), t_{OS} 30sec

Note 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Short circuit may be to GND or either supply.

Electrical Characteristics: (V+ = ±15V, R_L = 5kΩ to Pin7, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	R_S = 200Ω		–	1.0	6.0	mV
			T_A = 0° to +70°C	–	1.0	9.0	mV
			V_+ = ±4V, R_L = 10kΩ to Pin7	–	–	6.0	mV
Input Offset Current	I_{IO}			–	50	750	nA
		T_A = +70°C		–	0.5	1.5	µA
		T_A = 0°C		–	0.5	1.5	µA
		V+ = 4V, R_L = 10kΩ to Pin7		–	50	600	µA
Input Bias Current	I_{IB}			–	0.3	1.5	µA
		T_A = +70°C		–	0.3	3.0	µA
		T_A = 0°C		–	0.3	3.0	µA
		V+ = 4V, R_L = 10kΩ to Pin7		–	0.3	1.5	µA
Input Resistance	r_i			50	150	–	kΩ
Large Signal Voltage Gain	A_V	V_{OUT} = ±10V		15000	50000	–	V/V
		V_+ = ±4V, R_L = 10kΩ to Pin7, V_{OUT} = ±2V		15000	60000	–	V/V
Positive Output Voltage Swing	V_O			+12	+13	–	V
		T_A = 0° to +70°C		+12	+13	–	V
		V_+ = ±4V, R_L = 10kΩ to Pin7		+2.5	+2.8	–	V
Negative Output Voltage Swing	V_O			–14	–15	–	V
		T_A = 0° to +70°C		–14	–15	–	V
		V_+ = ±4V, R_L = 10kΩ to Pin7		–3.6	–4.0	–	V
Output Resistance	r_o	f = 1kHz		–	5.0	–	kΩ
Common Mode Rejection Ratio	CMRR	R_S = 200Ω, V_{IN} = +11.5V to –13.5V		70	90	–	dB
Supply Voltage Rejection Ratio	PSRR	R_S = 200Ω		–	50	350	µV/V
Input Voltage Range	V_I			–13	–	+11	V
Internal Power Dissipation		V_{OUT} = 0		–	180	330	mW
			V_+ = ±4V, R_L = 10kΩ to Pin7	–	20	–	mW
Supply Current	I_{CC}, I_{EE}	V_{OUT} = 0		–	9.0	14.0	mA
			V_+ = ±4V, R_L = 10kΩ to Pin7	–	2.5	–	mA
Broadband Noise Figure		R_S = 10kΩ, BW = 10Hz to 10kHz		–	2.5	–	dB
Turn On Delay	t_{on}	Open Loop, V_{IN} = ±20mV		–	0.2	–	µs
Turn Off Delay	t_{off}	Open Loop, V_{IN} = ±20mV		–	0.3	–	µs
Slew Rate (Unity Gain)	SR	C_1 = 0.02µF, R_1 = 33Ω, C_2 = 10pF		–	1.0	–	V/µs
Channel Separation		R_S = 1kΩ, f = 10kHz		–	140	–	dB
Input Offset Voltage Drift		R_S = 200Ω	+25°C ≤ T_A ≤ +70°C	–	3.0	–	µV/°C
			0°C ≤ T_A ≤ +25°C	–	3.0	–	µV/°C

Pin Connection Diagram
(Top View)