



FLASH-ROM MODULE 4MByte (1M x 32-Bit), 72pin-SIMM, 5V
Part No. HMF1M32M8G

GENERAL DESCRIPTION

The HMF1M32M8G is a high-speed flash read only memory (FROM) module containing 1,048,576 words organized in a x32bit configuration. The module consists of eight 512K x 8 FROM mounted on a 72 -pin, single-sided, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Eight chip enable inputs, (/CE_UU1, /CE_UM1, /CE_LM1, /CE_LL1, /CE_UU2, /CE_UM2, /CE_LM2, /CE_LL2) are used to enable the module's 4 bytes independently. Output enable (/OE) and write enable (/WE) can set the memory input and output. When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +5V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- w Access time: 55, 70, 90 and 120ns
- w High-density 4MByte design
- w High-reliability, low-power design
- w Single + 5V \pm 0.5V power supply
- w Easy memory expansion
- w All inputs and outputs are TTL-compatible
- w FR4-PCB design
- w Low profile 72-pin SIMM
- w Minimum 1,000,000 write/erase cycle
- w Sector erases architecture
- w Sector group protection
- w Temporary sector group unprotection

OPTIONS

w Timing

| | |
|--------------|------|
| 55ns access | -55 |
| 70ns access | -70 |
| 90ns access | -90 |
| 120ns access | -120 |

w Packages

| | |
|-------------|---|
| 72-pin SIMM | M |
|-------------|---|

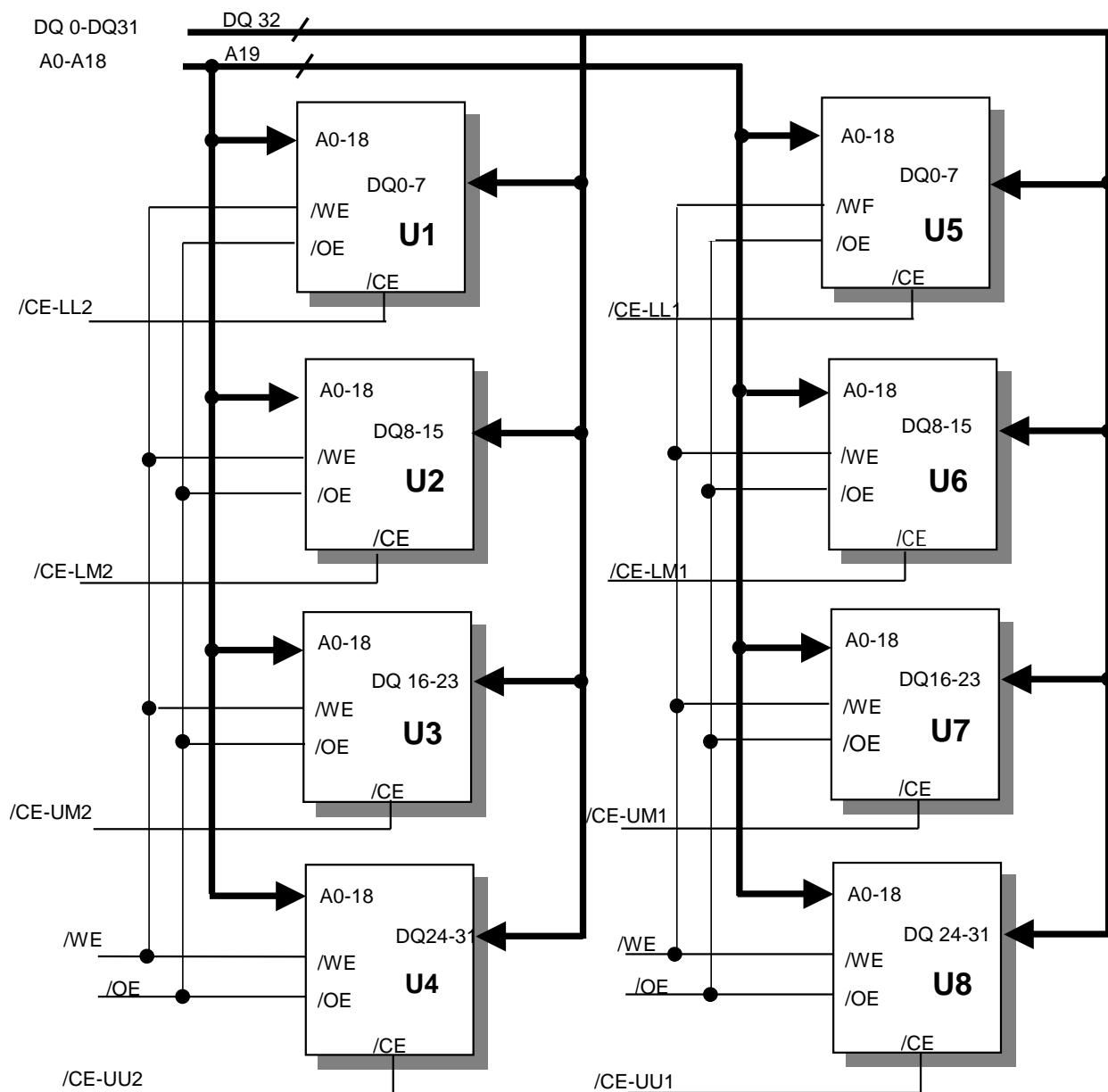
MARKING

PIN ASSIGNMENT

| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|-----|---------|-----|---------|-----|---------|
| 1 | Vss | 25 | Vcc | 49 | DQ17 |
| 2 | A3 | 26 | DQ8 | 50 | DQ18 |
| 3 | A2 | 27 | DQ9 | 51 | DQ22 |
| 4 | A1 | 28 | DQ10 | 52 | DQ21 |
| 5 | A0 | 29 | /CE_LM2 | 53 | DQ20 |
| 6 | Vcc | 30 | Vcc | 54 | DQ19 |
| 7 | A11 | 31 | /CE_LM1 | 55 | Vcc |
| 8 | /OE | 32 | DQ15 | 56 | A15 |
| 9 | A10 | 33 | DQ14 | 57 | A12 |
| 10 | Vcc | 34 | DQ13 | 58 | A7 |
| 11 | /CE_LL2 | 35 | DQ12 | 59 | Vcc |
| 12 | /CE_LL1 | 36 | DQ11 | 60 | A8 |
| 13 | DQ7 | 37 | A18 | 61 | A9 |
| 14 | DQ0 | 38 | A16 | 62 | DQ24 |
| 15 | DQ1 | 39 | Vss | 63 | DQ25 |
| 16 | DQ2 | 40 | A6 | 64 | DQ26 |
| 17 | DQ6 | 41 | Vcc | 65 | /CE_UU2 |
| 18 | DQ5 | 42 | A5 | 66 | /CE_UU1 |
| 19 | DQ4 | 43 | A4 | 67 | DQ31 |
| 20 | DQ3 | 44 | Vcc | 68 | DQ30 |
| 21 | /WE | 45 | /CE_UM2 | 69 | DQ29 |
| 22 | A17 | 46 | /CE_UM1 | 70 | DQ28 |
| 23 | A14 | 47 | DQ23 | 71 | DQ27 |
| 24 | A13 | 48 | DQ16 | 72 | Vss |

72-PIN SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

| MODE | /OE | /CE | /WE | DQ | POWER |
|----------------|-----|-----|-----|--------|---------|
| STANDBY | X | H | X | HIGH-Z | STANDBY |
| NOT SELECTED | H | L | H | HIGH-Z | ACTIVE |
| READ | L | L | H | Q | ACTIVE |
| WRITE or ERASE | X | L | L | D | ACTIVE |

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING |
|---|--------------|-----------------|
| Voltage with respect to ground all other pins | $V_{IN,OUT}$ | -2.0V to +7.0V |
| Voltage with respect to ground V_{CC} | V_{CC} | -2.0V to +7.0V |
| Storage Temperature | T_{STG} | -65°C to +125°C |
| Operating Temperature | T_A | -55°C to +125°C |

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP. | MAX |
|--|----------|-------|------|-------|
| V_{CC} for $\pm 5\%$ device Supply Voltages | V_{CC} | 4.75V | | 5.25V |
| V_{CC} for $\pm 10\%$ device Supply Voltages | V_{CC} | 4.5V | | 5.5V |
| Ground | V_{SS} | 0 | 0 | 0 |

DC AND OPERATING CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 5\text{V} \pm 0.5\text{V}$)

| PARAMETER | TEST CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|---|---|-----------|-----|-----------|---------------|
| Input Leakage Current | $V_{CC}=V_{CC} \text{ max, } V_{IN}=\text{GND to } V_{CC}$ | I_{L1} | | ± 1.0 | μA |
| Output Leakage Current | $V_{CC}=V_{CC} \text{ max, } V_{OUT}=\text{GND to } V_{CC}$ | I_{L0} | | ± 1.0 | μA |
| Output High Voltage | $I_{OH} = -2.5\text{mA, } V_{CC} = V_{CC} \text{ min}$ | V_{OH} | 2.4 | | V |
| Output Low Voltage | $I_{OL} = 12\text{mA, } V_{CC} = V_{CC} \text{ min}$ | V_{OL} | | 0.45 | V |
| V_{CC} Active Current for Read(1) | $/\text{CE} = V_{IL}, /\text{OE} = V_{IH}$ | I_{CC1} | | 12 | mA |
| V_{CC} Active Current for Program or Erase(2) | $/\text{CE} = V_{IL}, /\text{OE} = V_{IH}$ | I_{CC2} | | 40 | mA |
| V_{CC} Standby Current | $/\text{CE} = V_{IH}$ | I_{CC3} | | 1.0 | mA |
| Low V_{CC} Lock-Out Voltage | | V_{LKO} | 3.2 | 4.2 | V |

Notes:

1. The I_{CC} current listed is typically less than 2mA/MHz, with $/\text{OE}$ at V_{IH} .
2. I_{CC} active while embedded algorithm (program or erase) is in progress
3. Maximum I_{CC} current specifications are tested with $V_{CC}=V_{CC} \text{ max}$

ERASE AND PROGRAMMING PERFORMANCE

| PARAMETER | LIMITS | | | UNIT | COMMENTS |
|-----------------------|--------|------|------|------|---|
| | MIN. | TYP. | MAX. | | |
| Sector Erase Time | - | 1 | 8 | sec | Excludes 00H programming prior to erasure |
| Byte Programming Time | - | 7 | 300 | μs | Excludes system-level overhead |
| Chip Programming Time | - | 3.6 | 10.8 | sec | Excludes system-level overhead |

CAPACITANCE

| PARAMETER SYMBOL | PARAMETER DESCRIPTION | TEST SETUP | TYP. | MAX | UNIT |
|------------------|-------------------------|----------------------|------|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = 0 | 4 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0 | 8 | 12 | pF |
| C _{IN2} | Control Pin Capacitance | V _{IN} = 0 | 8 | 12 | pF |

Notes : Test conditions T_A = 25°C, f=1.0 MHz.

AC CHARACTERISTICS

└ Read Only Operations Characteristics

| PARAMETER SYMBOLS | | DESCRIPTION | TEST SETUP | | -55 | -90 | UNIT |
|-------------------|------------------|--|--|-----|-----|-----|------|
| JEDEC | STANDARD | | | | | | |
| t _{AVAV} | t _{RC} | Read Cycle Time | | Min | 55 | 90 | ns |
| t _{AVQV} | t _{ACC} | Address to Output Delay | /CE = V _{IL} /OE = V _{IL} | Max | 55 | 90 | ns |
| t _{ELQV} | t _{CE} | Chip Enable to Output Delay | /OE = V _{IL} | Max | 55 | 90 | ns |
| t _{GLQV} | t _{OE} | Chip Enable to Output Delay | | Max | 30 | 35 | ns |
| t _{EHQZ} | t _{DF} | Chip Enable to Output High-Z | | Max | 18 | 20 | ns |
| t _{GHQZ} | t _{DF} | Output Enable to Output High-Z | | Max | 18 | 20 | ns |
| t _{AXQX} | t _{QH} | Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First | | Min | 0 | 0 | ns |

Notes : Test Conditions : Output Load : 1TTL gate and Output Load Capacitance 100 pF, in case of 55ns-30pF

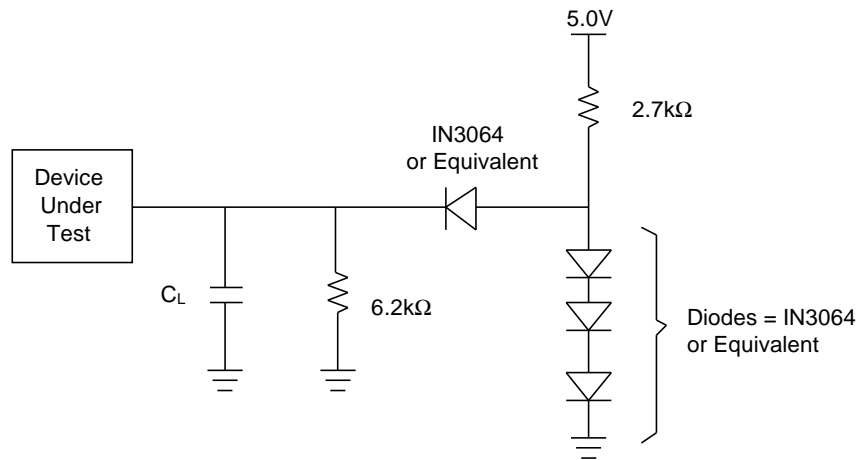
Input rise and fall times : 5 ns, In case of 55ns-5ns

Input pulse levels : 0.45V to 2.4V, In case of 55ns- 0.0V-3.0V

Timing measurement reference level

Input : 0.8V, In case of 55ns-1.5V

Output : 2.0V, In case of 55ns-1.5V



Note : CL = 100pF including jig capacitance

u Erase/Program Operations

| PARAMETER SYMBOLS | | DESCRIPTION | | -55 | -90 | UNIT |
|-------------------|----------|--------------------------------|-----|-----|-----|------|
| JEDEC | STANDARD | | | | | |
| tAVAV | tWC | Write Cycle Time | Min | 55 | 90 | ns |
| tAVWL | tAS | Address Setup Time | Min | 0 | 0 | ns |
| tWLAX | tAH | Address Hold Time | Min | 40 | 45 | ns |
| tDVWH | tDS | Data Setup Time | Min | 25 | 45 | ns |
| tWHDX | tDH | Data Hold Time | Min | 0 | 0 | ns |
| | tOES | Output Enable Setup Time | Min | 0 | 0 | ns |
| tGHWL | tGHWL | Read Recover Time Before Write | Min | 0 | 0 | ns |
| tELWL | tCS | /CE Setup Time | Min | 0 | 0 | ns |
| tWHEH | tCH | /CE Hold Time | Min | 0 | 0 | ns |
| tWLWH | tWP | Write Pulse Width | Min | 30 | 45 | ns |
| tWHWL | tWPH | Write Pulse Width High | Min | 20 | 20 | ns |
| tWHWH1 | tWHWH1 | Byte Programming Operation | Typ | 7 | 7 | μs |
| tWHWH2 | tWHWH2 | Sector Erase Operation (Note1) | Typ | 1 | 1 | sec |
| | tVCS | Vcc set up time | Min | 50 | 50 | μs |

Notes :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

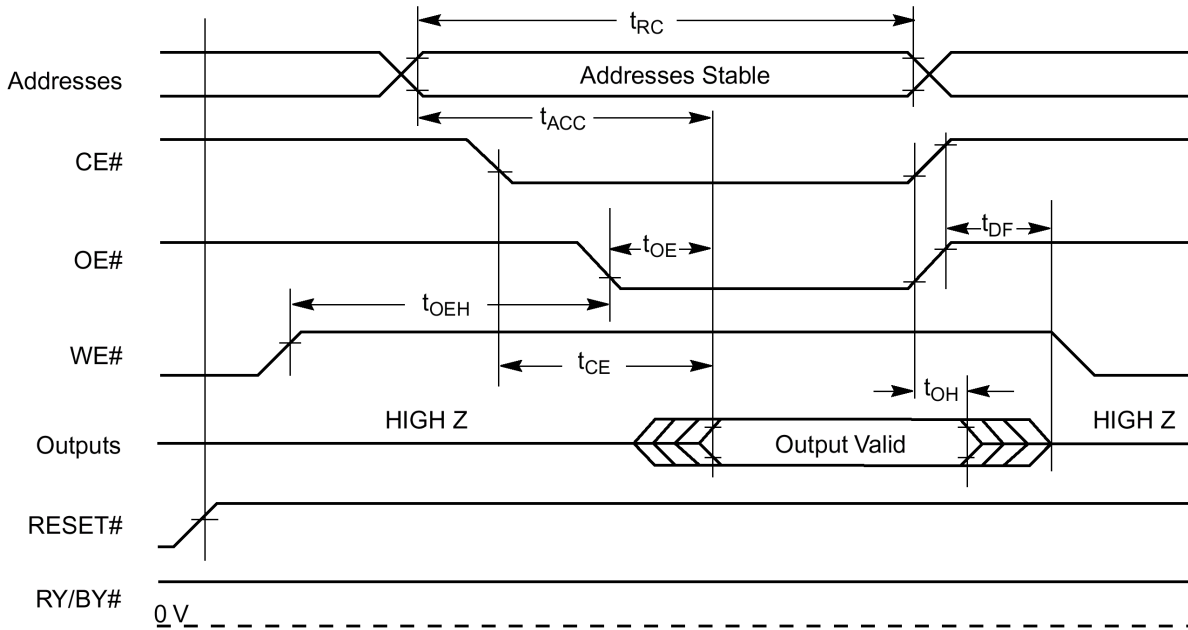
U Erase/Program Operations

Alternate /CE Controlled Writes

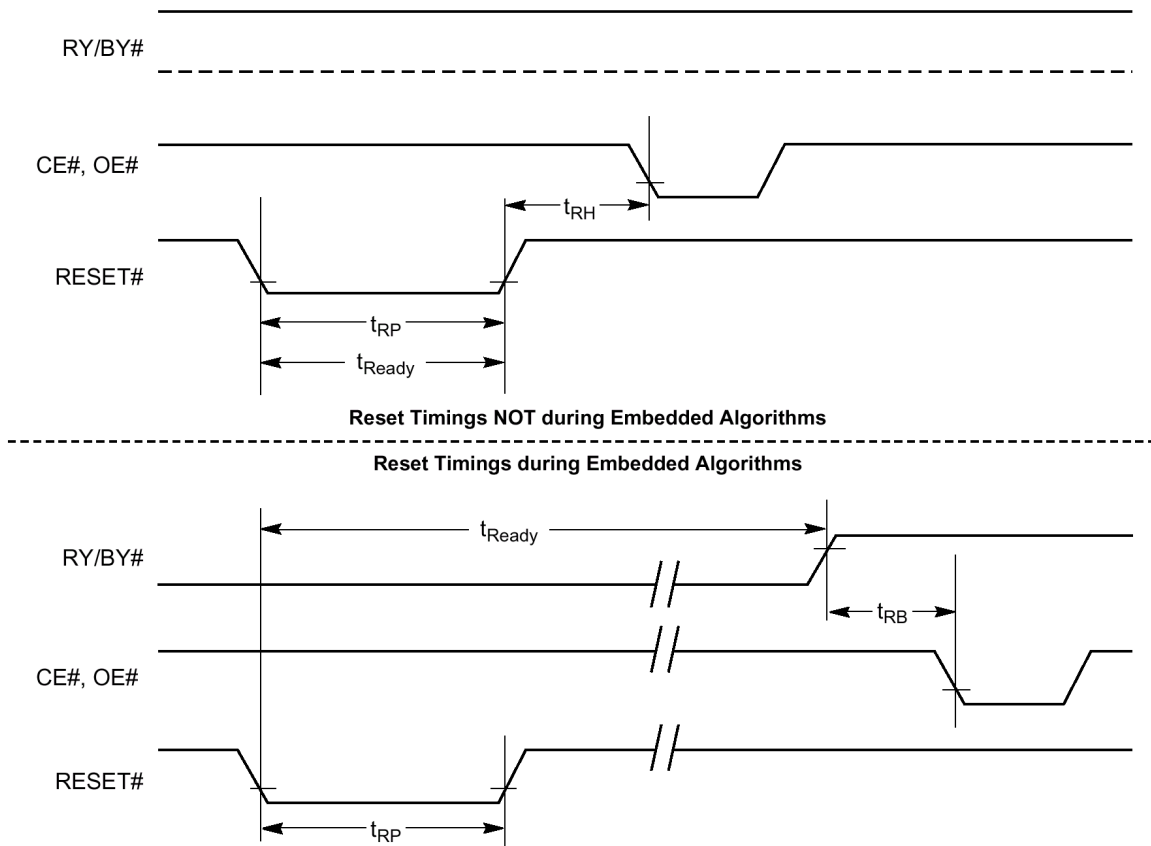
| PARAMETER SYMBOLS | | DESCRIPTION | | -55 | -90 | UNIT |
|--------------------|--------------------|--------------------------------|-----|-----|-----|------|
| JEDEC | STANDARD | | | | | |
| t _{AVAV} | t _{WC} | Write Cycle Time | Min | 55 | 90 | ns |
| t _{AVEL} | t _{AS} | Address Setup Time | Min | 0 | 0 | ns |
| t _{ELAX} | t _{AH} | Address Hold Time | Min | 40 | 45 | ns |
| t _{DVEH} | t _{DS} | Data Setup Time | Min | 25 | 45 | ns |
| t _{EHDX} | t _{DH} | Data Hold Time | Min | 0 | 0 | ns |
| | t _{OES} | Output Enable Setup Time | Min | 0 | 0 | ns |
| t _{GHEL} | t _{GHEL} | Read Recover Time Before Write | Min | 0 | 0 | ns |
| t _{WLEL} | t _{WS} | /WE Setup Time | Min | 0 | 0 | ns |
| t _{EHWH} | t _{WH} | /WE Hold Time | Min | 0 | 0 | ns |
| t _{ELEH} | t _{CP} | /CE Pulse Width | Min | 30 | 45 | ns |
| t _{EHEL} | t _{CPH} | /CE Pulse Width High | Min | 20 | 20 | ns |
| t _{WHWH1} | t _{WHWH1} | Byte Programming Operation | Typ | 7 | 7 | μs |
| t _{WHWH2} | t _{WHWH2} | Sector Erase Operation (Note) | Typ | 1 | 1 | sec |

Notes : This does not include the preprogramming time.

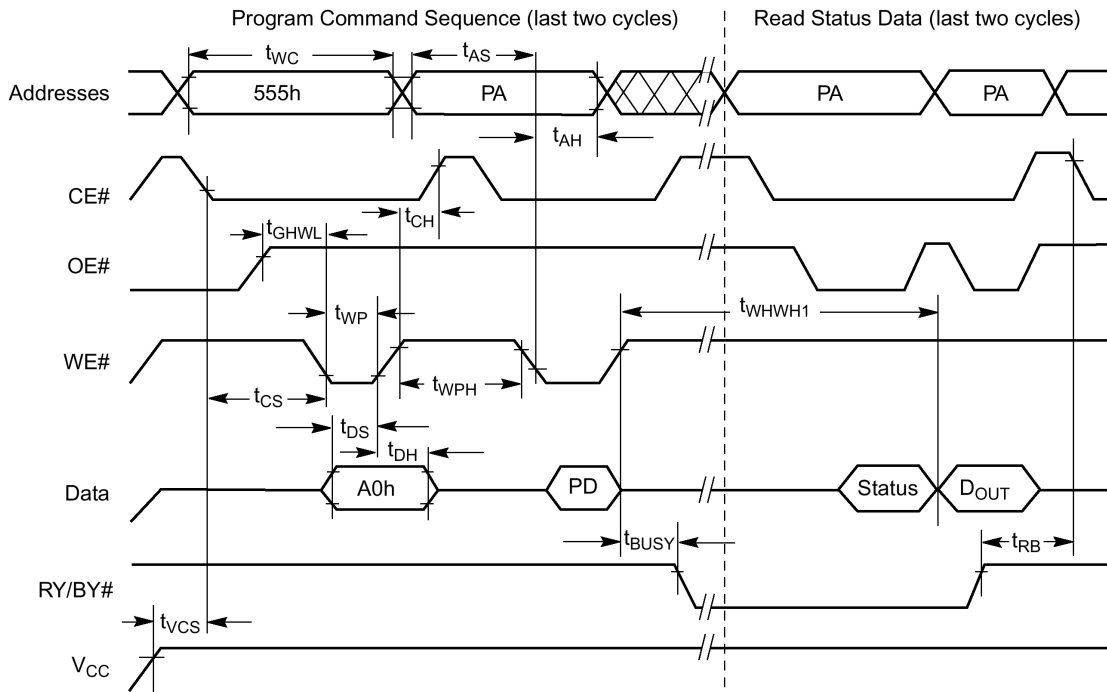
⌌ READ OPERATIONS TIMING



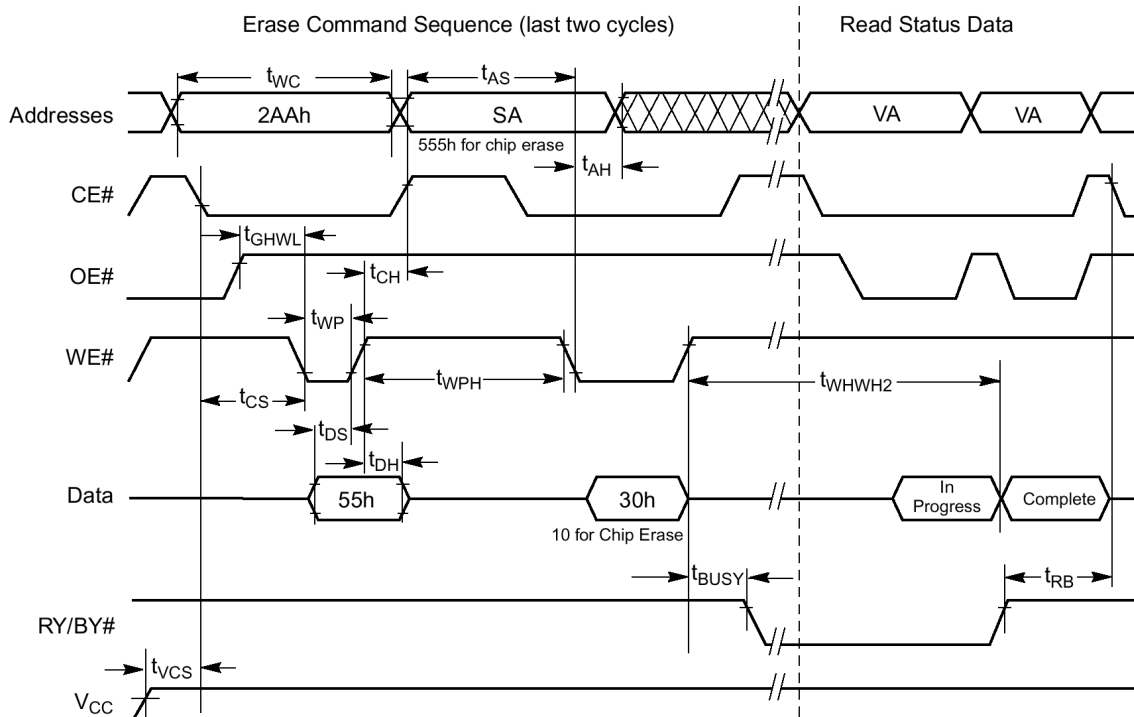
⌌ RESET TIMING



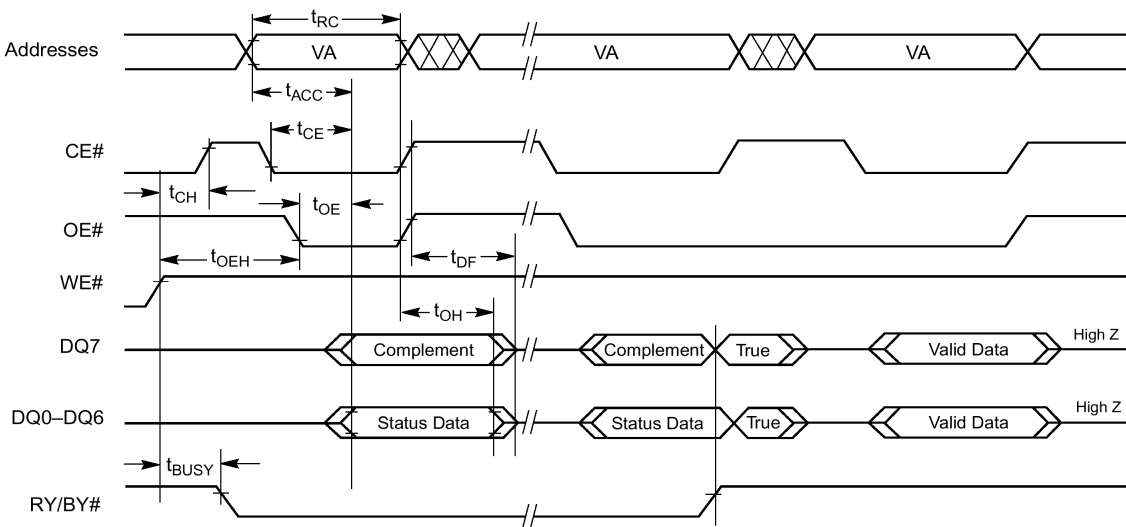
PROGRAM OPERATIONS TIMING



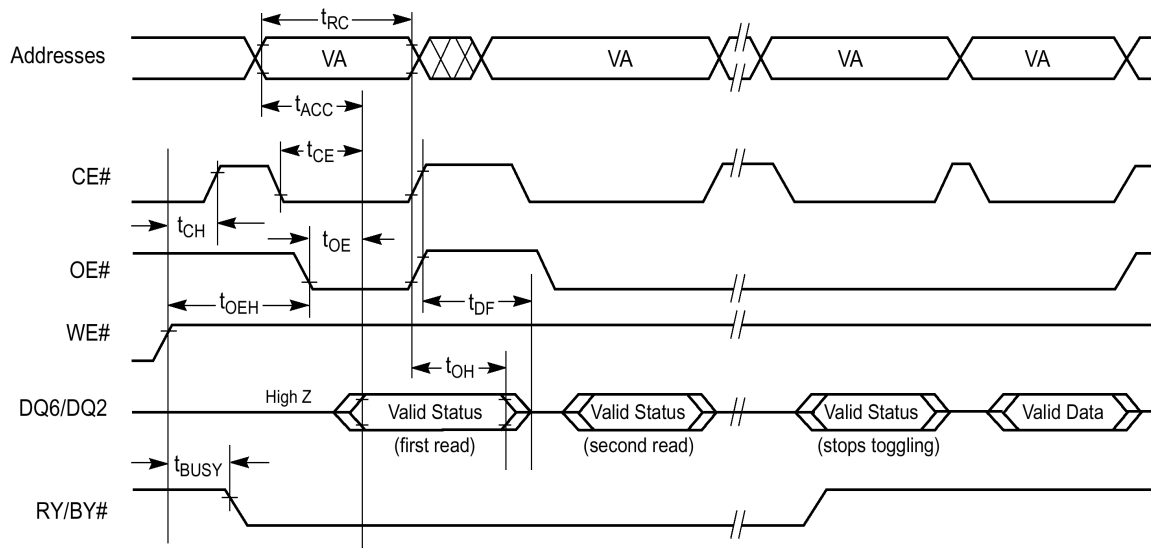
CHIP/SECTOR ERASE OPERATION TIMINGS



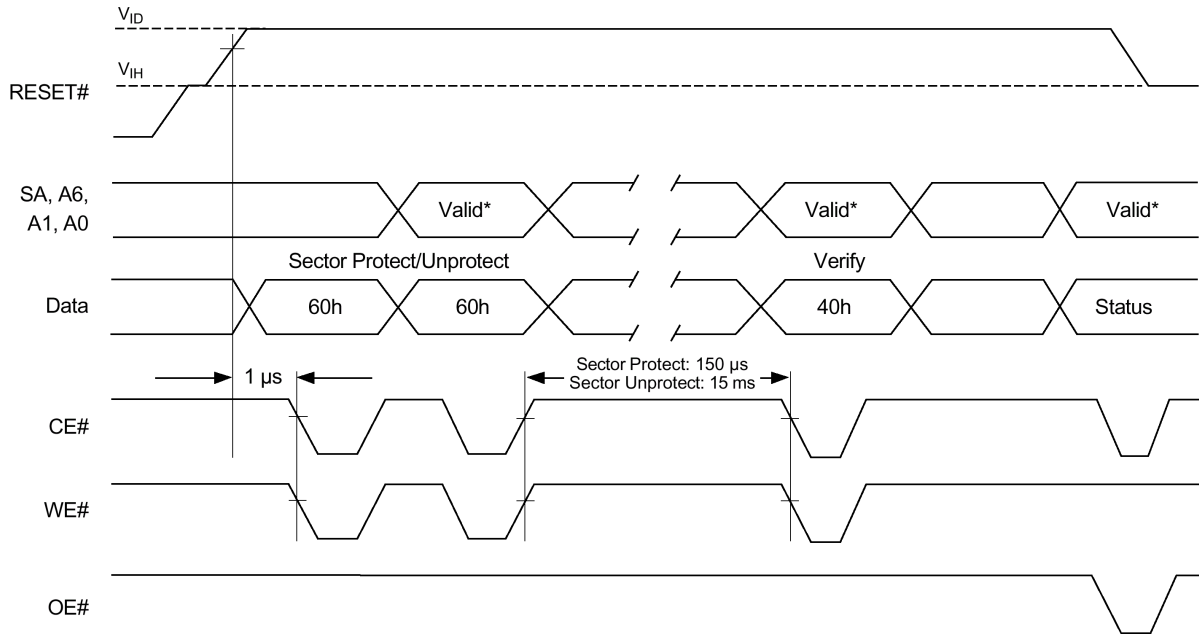
U DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



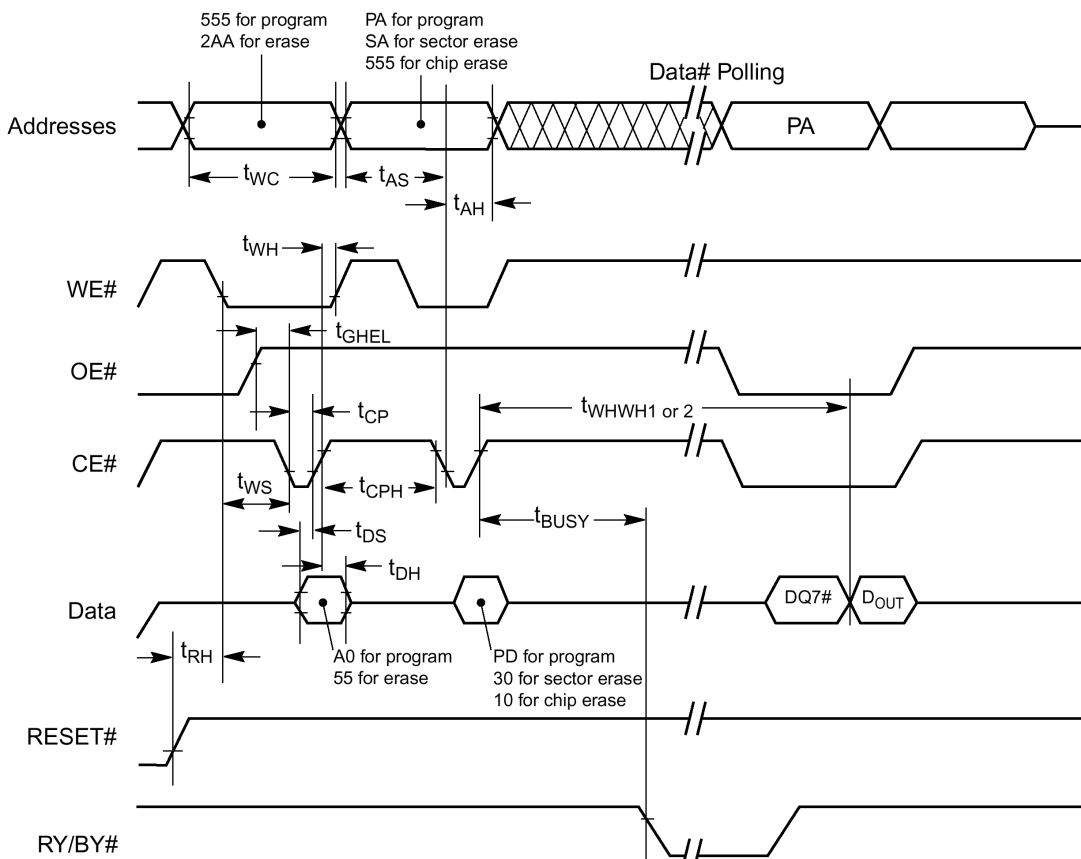
U TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



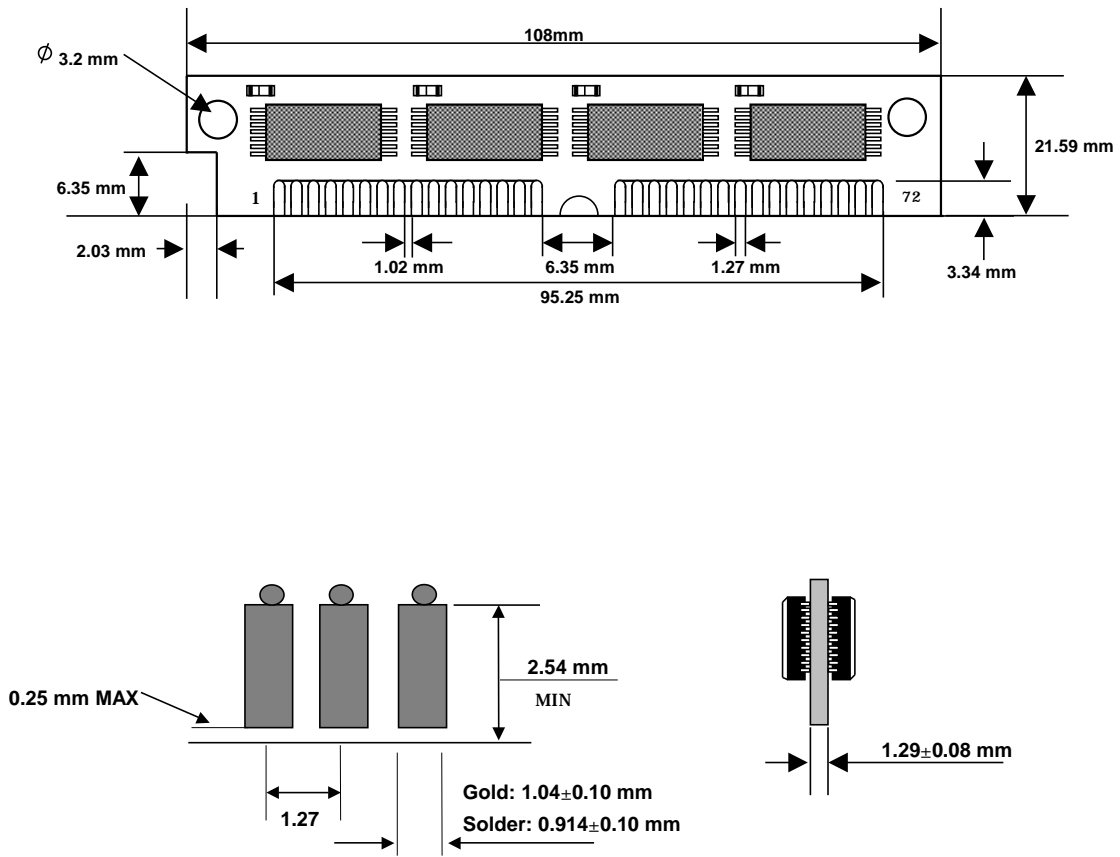
U SECTOR PROTECT UNPROTECT TIMEING DIAGRAM



U ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS



(Solder & Gold Plating)

ORDERING INFORMATION

| Part Number | Density | Org. | Package | Component Number | Vcc | SPEED |
|----------------|---------|----------|------------|------------------|------|-------|
| HMF1M32M8G-55 | 4MByte | 1M×32bit | 72pin-SIMM | 8EA | 5.0V | 55ns |
| HMF1M32M8G-70 | 4MByte | 1M×32bit | 72pin-SIMM | 8EA | 5.0V | 70ns |
| HMF1M32M8G-90 | 4MByte | 1M×32bit | 72pin-SIMM | 8EA | 5.0V | 90ns |
| HMF1M32M8G-120 | 4MByte | 1M×32bit | 72pin-SIMM | 8EA | 5.0V | 120ns |