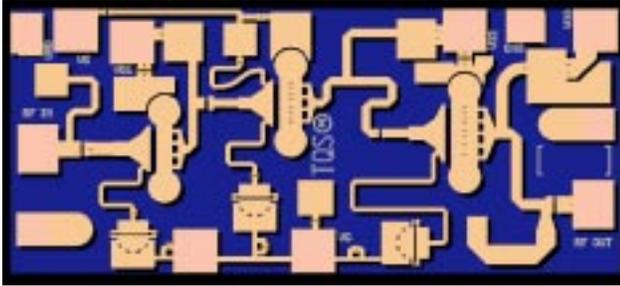


## 32 - 45 GHz Wide Band Driver Amplifier

## TGA4521



### Key Features

- Frequency Range: 32 - 45 GHz
- 25 dBm Nominal Psat @ 38 GHz
- 24 dBm P1dB @ 38 GHz
- 16 dB Nominal Gain @ 38 GHz
- 33 dBm OTOI @ 16dBm/Tone
- Bias: 6 V @ 175 mA Idq
- 0.15 um 3MI pHEMT Technology
- Chip Dimensions 1.60 x 0.75 x 0.10 mm  
(0.063 x 0.030 x 0.004 in)

### Product Description

The TriQuint TGA4521 is a compact Driver Amplifier MMIC for Ka-band and Q-band applications. The part is designed using TriQuint's 0.15um power pHEMT production process.

The TGA4521 nominally provides 25 dBm saturated output power, and 24 dBm output power at 1dB Gain compression @ 38 GHz. It also has typical gain of 16 dB.

The part is ideally suited for low cost emerging markets such as Digital Radio, Point-to-Point Radio and Point-to-Multi Point Communications.

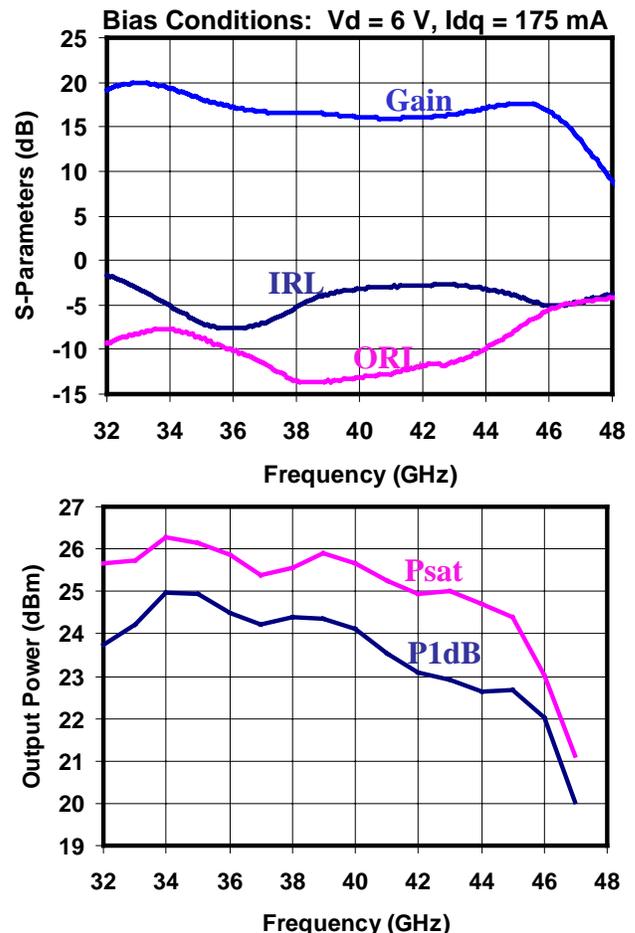
The TGA4521 is 100% DC and RF tested on-wafer to ensure performance compliance.

Lead-Free & RoHS compliant.

### Primary Applications

- Digital Radio
- Point-to-Point Radio
- Point-to-Multipoint Communications
- Military SAT-COM

### Measured Fixtured Data



Note: Devices is early in the characterization process prior to finalizing all electrical specifications. Specifications are subject to change without notice

**TABLE I**  
**MAXIMUM RATINGS 1/**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>VALUE</b>	<b>NOTES</b>
V <sub>d</sub>	Drain Voltage	6.5 V	<u>2/</u>
V <sub>g</sub>	Gate Voltage Range	-2 TO 0 V	
I <sub>d</sub>	Drain Current	350 mA	<u>2/ 3/</u>
I <sub>g</sub>	Gate Current	9 mA	<u>3/</u>
P <sub>IN</sub>	Input Continuous Wave Power	20 dBm	
P <sub>D</sub>	Power Dissipation	See note <u>4/</u>	<u>2/</u>
T <sub>CH</sub>	Operating Channel Temperature	150 °C	<u>5/ 6/</u>
T <sub>M</sub>	Mounting Temperature (30 Seconds)	320 °C	
T <sub>STG</sub>	Storage Temperature	-65 to 150 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.

3/ Total current for the entire MMIC.

4/ For a median life time of 1E+6 hrs, Power dissipation is limited to:

$$P_D(\text{max}) = (150 \text{ }^\circ\text{C} - T_{\text{BASE}} \text{ }^\circ\text{C}) / 70 \text{ (}^\circ\text{C/W)}$$

Where T<sub>BASE</sub> is the base plate temperature.

5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

6/ These ratings apply to each individual FET.

**TABLE II**  
**ELECTRICAL CHARACTERISTICS**

(Ta = 25 °C Nominal)

PARAMETER	TYPICAL	UNITS
Frequency Range	32 - 45	GHz
Drain Voltage, Vd	6.0	V
Drain Current, Id	175	mA
Gate Voltage, Vg	-0.7	V
Small Signal Gain, S21	16	dB
Input Return Loss, S11	6	dB
Output Return Loss, S22	10	dB
Output Power @ 1dB Gain Compression, P1dB	24	dBm
Saturated Power, Psat	25	dBm
OTOI @ 16dBm/tone	33	dBm

**TABLE III**  
**THERMAL INFORMATION**

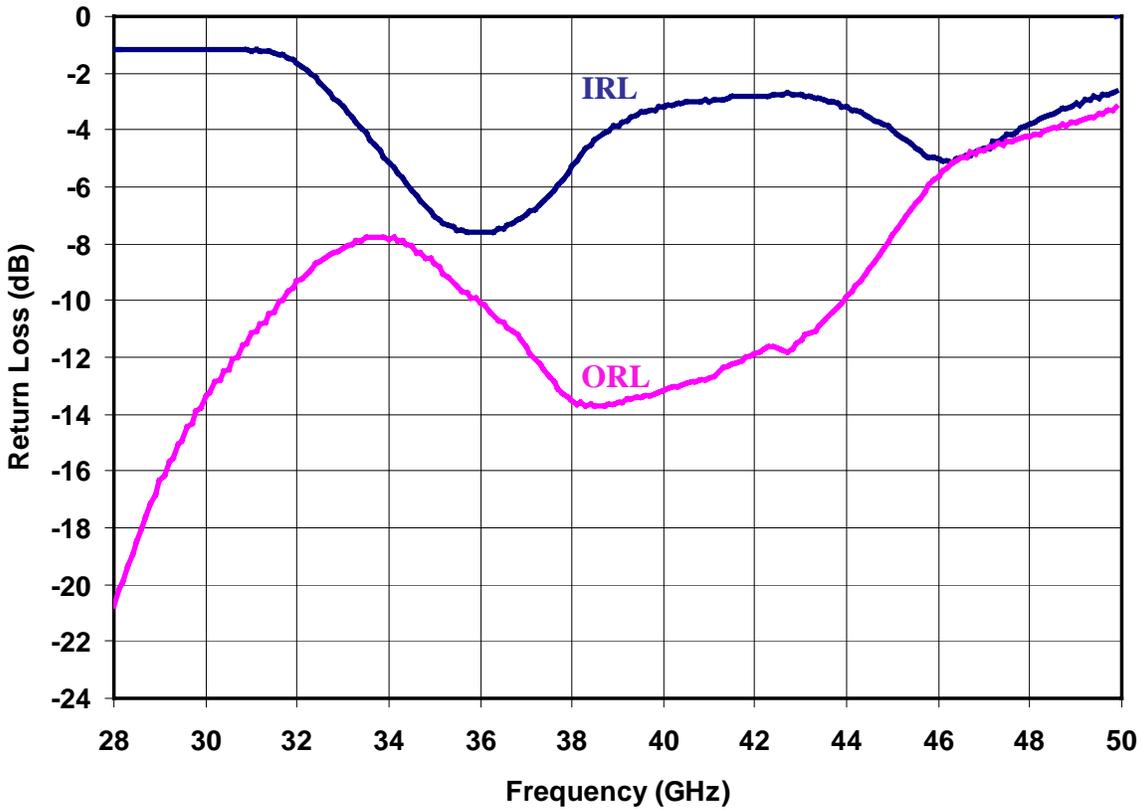
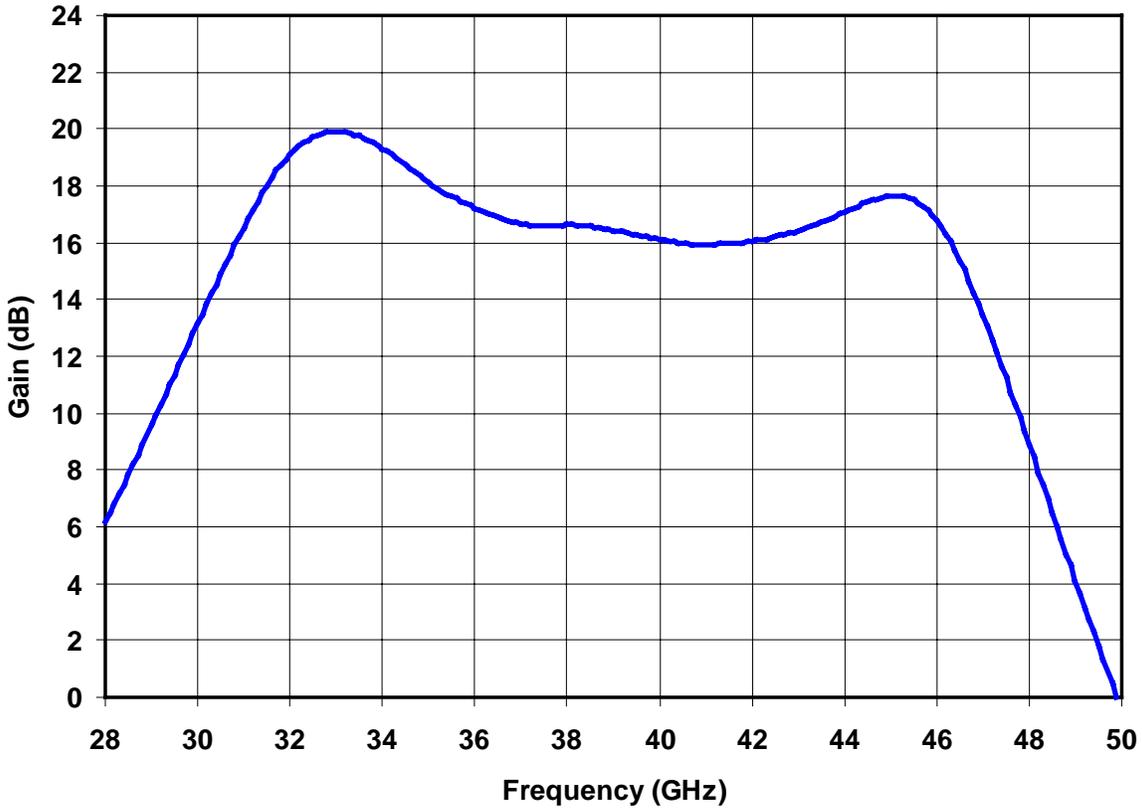
PARAMETER	TEST CONDITIONS	T <sub>CH</sub> (°C)	R <sub>θJC</sub> (°C/W)	T <sub>M</sub> (HRS)
R <sub>θJC</sub> Thermal Resistance (channel to Case)	Vd = 6 V Id = 175 mA P <sub>diss</sub> = 1.05 W	144	70	1.7E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70 °C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

**Measured Data**

**TGA4521**

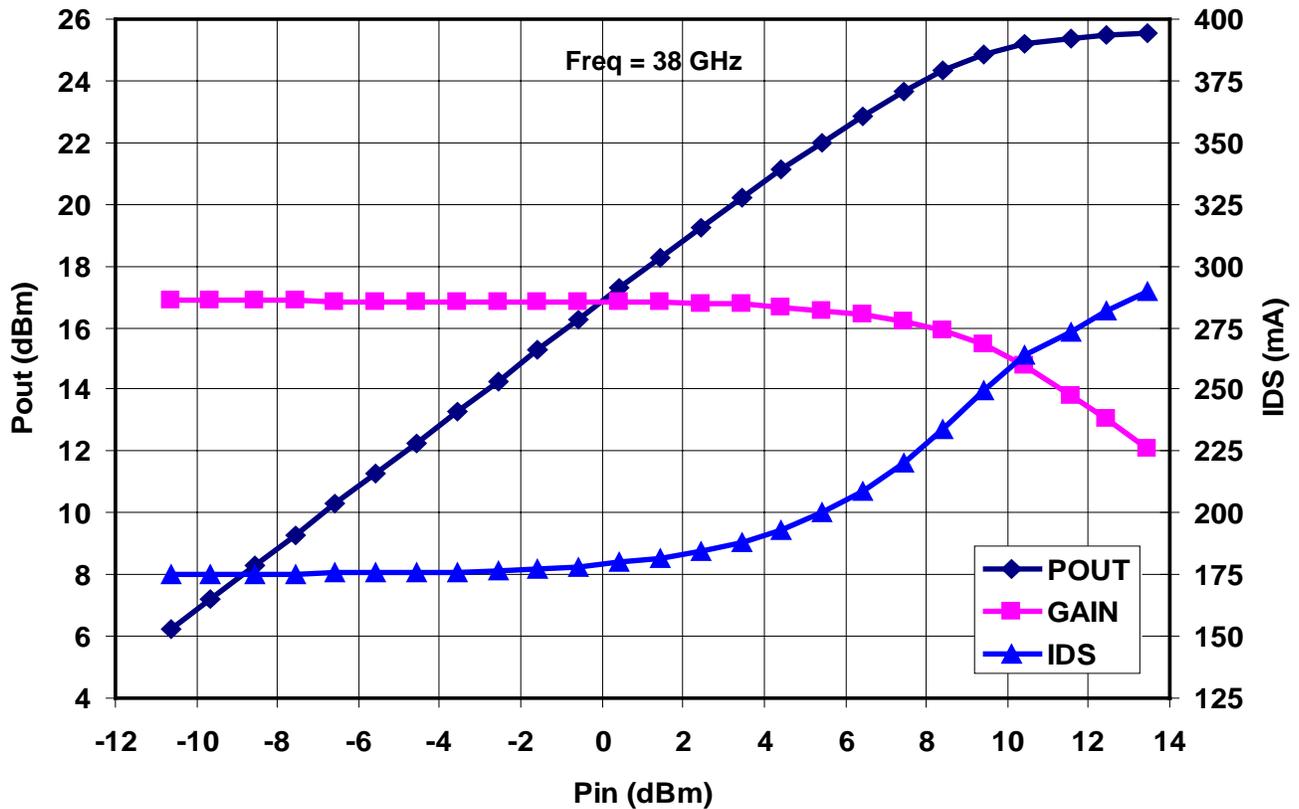
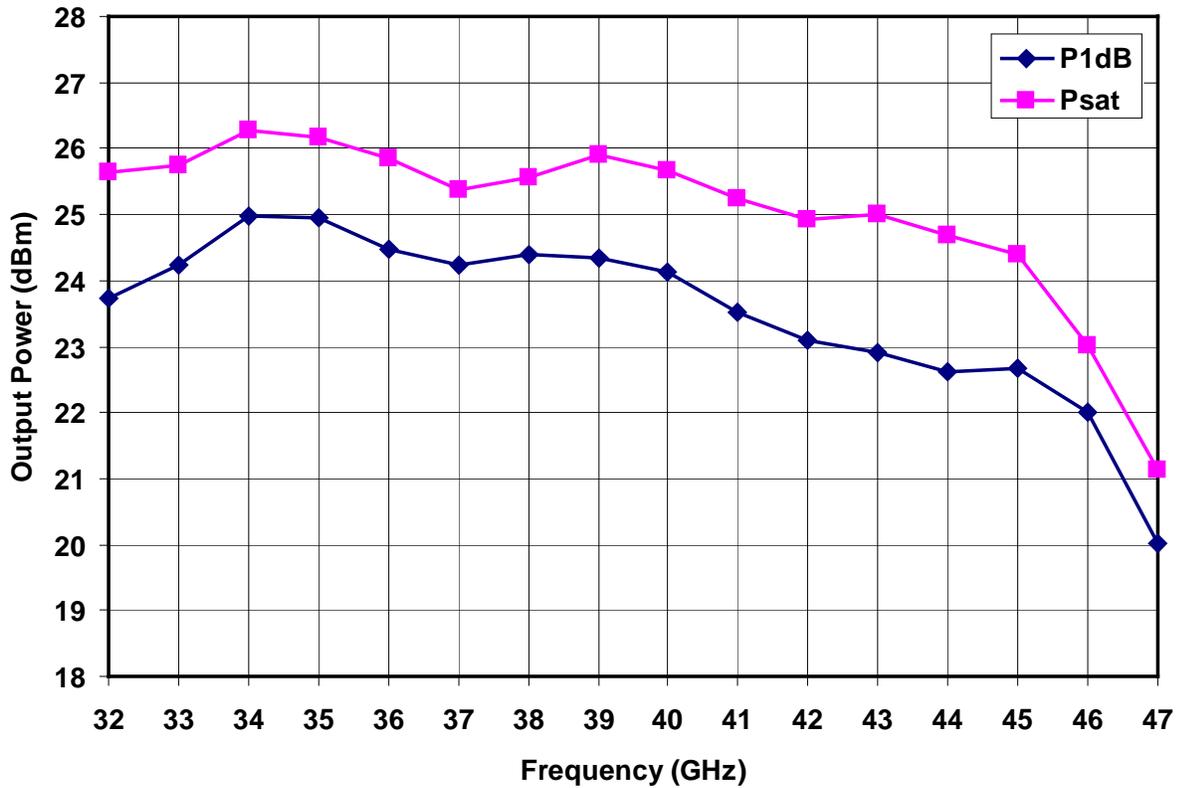
Bias Conditions:  $V_d = 6\text{ V}$ ,  $I_{dq} = 175\text{ mA}$



**Measured Data**

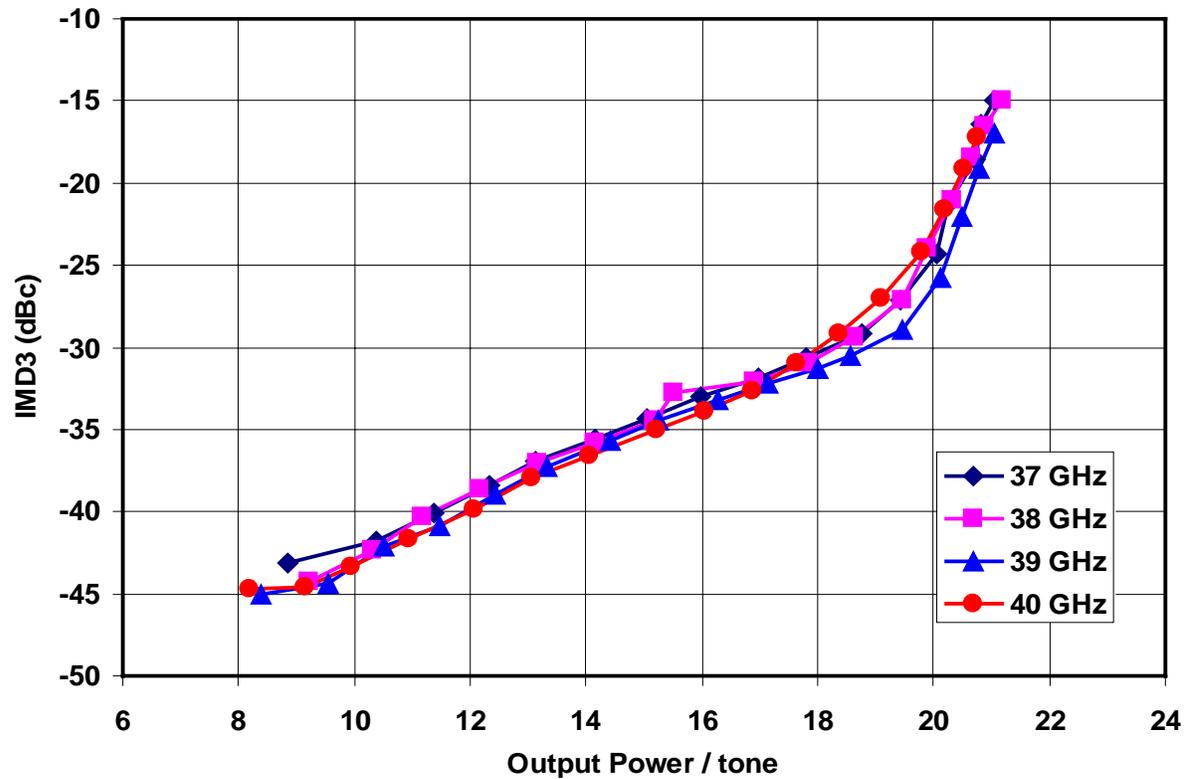
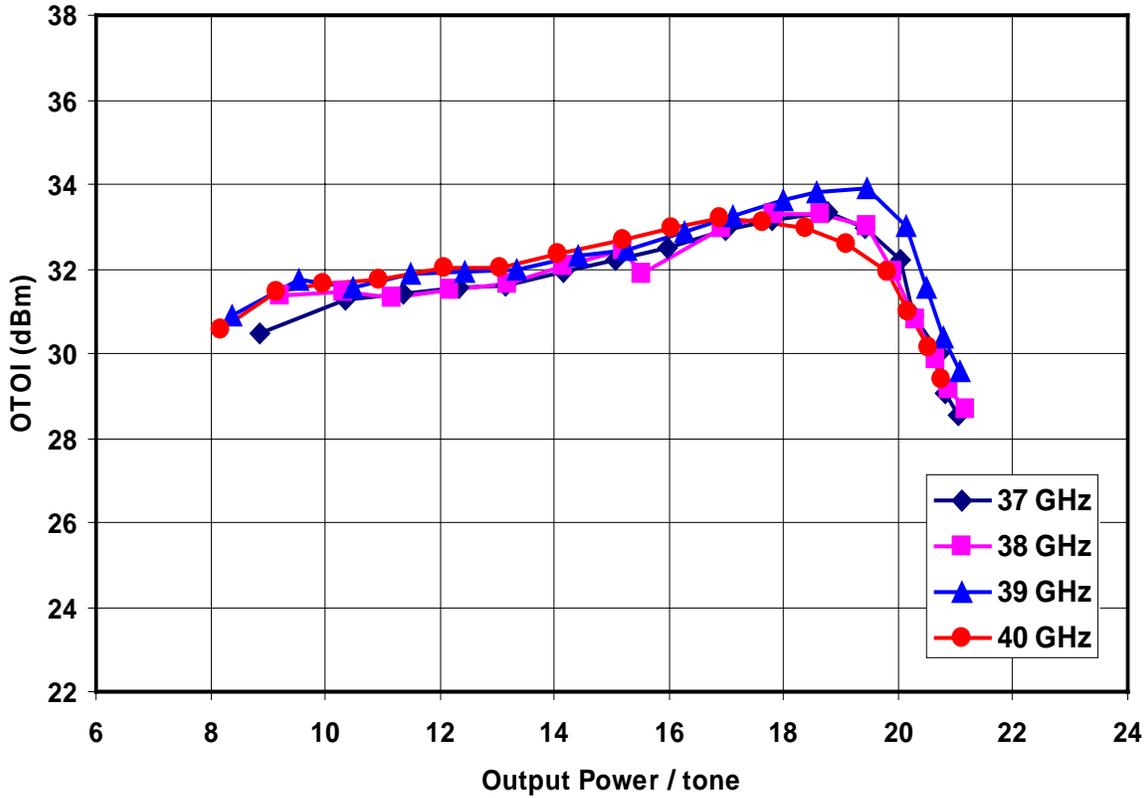
**TGA4521**

Bias Conditions:  $V_d = 6\text{ V}$ ,  $I_{dq} = 175\text{ mA}$

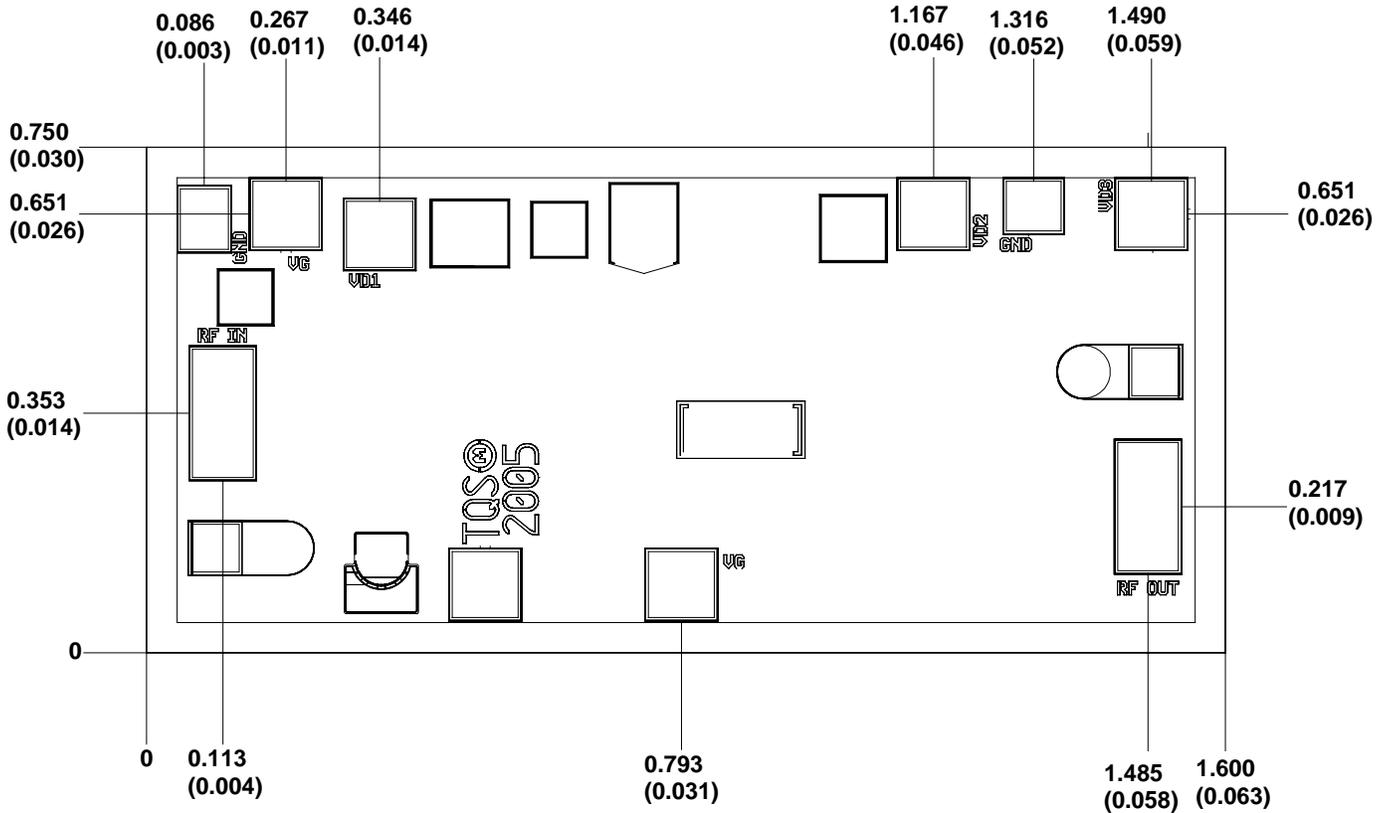


**Measured Data**

Bias Conditions:  $V_d = 6\text{ V}$ ,  $I_{dq} = 175\text{ mA}$ ,  $\Delta f = 10\text{ MHz}$



**Mechanical Drawing**



Units: millimeters (inches)

Thickness: 0.100 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

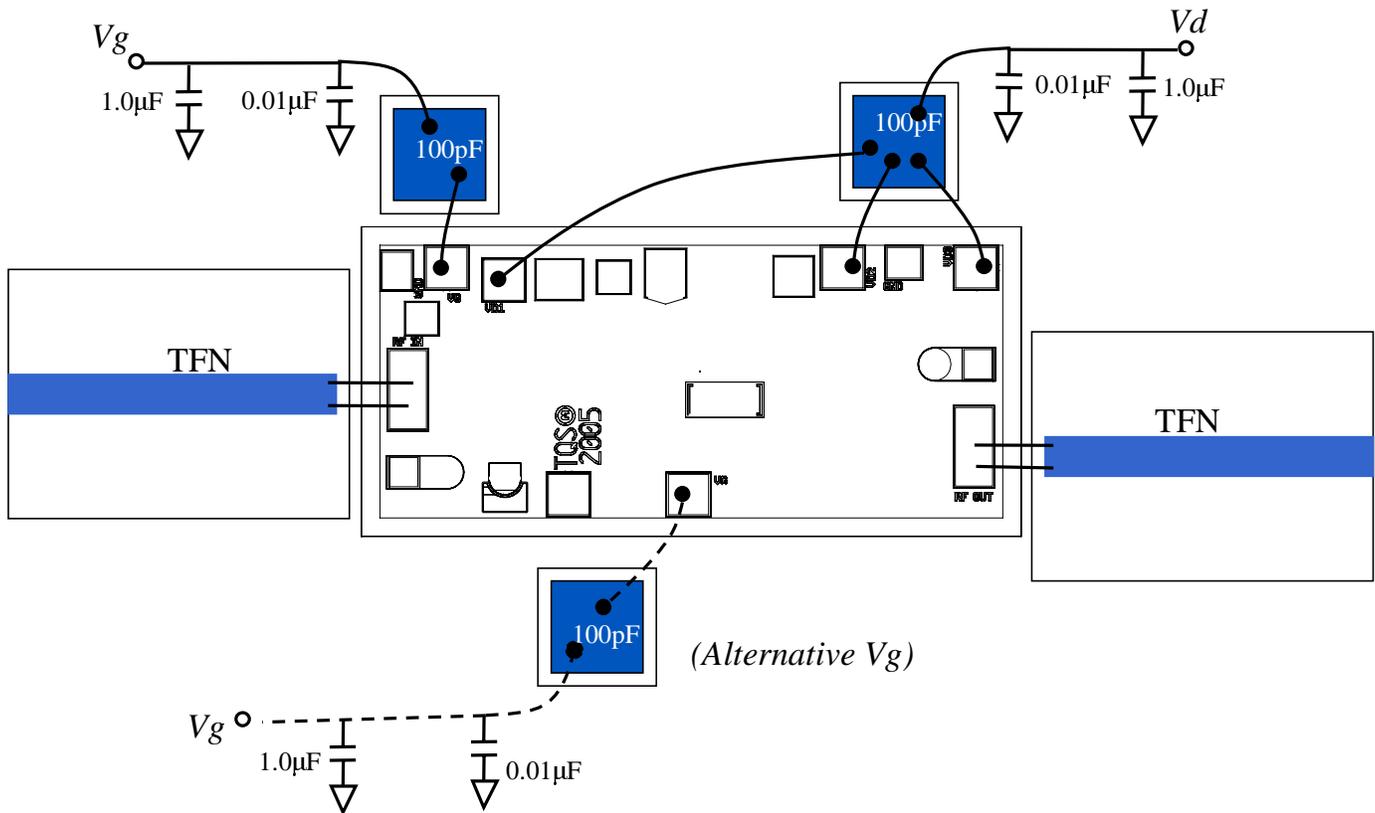
Chip size tolerance: +/- 0.051 (0.002)

GND is back side of MMIC

Bond pad #1	(RF In)	0.100 x 0.200	(0.004 x 0.008)
Bond pad #2	(N/C)	0.081 x 0.100	(0.003 x 0.004)
Bond pad #3, 9	(Vg)	0.108 x 0.108	(0.004 x 0.004)
Bond pad #4, 5, 7	(Vd)	0.108 x 0.108	(0.004 x 0.004)
Bond pad #6	(N/C)	0.091 x 0.084	(0.004 x 0.003)
Bond pad #8	(RF Out)	0.100 x 0.200	(0.004 x 0.008)

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

## Recommended Chip Assembly Diagram



**Bias Conditions:  $V_d = 6\text{ V}$   
 $V_g = \sim -0.7\text{ V}$  to get 175mA  $I_d$**

*GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.*

## **Assembly Process Notes**

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300<sup>0</sup>C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200<sup>0</sup>C.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***