

512K x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

APRIL 2003

FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation
 - 36 mW (typical) operating
 - 9 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
 - 1.65V – 2.2V V_{DD} (IS62WV5128ALL)
 - 2.5V – 3.6V V_{DD} (IS62WV5128BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available

DESCRIPTION

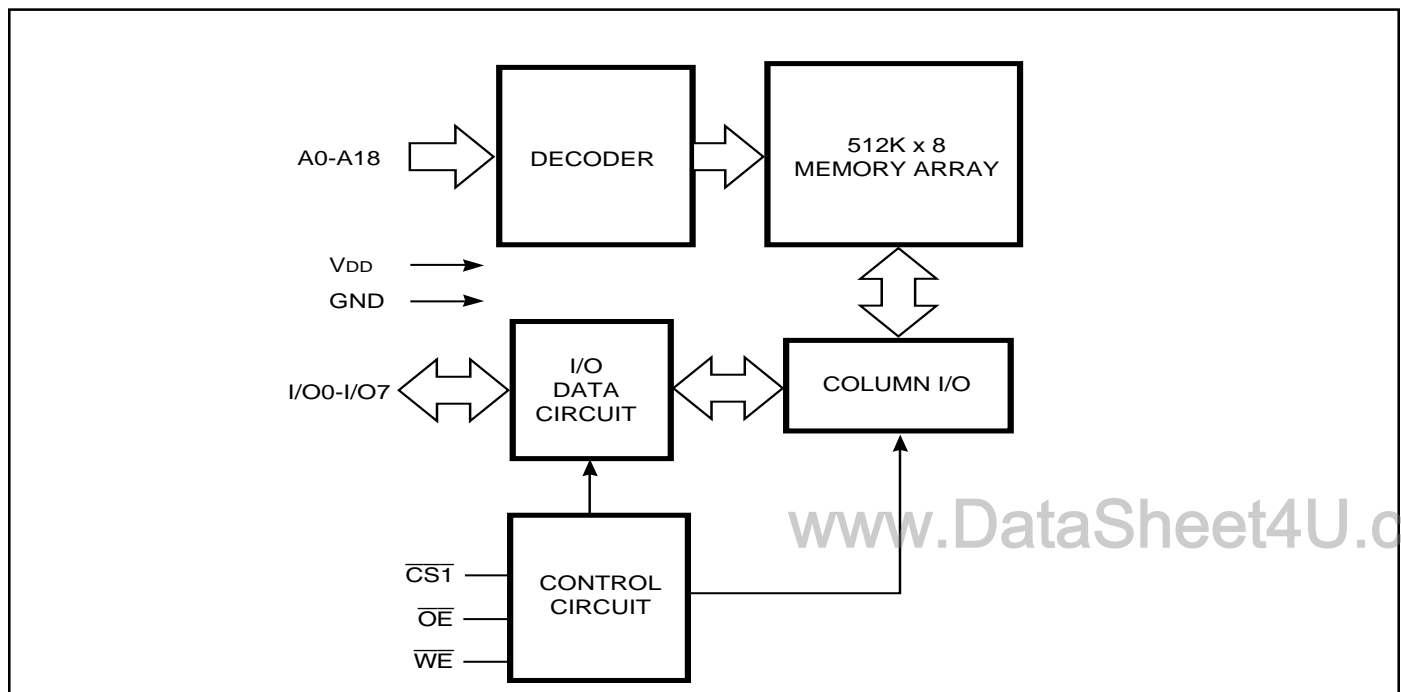
The *ISSI* IS62WV5128ALL / IS62WV5128BLL are high-speed, 4M bit static RAMs organized as 512K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS62WV5128ALL and IS62WV5128BLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), 32-pin sTSOP (TYPE I), and 32-pin TSOP (Type II).

FUNCTIONAL BLOCK DIAGRAM



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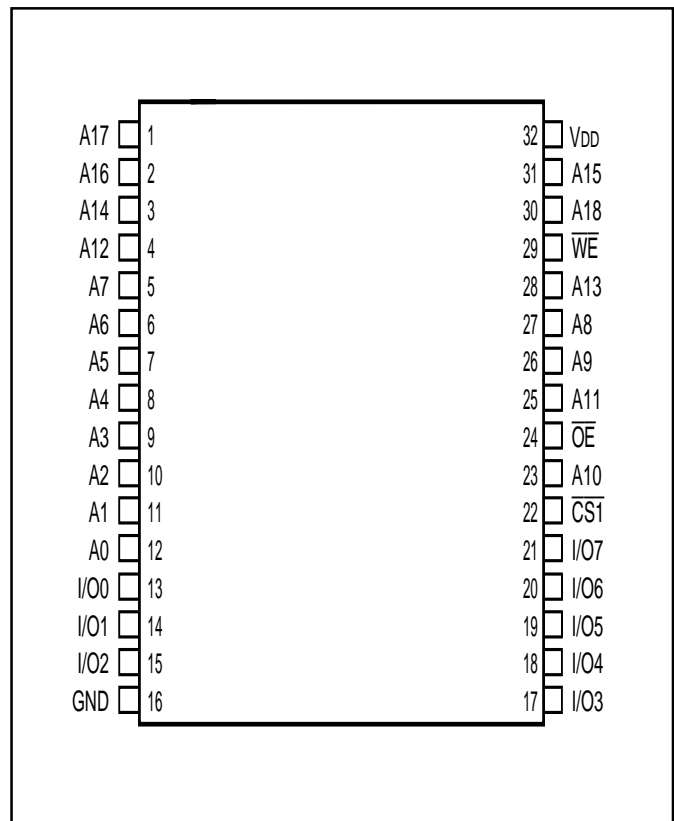
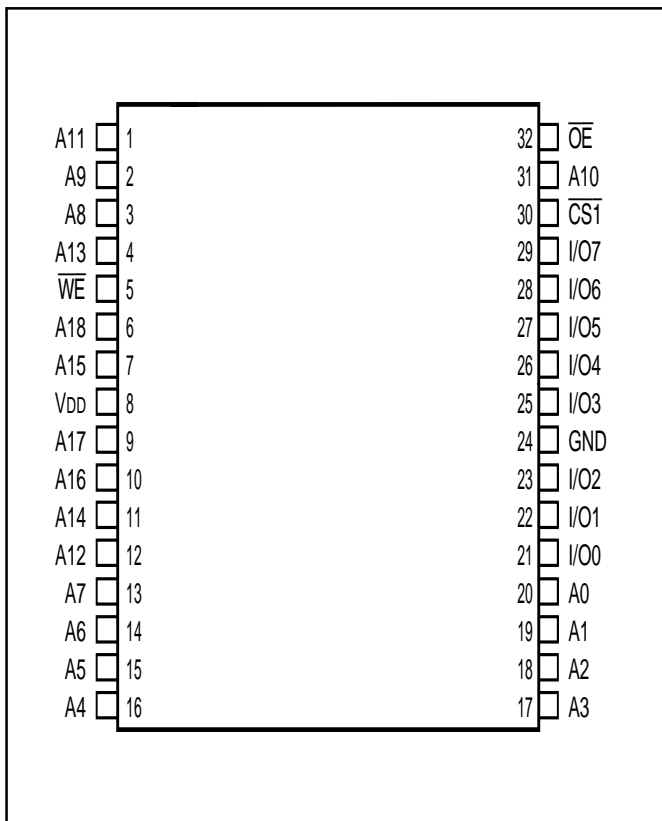
PIN DESCRIPTIONS

| | |
|------------------|---------------------|
| A0-A18 | Address Inputs |
| $\overline{CS1}$ | Chip Enable 1 Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O0-I/O7 | Input/Output |
| NC | No Connection |
| V _{DD} | Power |
| GND | Ground |

PIN CONFIGURATION

32-pin TSOP (TYPE I), (Package Code T)
32-pin sTSOP (TYPE I) (Package Code H)

32-pin TSOP (TYPE II)
(Package Code T2)



OPERATING RANGE (V_{DD})

| Range | Ambient Temperature | IS62WV5128ALL | IS62WV5128BLL |
|------------|---------------------|---------------|---------------|
| Commercial | 0°C to +70°C | 1.65V - 2.2V | 2.5V - 3.6V |
| Industrial | -40°C to +85°C | 1.65V - 2.2V | 2.5V - 3.6V |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.2 to V _{DD} +0.3 | V |
| V _{DD} | V _{DD} Related to GND | -0.2 to V _{DD} +0.3 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | V _{DD} | Min. | Max. | Unit |
|--------------------------------|---------------------|---|-----------------|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | I _{OH} = -0.1 mA | 1.65-2.2V | 1.4 | — | V |
| | | I _{OH} = -1 mA | 2.5-3.6V | 2.2 | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 0.1 mA | 1.65-2.2V | — | 0.2 | V |
| | | I _{OL} = 2.1 mA | 2.5-3.6V | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 1.65-2.2V | 1.4 | V _{DD} + 0.2 | V |
| | | | 2.5-3.6V | 2.2 | V _{DD} + 0.3 | V |
| V _{IL} ⁽¹⁾ | Input LOW Voltage | | 1.65-2.2V | -0.2 | 0.4 | V |
| | | | 2.5-3.6V | -0.2 | 0.6 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | | -1 | 1 | μA |

Notes:

1. V_{IL} (min.) = -1.0V for pulse width less than 10 ns.

CAPACITANCE⁽¹⁾

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 8 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 10 | pF |

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

| Parameter | IS62WV5128ALL (Unit) | IS62WV5128BLL (Unit) |
|---|-------------------------------|-------------------------------|
| Input Pulse Level | 0.4V to V _{DD} -0.2V | 0.4V to V _{DD} -0.3V |
| Input Rise and Fall Times | 5 ns | 5ns |
| Input and Output Timing and Reference Level | V _{REF} | V _{REF} |
| Output Load | See Figures 1 and 2 | See Figures 1 and 2 |

| | IS62WV5128ALL 1.65 - 2.2V | IS62WV5128BLL 2.5V - 3.6V |
|------------------|------------------------------|------------------------------|
| R1(Ω) | 3070 | 3070 |
| R2(Ω) | 3150 | 3150 |
| V _{REF} | 0.9V | 1.5V |
| V _{TM} | 1.8V | 2.8V |

AC TEST LOADS

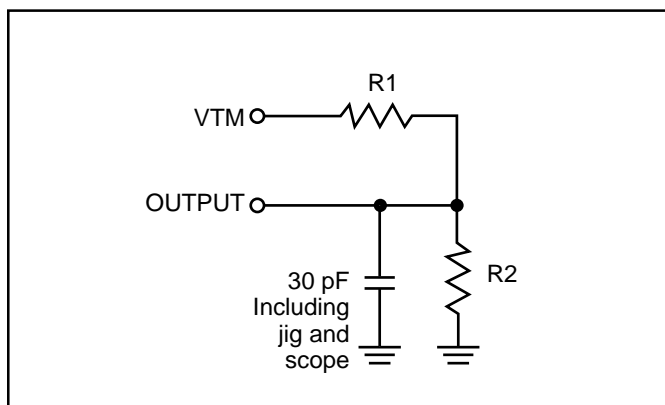


Figure 1

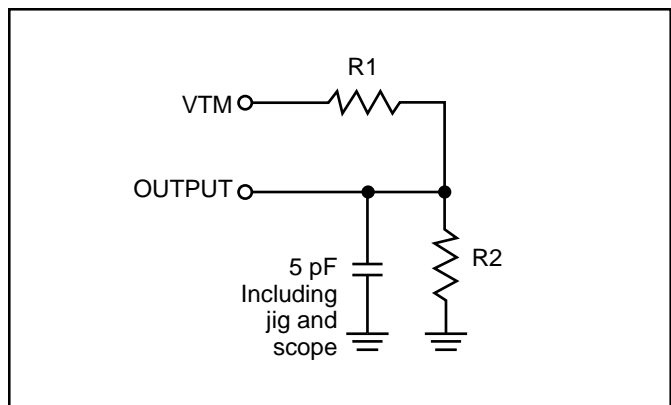


Figure 2

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)**62WV5128ALL** (1.65V - 2.2V)

| Symbol | Parameter | Test Conditions | | Max. 70 ns | Unit |
|------------------|--|---|--------------|---------------|------|
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. Ind. | 25 30 | mA |
| I _{CC1} | Operating Supply Current | V _{DD} = Max., $\overline{CS1} = 0.2V$ $\overline{WE} = V_{DD} - 0.2V$ f = 1 MHz | Com. Ind. | 10 10 | mA |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CS1} = V_{IH}$, f = 1 MHz | Com. Ind. | 0.35 0.35 | mA |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., $\overline{CS1} \geq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. Ind. | 15 15 | μA |

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)**62WV5128BLL** (2.5V - 3.6V)

| Symbol | Parameter | Test Conditions | | Max. 55 ns | Max. 70 ns | Unit |
|------------------|--|---|--------------|---------------|---------------|------|
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. Ind. | 40 45 | 35 40 | mA |
| I _{CC1} | Operating Supply Current | V _{DD} = Max., $\overline{CS1} = 0.2V$ $\overline{WE} = V_{DD} - 0.2V$ f = 1 MHz | Com. Ind. | 15 15 | 15 15 | mA |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CS1} = V_{IH}$, f = 1 MHz | Com. Ind. | 0.35 0.35 | 0.35 0.35 | mA |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., $\overline{CS1} \geq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. Ind. | 15 15 | 15 15 | μA |

Note:

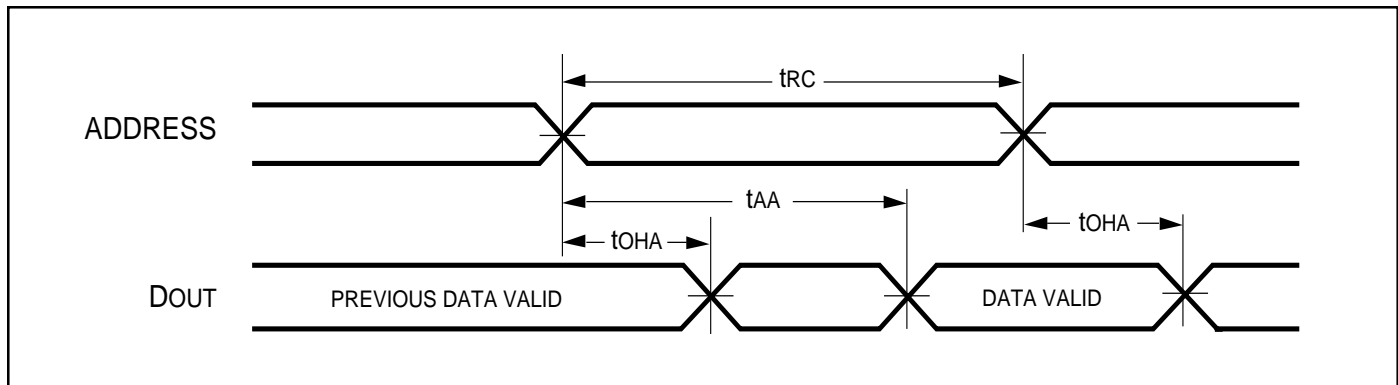
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | 55 ns | | 70 ns | | Unit |
|----------------------------------|---|-------|------|-------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 55 | — | 70 | — | ns |
| t _{AA} | Address Access Time | — | 55 | — | 70 | ns |
| t _{OHA} | Output Hold Time | 10 | — | 10 | — | ns |
| t _{ACS1} | $\overline{\text{CS}}_1$ Access Time | — | 55 | — | 70 | ns |
| t _{DOE} | $\overline{\text{OE}}$ Access Time | — | 25 | — | 35 | ns |
| t _{HZOE} ⁽²⁾ | $\overline{\text{OE}}$ to High-Z Output | — | 20 | — | 25 | ns |
| t _{LZOE} ⁽²⁾ | $\overline{\text{OE}}$ to Low-Z Output | 5 | — | 5 | — | ns |
| t _{HZCS1} | $\overline{\text{CS}}_1$ to High-Z Output | 0 | 20 | 0 | 25 | ns |
| t _{LZCS1} | $\overline{\text{CS}}_1$ to Low-Z Output | 10 | — | 10 | — | ns |

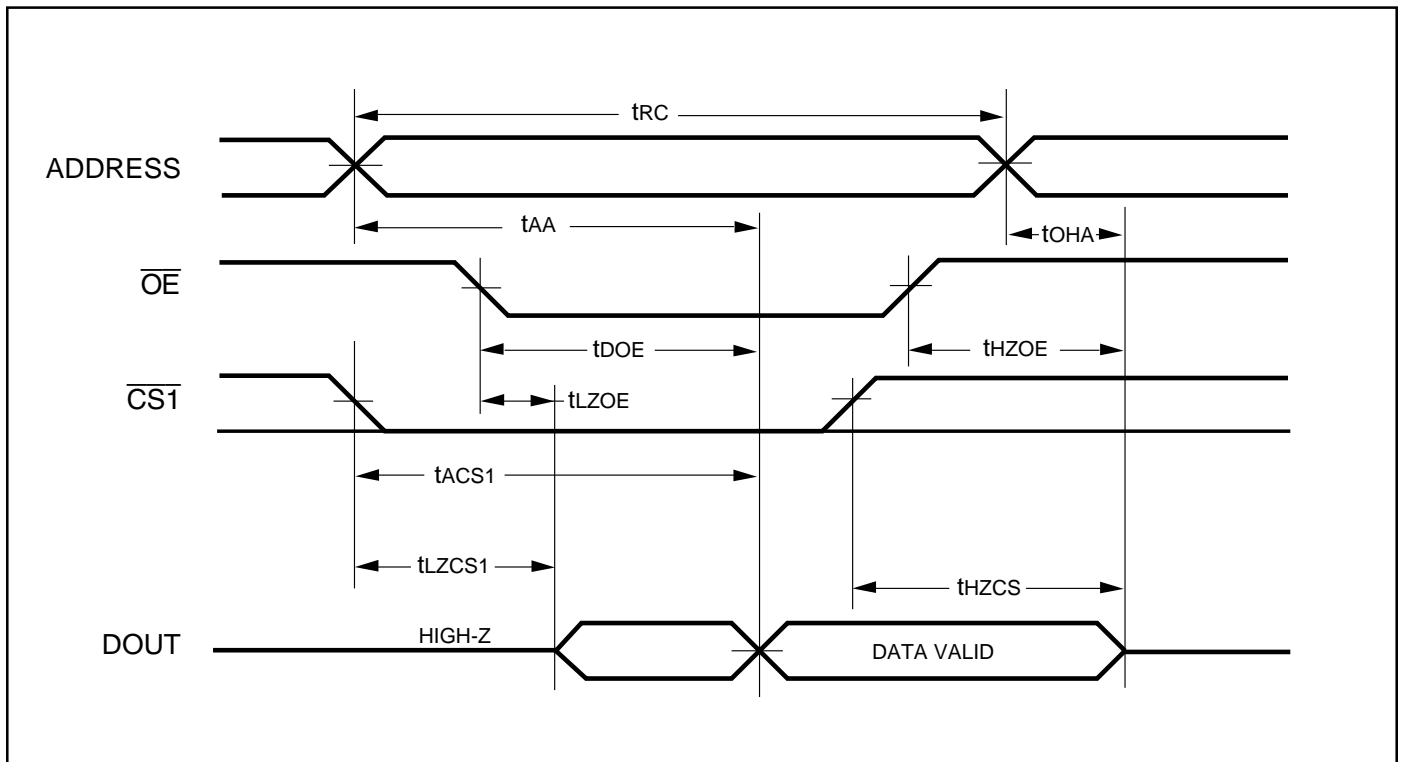
Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS**READ CYCLE NO. 1^(1,2)** (Address Controlled) ($\overline{\text{CS}}_1 = \overline{\text{OE}} = V_{\text{IL}}$, $\overline{\text{WE}} = V_{\text{IH}}$)

AC WAVEFORMS

READ CYCLE NO. 2^(1,3) ($\overline{CS1}$, \overline{OE} Controlled)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CS1} = V_{IL}$. $\overline{WE} = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

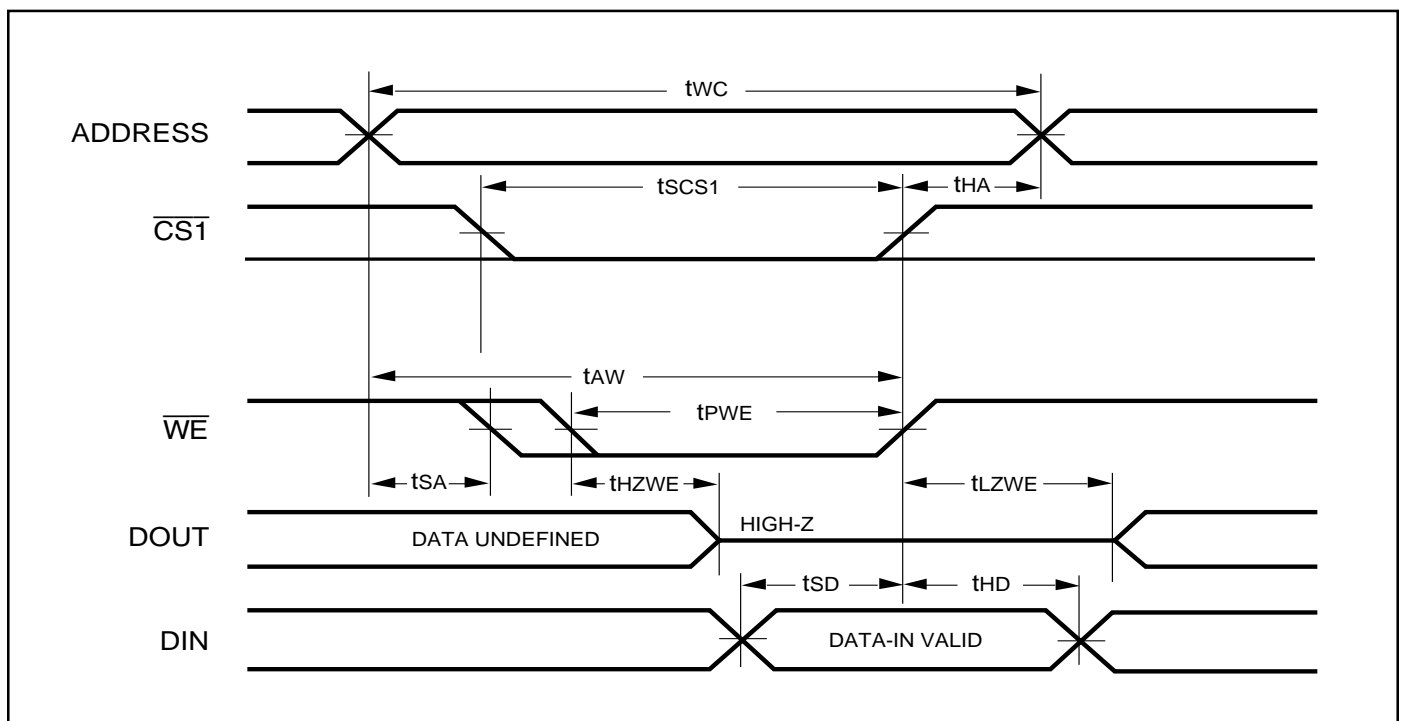
| Symbol | Parameter | 55 ns | | 70 ns | | Unit |
|---------------------------------|--------------------------------------|-------|------|-------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 55 | — | 70 | — | ns |
| t _{SCS1} | $\overline{CS1}$ to Write End | 45 | — | 60 | — | ns |
| t _{AW} | Address Setup Time to Write End | 45 | — | 60 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | ns |
| t _{PWE} | \overline{WE} Pulse Width | 40 | — | 50 | — | ns |
| t _{SD} | Data Setup to Write End | 25 | — | 30 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | ns |
| t _{HZWE⁽³⁾} | \overline{WE} LOW to High-Z Output | — | 20 | — | 20 | ns |
| t _{LZWE⁽³⁾} | \overline{WE} HIGH to Low-Z Output | 5 | — | 5 | — | ns |

Notes:

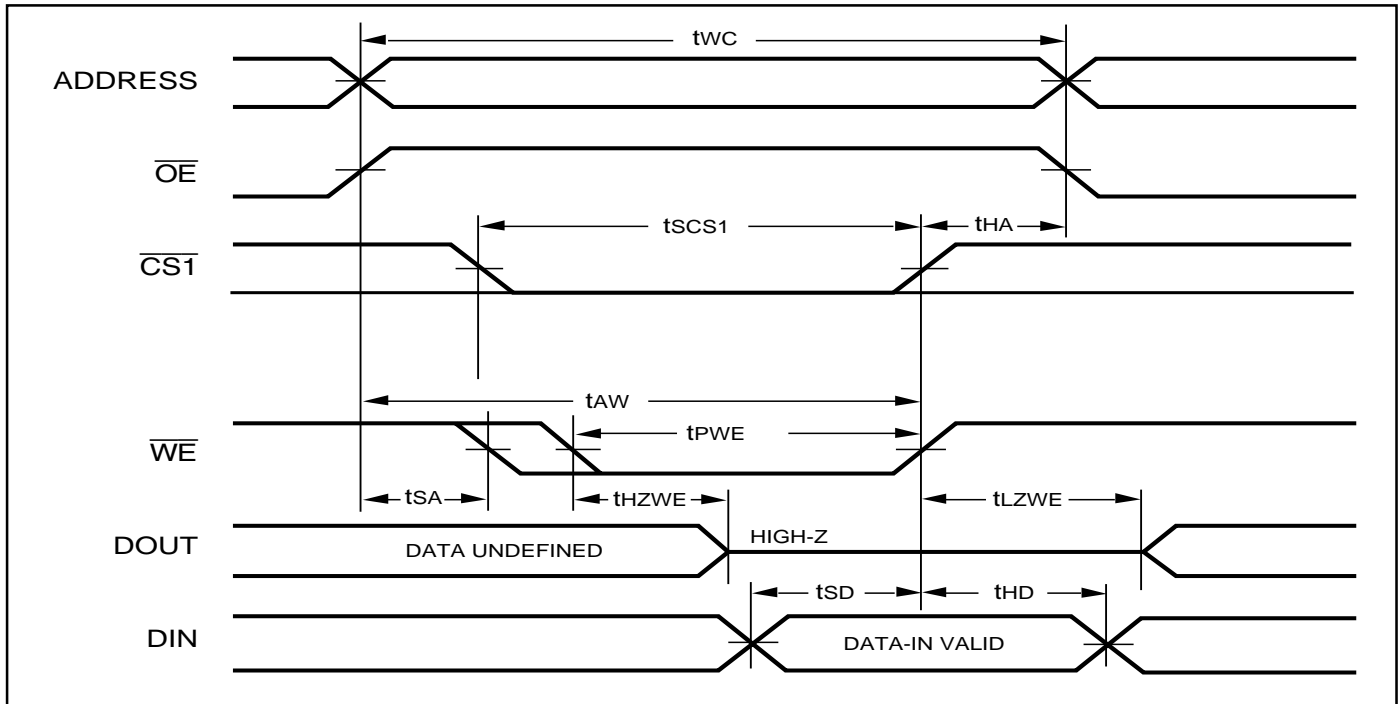
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V_{DD}-0.2V/V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

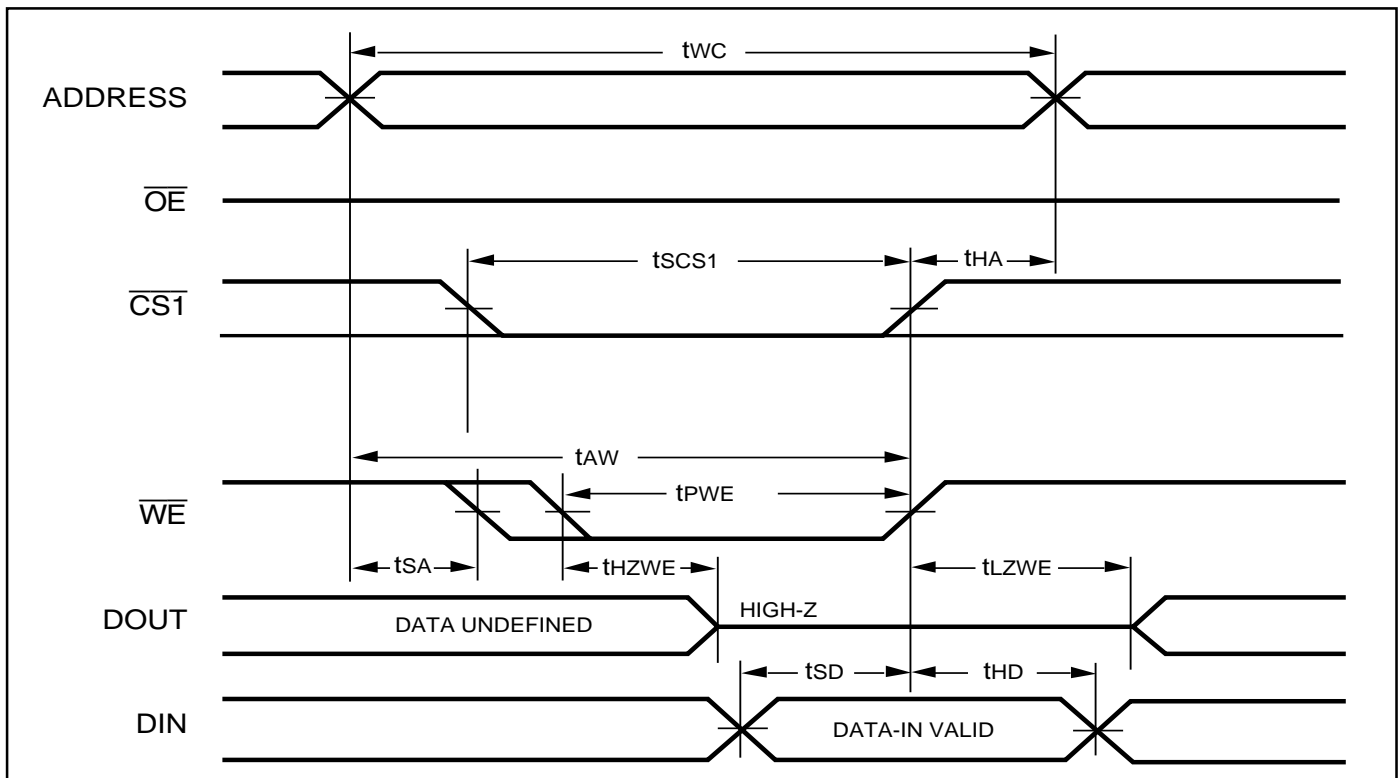
WRITE CYCLE NO. 1 ($\overline{CS1}$ Controlled, \overline{OE} = HIGH or LOW)



WRITE CYCLE NO. 2 (\overline{WE} Controlled: \overline{OE} is HIGH During Write Cycle)



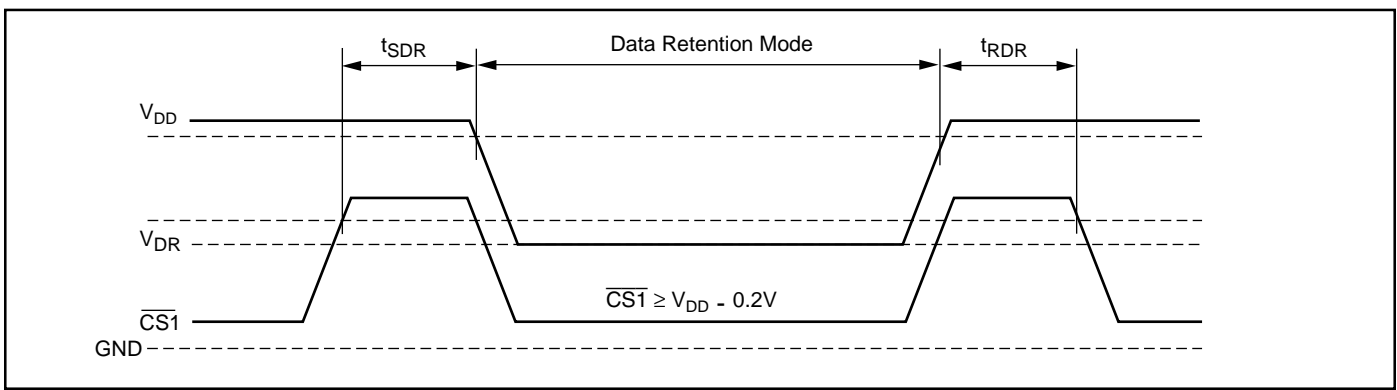
WRITE CYCLE NO. 3 (\overline{WE} Controlled: \overline{OE} is LOW During Write Cycle)



DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|------------------|------------------------------------|---|-----------------|------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | 1.2 | 3.6 | V |
| I _{DR} | Data Retention Current | V _{DD} = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$ | — | 15 | μA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | 0 | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | t _{RC} | — | ns |

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



IS62WV5128ALL, IS62WV5128BLL**ORDERING INFORMATION****IS62WV5128ALL (1.65V - 2.2V)****Commercial Range: 0°C to +70°C**

| Speed (ns) | Order Part No. | Package |
|------------|--------------------|---------------|
| 70 | IS62WV5128ALL-70T | TSOP, TYPE I |
| 70 | IS62WV5128ALL-70T2 | TSOP, TYPE II |
| 70 | IS62WV5128ALL-70H | sTSOP, TYPE I |

Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|---------------------|---------------|
| 70 | IS62WV5128ALL-70TI | TSOP, TYPE I |
| 70 | IS62WV5128ALL-70T2I | TSOP, TYPE II |
| 70 | IS62WV5128ALL-70HI | sTSOP, TYPE I |

ORDERING INFORMATION**IS62WV5128BLL (2.5V - 3.6V)****Commercial Range: 0°C to +70°C**

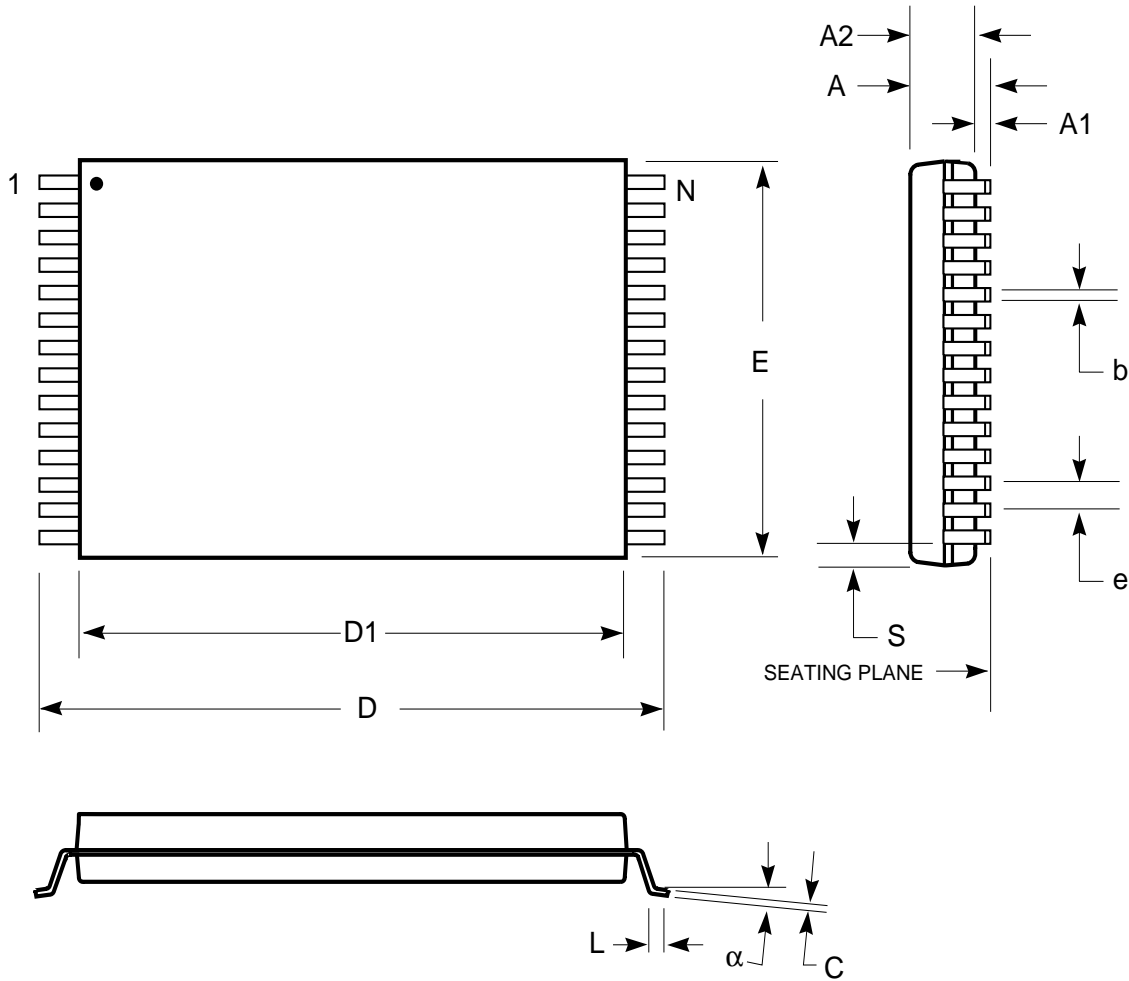
| Speed (ns) | Order Part No. | Package |
|------------|--------------------|---------------|
| 55 | IS62WV5128BLL-55T2 | TSOP, TYPE II |
| 55 | IS62WV5128BLL-55H | sTSOP, TYPE I |
| 70 | IS62WV5128BLL-70T | TSOP, TYPE I |
| 70 | IS62WV5128BLL-70T2 | TSOP, TYPE II |
| 70 | IS62WV5128BLL-70H | sTSOP, TYPE I |

Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|---------------------|---------------|
| 55 | IS62WV5128BLL-55TI | TSOP, TYPE I |
| 55 | IS62WV5128BLL-55T2I | TSOP, TYPE II |
| 55 | IS62WV5128BLL-55HI | sTSOP, TYPE I |
| 70 | IS62WV5128BLL-70TI | TSOP, TYPE I |
| 70 | IS62WV5128BLL-70HI | sTSOP, TYPE I |

PACKAGING INFORMATION

Plastic STSOP - 32 pins
 Package Code: H (Type I)



| Plastic STSOP (H - Type I) | | | | |
|----------------------------|-------------|-------|------------|--------|
| | Millimeters | | Inches | |
| Symbol | Min | Max | Min | Max |
| Ref. Std. | | | | |
| N | 32 | | | |
| A | — | 1.25 | — | 0.049 |
| A1 | 0.05 | — | 0.002 | — |
| A2 | 0.95 | 1.05 | 0.037 | 0.041 |
| b | 0.17 | 0.23 | 0.007 | 0.009 |
| C | 0.14 | 0.16 | 0.0055 | 0.0063 |
| D | 13.20 | 13.60 | 0.520 | 0.535 |
| D1 | 11.70 | 11.90 | 0.461 | 0.469 |
| E | 7.90 | 8.10 | 0.311 | 0.319 |
| e | 0.50 BSC | | 0.020 BSC | |
| L | 0.30 | 0.70 | 0.012 | 0.028 |
| S | 0.28 Typ. | | 0.011 Typ. | |
| alpha | 0° | 5° | 0° | 5° |

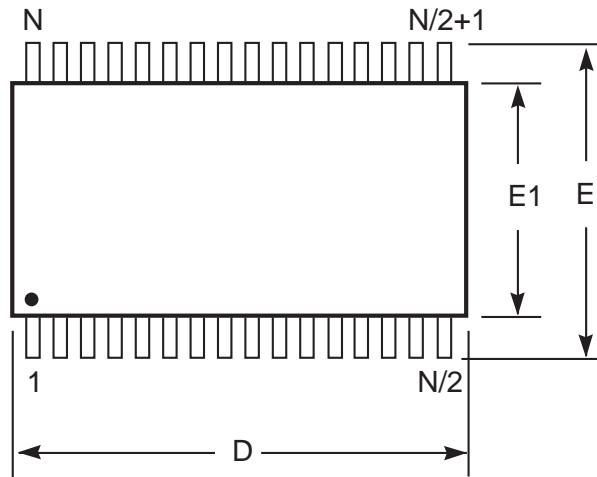
Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

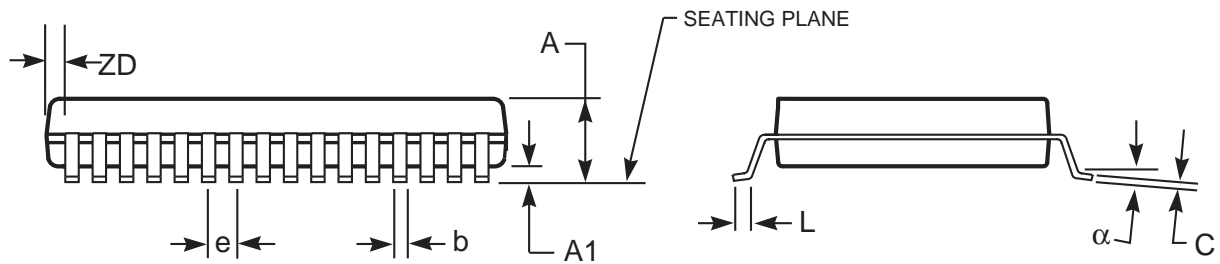


Plastic TSOP Package Code: T (Type II)



Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

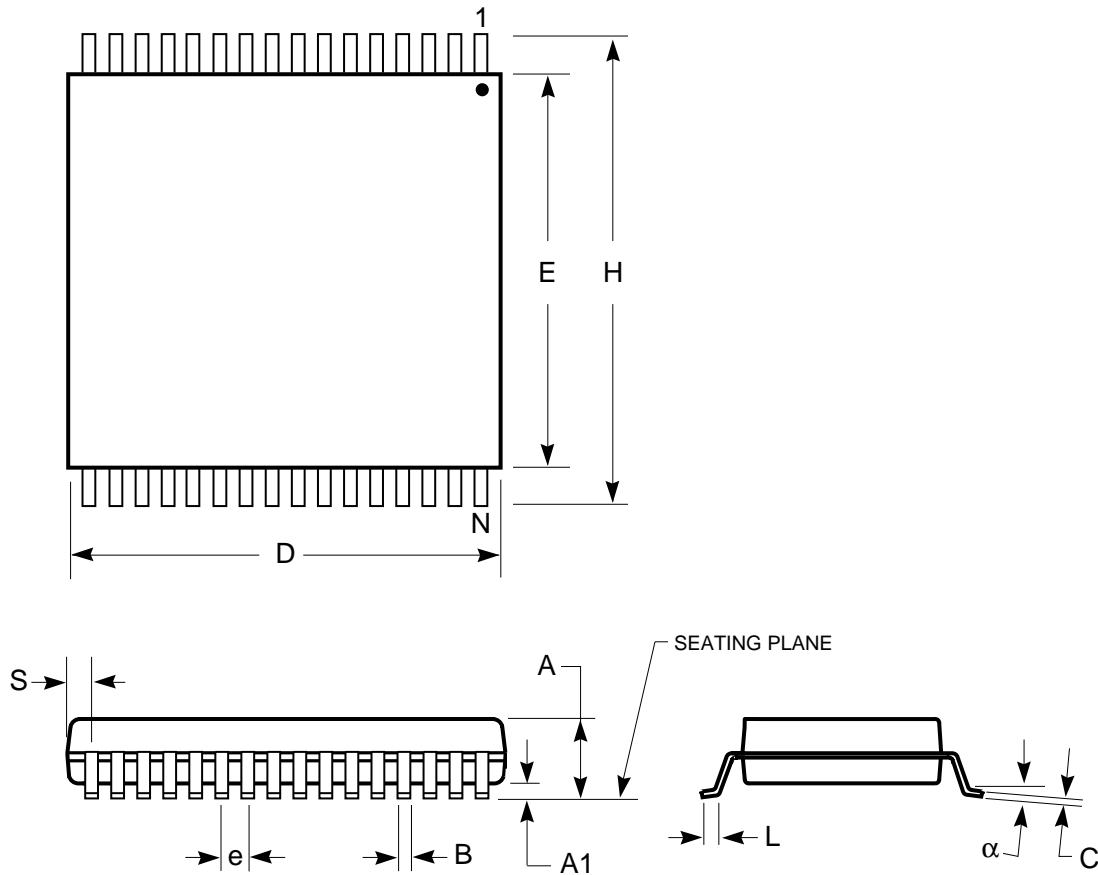
| Symbol | Millimeters | | Inches | | Millimeters | | Inches | | Millimeters | | Inches | |
|---------------|-------------|-------|------------|-------|-------------|-------|------------|-------|-------------|-------|------------|-------|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| Ref. Std. | | | | | | | | | | | | |
| No. Leads (N) | 32 | | | | 44 | | | | 50 | | | |
| A | — | 1.20 | — | 0.047 | — | 1.20 | — | 0.047 | — | 1.20 | — | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 |
| b | 0.30 | 0.52 | 0.012 | 0.020 | 0.30 | 0.45 | 0.012 | 0.018 | 0.30 | 0.45 | 0.012 | 0.018 |
| C | 0.12 | 0.21 | 0.005 | 0.008 | 0.12 | 0.21 | 0.005 | 0.008 | 0.12 | 0.21 | 0.005 | 0.008 |
| D | 20.82 | 21.08 | 0.820 | 0.830 | 18.31 | 18.52 | 0.721 | 0.729 | 20.82 | 21.08 | 0.820 | 0.830 |
| E1 | 10.03 | 10.29 | 0.391 | 0.400 | 10.03 | 10.29 | 0.395 | 0.405 | 10.03 | 10.29 | 0.395 | 0.405 |
| E | 11.56 | 11.96 | 0.451 | 0.466 | 11.56 | 11.96 | 0.455 | 0.471 | 11.56 | 11.96 | 0.455 | 0.471 |
| e | 1.27 BSC | | 0.050 BSC | | 0.80 BSC | | 0.032 BSC | | 0.80 BSC | | 0.031 BSC | |
| L | 0.40 | 0.60 | 0.016 | 0.024 | 0.41 | 0.60 | 0.016 | 0.024 | 0.40 | 0.60 | 0.016 | 0.024 |
| ZD | 0.95 REF. | | 0.037 REF. | | 0.81 REF. | | 0.032 REF. | | 0.88 REF. | | 0.035 REF. | |
| α | 0° | 5° | 0° | 5° | 0° | 5° | 0° | 5° | 0° | 5° | 0° | 5° |

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Rev. E
02/20/03

Plastic TSOP - 32 pins
 Package Code: T (Type I)



| Plastic TSOP (T—Type I) | | | | |
|-------------------------|-------------|-------|-----------|-------|
| Symbol | Millimeters | | Inches | |
| | Min | Max | Min | Max |
| Ref. Std. | | | | |
| No. Leads | 32 | | | |
| A | — | 1.20 | — | 0.047 |
| A1 | 0.05 | 0.25 | 0.002 | 0.010 |
| B | 0.17 | 0.23 | 0.007 | 0.009 |
| C | 0.12 | 0.17 | 0.006 | 0.014 |
| D | 7.90 | 8.10 | 0.308 | 0.316 |
| E | 18.30 | 18.50 | 0.714 | 0.722 |
| H | 19.80 | 20.20 | 0.772 | 0.788 |
| e | 0.50 BSC | | 0.020 BSC | |
| L | 0.40 | 0.60 | 0.016 | 0.024 |
| alpha | 0° | 8° | 0° | 8° |

Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.