Data Book

AU6388

USB2.0 Flash Disk Controller

Technical Reference Manual

Product Specification

Official Release

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May 2006

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Objective specification	This data book contains target specifications for product development.
Preliminary specification	This data book contains preliminary data; supplementary data may be published later.
Product specification	This data book contains final product specifications.

Revision History

Date	Revision	Description
Aug 2005	V1.00W	Official Release
May 2006	V1.01W	Modified “Figure 6.1 Mechanical Information Diagram”

Contact Information:

Web site: http://www.alcormicro.com/

Taiwan
Alcor Micro Corp.
4F, No 200 Kang Chien Rd., Nei Hu,
Taipei, Taiwan, R.O.C.
Phone: 886-2-8751-1984
Fax: 886-2-2659-7723

China ShenZhen Office
Rm.2407-08 ,Industrial Bank Building
No.4013, Shennan Road ,ShenZhen,China.
518026
Phone: (0755) 8366-9039
Fax: (0755) 8366-9101

Santa Clara Office
2901 Tasman Drive, Suite 206
Santa Clara, CA 95054
USA
Phone: (408) 845-9300
Fax: (408) 845-9086

Los Angeles Office
9400 Seventh St., Bldg. A2
Rancho Cucamonga, CA 91730
USA
Phone: (909) 483-9900
Fax: (909) 944-0464

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1.0 Introduction

1.1 Description

AU6388 is a single chip USB 2.0 flash disk controller that supports dual channel mode for high performance operation. The AU6388 it can be used as a removable storage disk in enormous data exchange application between USB enabled PC and NAND type flash memory, it can also be configured as bootable disk for system recovery.

Alcor Micro provides iRun smart application as a handy tool to manage partition and password for USB storage device.

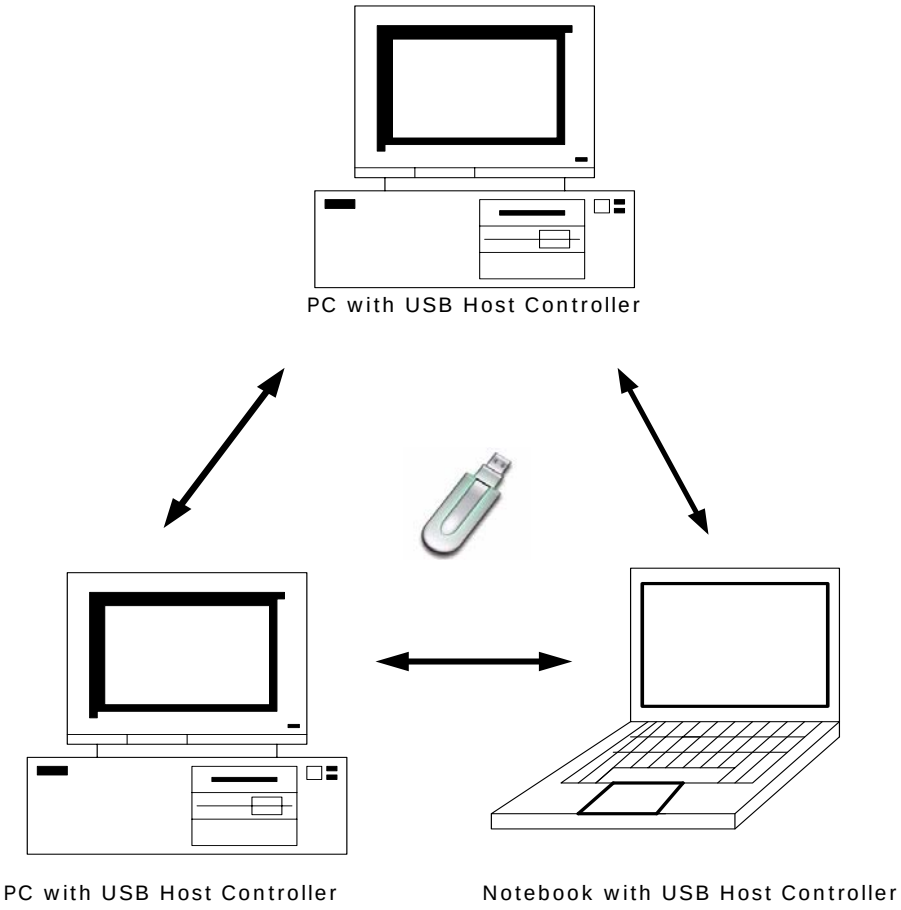
1.2 Features

- Support dual channel mode for high-speed transfer
- Support USB v2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Work with default driver from Windows ME, Windows 2000, Windows XP, Mac 9.2, Mac OS X and vendor driver from Alcor for Windows 98SE
- Multiple FIFO implementation for concurrent bus operation
- Runs at 12MHz, built-in 480 MHz PLL
- LED for bus activity monitoring
- Built-in 3.3V to 2.5V regulator
- Integrate flash memory power control switch
- Support bad block management
- Support dynamic serial number via mass production software
- Support hardware and software write protection
- Support AutoRun feature
  - AutoRun feature on Windows ME, Windows 2000, Windows XP, Win98.
- Support smart application – iRun handy tool
  - Support password protection for access security
  - Support partition and lock disk function
  - Support software write protection function
- 48-pin package available

2.0 Application Block Diagram

Following is the application diagram of a typical flash disk product with AU6388. By connecting the flash disk to a desktop or notebook PC through USB bus, AU6388 is implemented as a bus-powered, high speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

2.1 Block Diagram



3.0 Pin Assignment

The AU6388 is packed in 48pin-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail

Figure 3.1 Pin Assignment Diagram

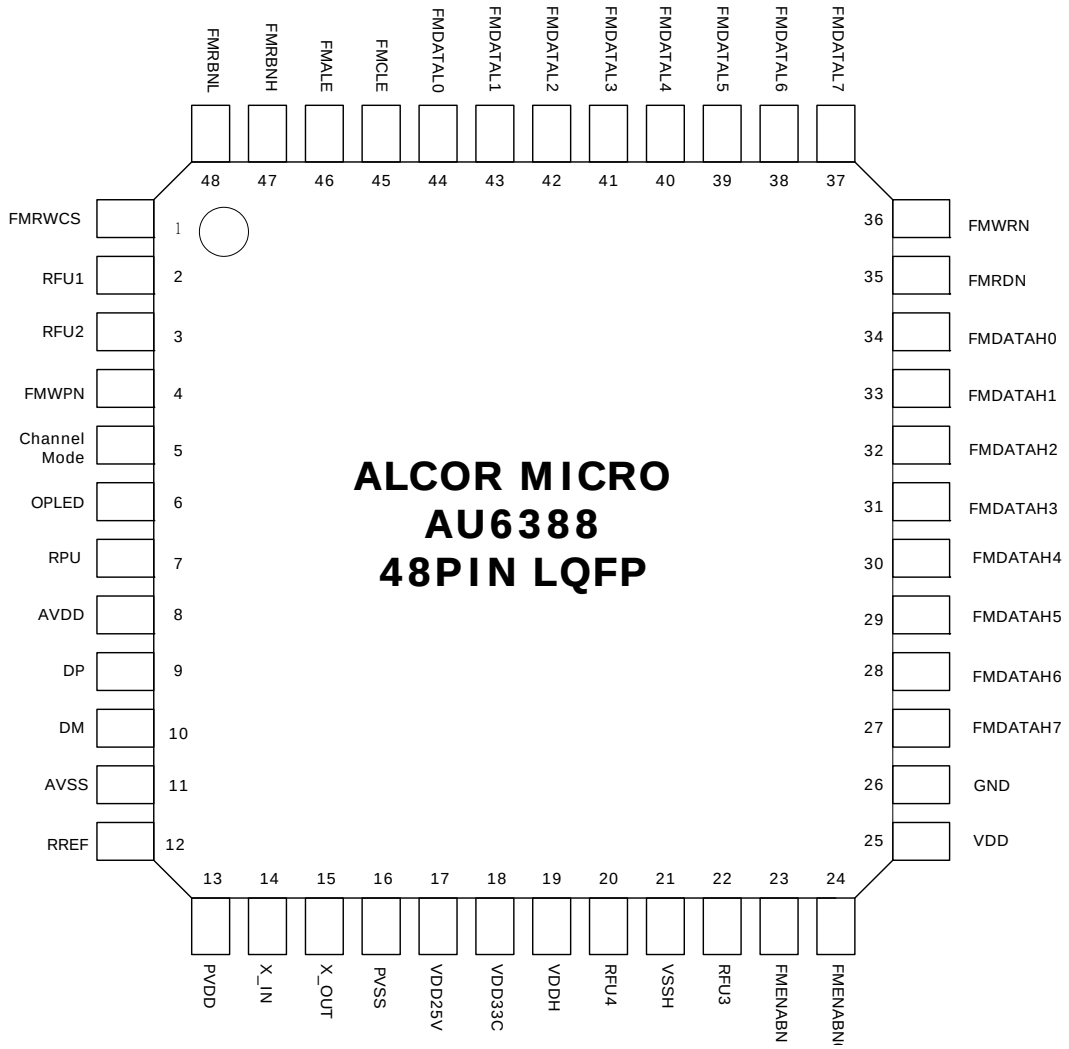


Table 3.1 Pin Descriptions

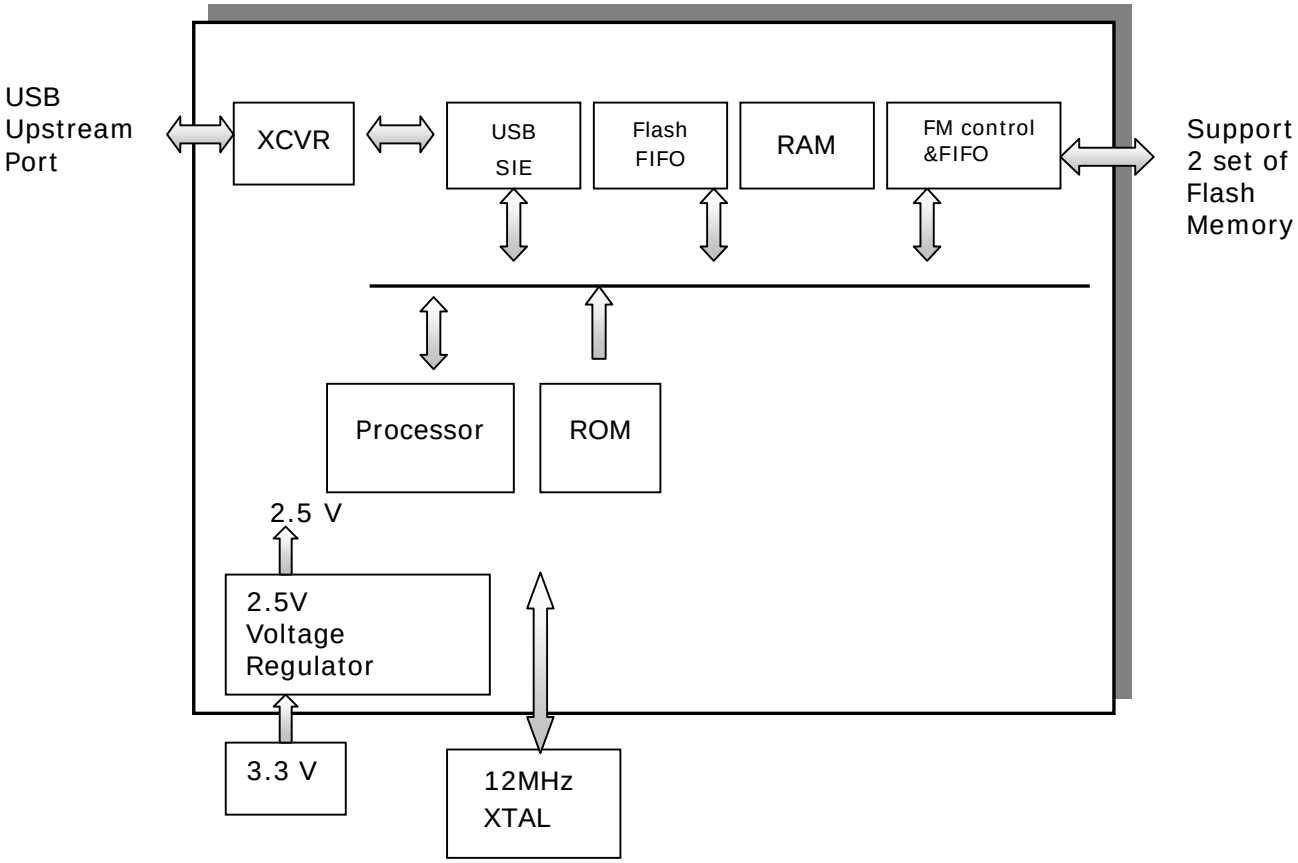
Pin #	Pin Name	I/O	Description
1	FMRWCS	I	Read Write cycle selection (0=50 ns; 1=66ns)
2	RFU1	NC	Reserved
3	RFU2	NC	Reserved
4	FMWPN	I	Hardware Write Protect (0: Normal; 1: Hardware Write Protect)
5	ChannelMode	I	Channel Selection (0: Single Channel; 1: Dual Channel)
6	OPLED	O	LED for busy activity monitoring
7	RPU	I	Connected with an 1.5k pull up resistor to 3.3V VDD
8	AVDD	I	3.3V Power Supply Input
9	DP	I/O	DP
10	DM	I/O	DM
11	AVSS	GND	Analog Ground
12	RREF	I	Connected to 1k resistor to analog ground
13	PVDD	I	3.3V Power Supply Input for Pad
14	X_IN	I	12 MHz crystal input.
15	X_OUT	O	12 MHz crystal output.
16	PVSS	GND	Pad Ground
17	VDD25V	O	2.5V voltage out for core
18	VDD33C	O	3.3V voltage out for flash
19	VDDH	I	3.3V Power Supply for IO
20	RFU4	NC	Reserved
21	VSSH	GND	IO Ground
22	RFU3	NC	Reserved
23	FMENABN1	O	Flash Memory #1 Enable
24	FMENABN0	O	Flash Memory #0 Enable
25	VDD	I	Core Power 2.5V Input
26	GND	GND	Core Ground
27	FMDATAH7	I/O	Flash Memory (H) Data [7]
28	FMDATAH6	I/O	Flash Memory (H) Data [6]
29	FMDATAH5	I/O	Flash Memory (H) Data [5]
30	FMDATAH4	I/O	Flash Memory (H) Data [4]
31	FMDATAH3	I/O	Flash Memory (H) Data [3]
32	FMDATAH2	I/O	Flash Memory (H) Data [2]
33	FMDATAH1	I/O	Flash Memory (H) Data [1]
34	FMDATAH0	I/O	Flash Memory (H) Data [0]
35	FMRDN	O	Flash Memory Read Enable
36	FMWRN	O	Flash Memory Write Enable

Pin #	Pin Name	I/O	Description
37	FMDATAL7	I/O	Flash Memory (L) Data [7]
38	FMDATAL6	I/O	Flash Memory (L) Data [6]
39	FMDATAL5	I/O	Flash Memory (L) Data [5]
40	FMDATAL4	I/O	Flash Memory (L) Data [4]
41	FMDATAL3	I/O	Flash Memory (L) Data [3]
42	FMDATAL2	I/O	Flash Memory (L) Data [2]
43	FMDATAL1	I/O	Flash Memory (L) Data [1]
44	FMDATAL0	I/O	Flash Memory (L) Data [0]
45	FMCLE	O	Flash Memory Command Latch Enable
46	FMALE	O	Flash Memory Address Latch Enable
47	FMRBNH	I	Flash Memory (H) Ready and Busy Signal (0=Busy; 1=Ready)
48	FMRBNL	I	Flash Memory (L) Ready and Busy Signal (0=Busy; 1=Ready)

4.0 System Architecture and Reference Design

4.1 AU6388 Block Diagram

Figure 4.1 AU6388 Block Diagram



5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply	-0.3 to V_{CC}+0.3	V
V_{IN}	Input Voltage	-0.3 to 3.6	V
V_{OUT}	Output Voltage	-0.3 to V_{CC}+0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{DD}	Digital Supply	2.25	2.5	2.75	V
V_{IN}	Input Voltage	0	3.3	5.2	V
T_{OPR}	Operating Temperature	0	25	125	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{CC}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\|I_{ol}\|$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\|I_{oh}\|$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	40	75	190	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	190	KΩ
I_{in}	Input leakage current	V_{in}= V_{CC} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AVCC	Analog supply Voltage		3.0	3.3	3.6	V
VCC	Digital supply Voltage		2.25	2.5	2.75	V
I_{CC}	Operating supply current	High speed operating at 480 MHz			73	mA
$I_{CC\ (susp)}$	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

Table 5.6 Static characteristic：Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
Output levels						
V_{OL}	Low-level output voltage				0.2	V
V_{OH}	High-level output voltage		VCC-0.2			V

AVCC=3.0V~3.6V；VCC=2.25V~2.75V；Temp=0℃~115℃

Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver（HS）						
Input Levels（differential receiver）						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV

V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver（FS/LS）						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

AVCC=3.0V~3.6V；VCC=2.25V~2.75V；Temp=0℃~115℃

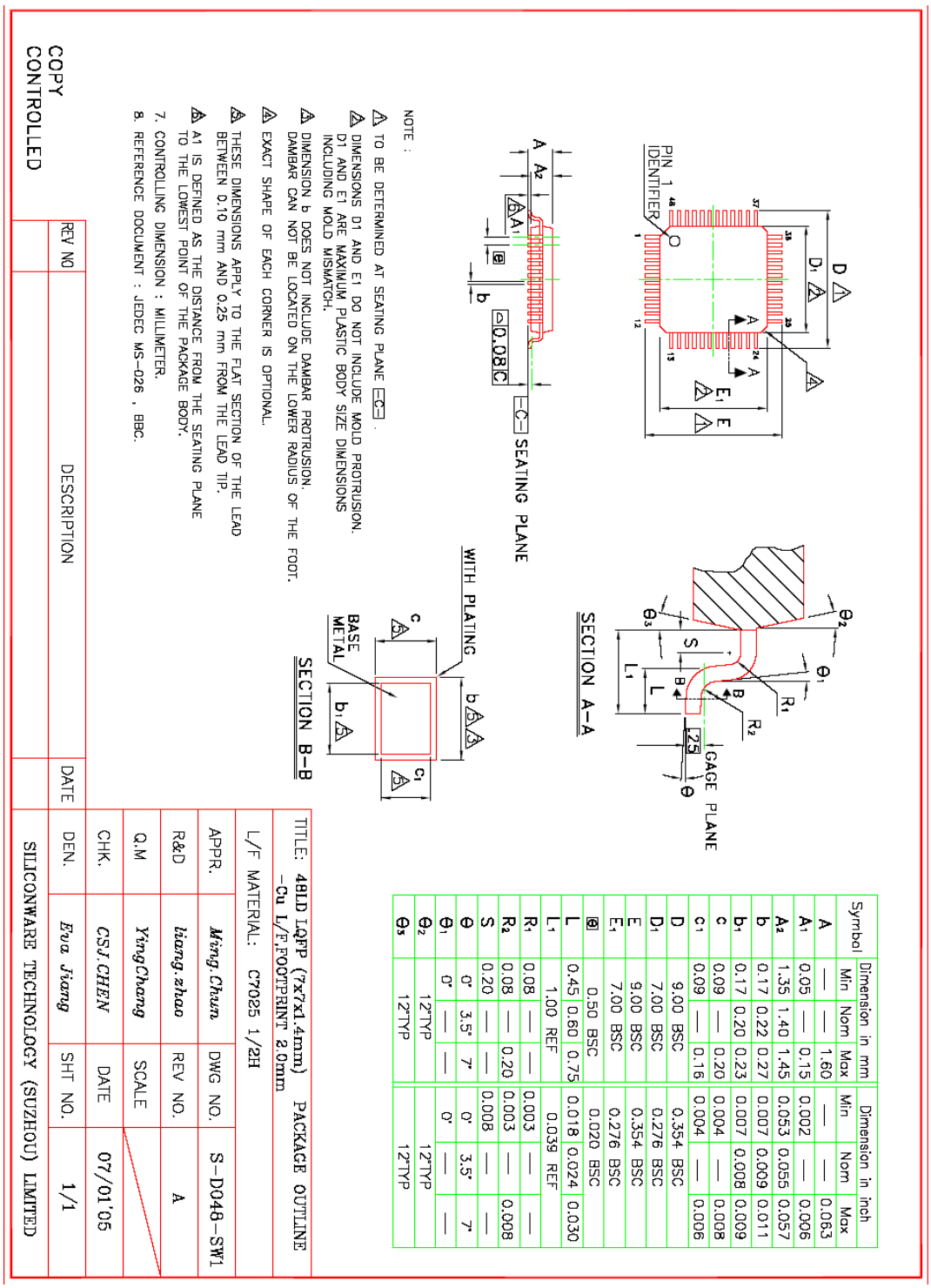
Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%

V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF ; 10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$;	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF ; 90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$;	75		300	ns
t_{LRMA}	Differential rise/fall time matching（t_{LR} / t_{LF}）	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

6.0 Mechanical Information

Figure 6.1 Mechanical Information Diagram



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D_1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E_1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	12°TYP			12°TYP		
θ_3	12°TYP			12°TYP		

7.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification

Autorun Automatically execute the customized images file to illustrate company logo or branding image.

iRUN The smart application – iRun handy tool for AU6388 to manage USB storage device.

【MEMO】

About Alcor Micro, Corp

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.