



Integrated Device Technology, Inc.

# 3.3V CMOS 16-BIT BUS TRANSCEIVER/ REGISTERS

IDT74FCT163646/A/C

## FEATURES:

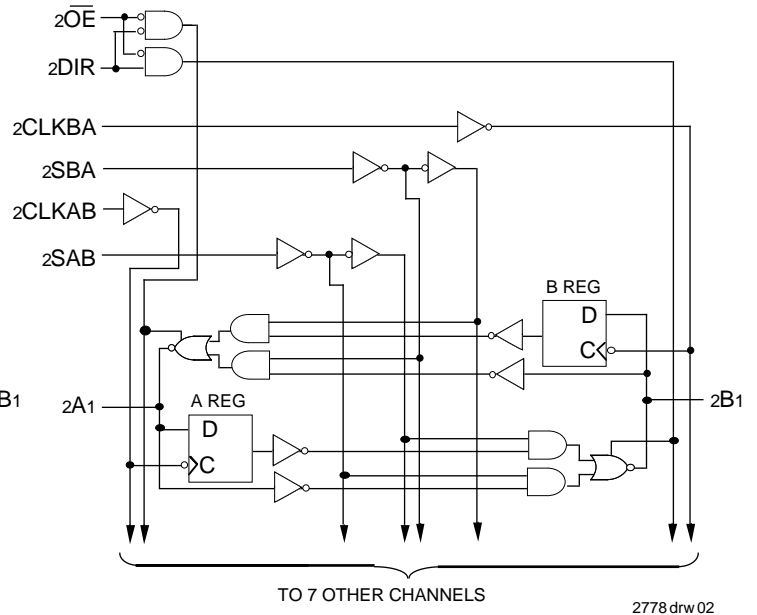
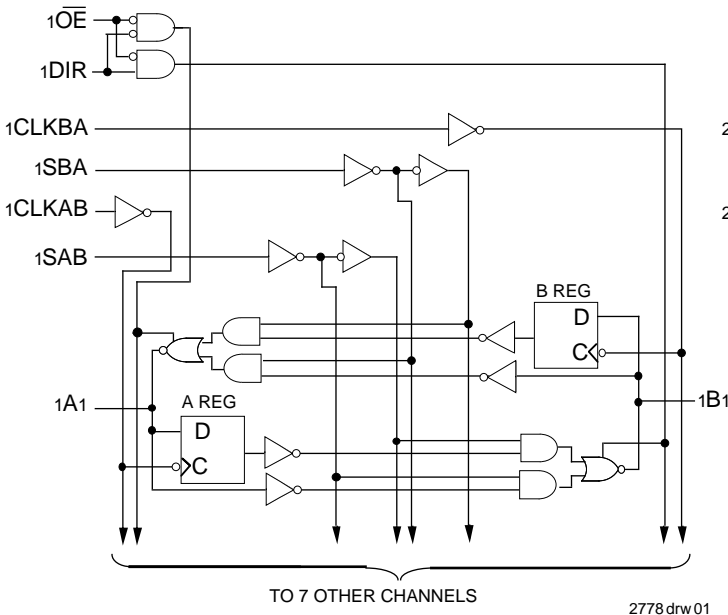
- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP and 15.7 mil pitch TVSOP
- Extended commercial range of -40°C to +85°C
- VCC = 3.3V ±0.3V, Normal Range or VCC = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

## DESCRIPTION:

The FCT163646/A/C 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (xDIR), over-riding Output Enable control (xOE) and Select lines (xSAB and xSBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the LOW-to-HIGH transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163646/A/C have series current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

## FUNCTIONAL BLOCK DIAGRAM

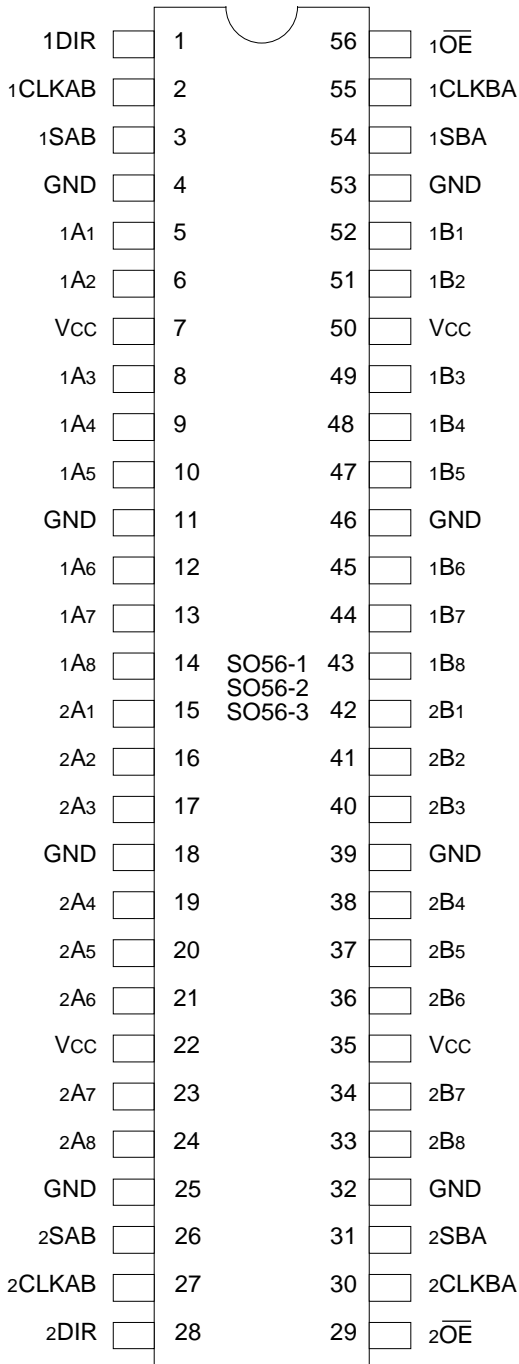


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGES

AUGUST 1996

## PIN CONFIGURATIONS



SSOP/  
TSSOP/TVSOP  
TOP VIEW

2778.drw 03

## PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCAB, xCBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xDIR, xOE	Output Enable Inputs

2778.tbl 01

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
VTERM <sup>(4)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC + 0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +60	mA

2778.lnk 03

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- Input terminals.
- Output and I/O terminals.

## CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6.0	pF
Ci/O	I/O Capacitance	VOUT = 0V	3.5	8.0	pF

### NOTE:

2778.lnk 04

- This parameter is measured at characterization but not tested.

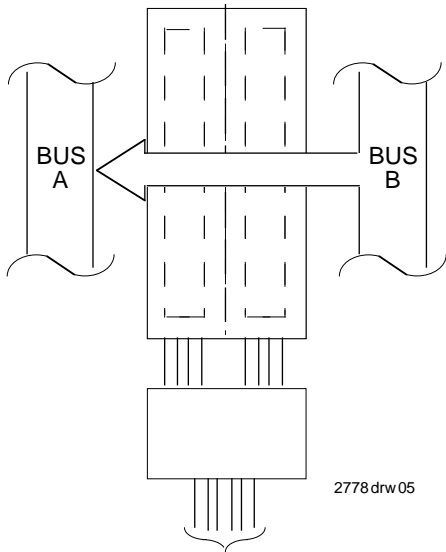
**FUNCTION TABLE<sup>(2)</sup>**

Inputs						Data I/O <sup>(1)</sup>		Operation or Function
x $\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

**NOTES:**

2778 tbl 02

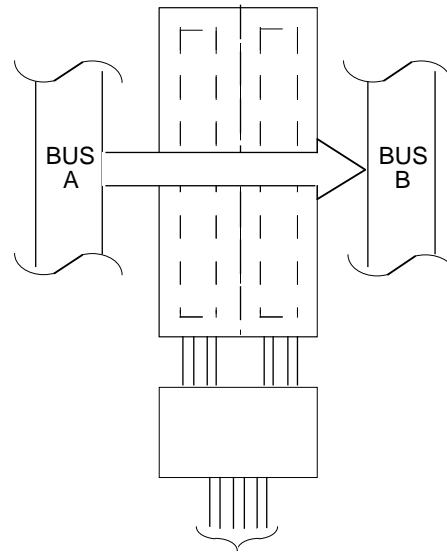
1. The data output functions may be enabled or disabled by various signals at the x $\overline{OE}$  or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ =LOW-to-HIGH Transition



2778 drw 05

xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

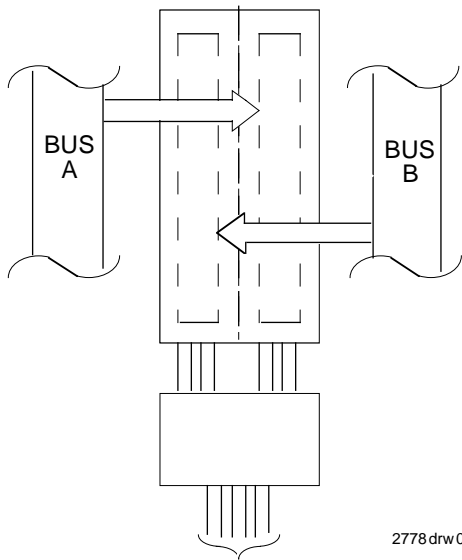
**REAL-TIME TRANSFER  
BUS B TO A**



2778 drw 06

xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

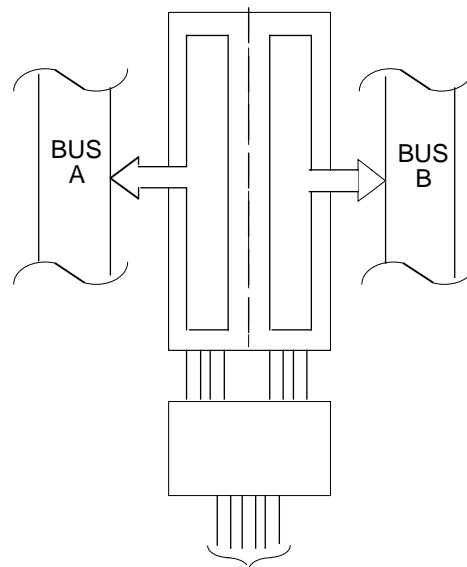
**REAL-TIME TRANSFER  
BUS A TO B**



2778 drw 07

xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

**STORAGE FROM  
A AND/OR B**



2778 drw 08

xDIR <sup>(1)</sup>	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

**TRANSFER STORED  
DATA TO A AND/OR B**

**NOTE:**

1. Cannot transfer data to A bus and B bus simultaneously.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:  
Commercial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit		
V <sub>IH</sub>	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2.0	—	5.5	V		
	Input HIGH Level (I/O pins)		2.0	—	V <sub>CC</sub> +0.5			
V <sub>IL</sub>	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V		
I <sub>IH</sub>	Input HIGH Current (Input pins)	V <sub>CC</sub> = Max.	V <sub>I</sub> = 5.5V	—	—	±1	μA	
	Input HIGH Current (I/O pins)							V <sub>I</sub> = V <sub>CC</sub>
I <sub>IL</sub>	Input LOW Current (Input pins)		V <sub>I</sub> = GND	—	—	±1		
	Input LOW Current (I/O pins)		V <sub>I</sub> = GND	—	—	±1		
IOZ <sub>H</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = Max.	V <sub>O</sub> = V <sub>CC</sub>	—	—	±1	μA	
IOZ <sub>L</sub>			V <sub>O</sub> = GND	—	—	±1		
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V		
IOD <sub>H</sub>	Output HIGH Current	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = 1.5V <sup>(3)</sup>	-36	-60	-110	mA		
IOD <sub>L</sub>	Output LOW Current	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = 1.5V <sup>(3)</sup>	50	90	200	mA		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min.	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> -0.2	—	—	V	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -3mA	2.4	3.0	—		
		V <sub>CC</sub> = 3.0V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -8mA	2.4 <sup>(5)</sup>	3.0	—		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 0.1mA	—	—	0.2	V	
			I <sub>OL</sub> = 16mA	—	0.2	0.4		
			I <sub>OL</sub> = 24mA	—	0.3	0.55		
		V <sub>CC</sub> = 3.0V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 24mA	—	0.3	0.50		
I <sub>OS</sub>	Short Circuit Current <sup>(4)</sup>	V <sub>CC</sub> = Max., V <sub>O</sub> = GND <sup>(3)</sup>	-60	-135	-240	mA		
V <sub>H</sub>	Input Hysteresis	—	—	150	—	mV		
ICCL ICCH IC CZ	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub>	—	0.1	10	μA		

2778 Ink 05

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V<sub>OH</sub> = V<sub>CC</sub> - 0.6V at rated current.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2.0	30	$\mu A$
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $xDIR = x\overline{OE} = GND$ 50% Duty Cycle One Input Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	60	100	$\mu A / MHz$
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10MHz (xCLKBA)$ 50% Duty Cycle $xDIR = x\overline{OE} = GND$ $f_i = 5MHz$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.6	1.0	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	—	0.6	1.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10MHz (xCLKBA)$ 50% Duty Cycle $xDIR = x\overline{OE} = GND$ $f_i = 2.5MHz$ 50% Duty Cycle Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	3.0	5.0 <sup>(5)</sup>	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	—	3.0	5.3 <sup>(5)</sup>	

### NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 3.3V$ ,  $+25^\circ C$  ambient.
- Per TTL driven input; all other inputs at  $V_{CC}$  or  $GND$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH_{NT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current } (I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$   
 $DH = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } DH$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

2778 tbl 06

### SWITCHING CHARACTERISTICS OVER OPERATING RANGE<sup>(4)</sup>

Symbol	Parameter	Condition <sup>(1)</sup>	FCT163646		FCT163646A		FCT163646C		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time xDIR or x $\overline{OE}$ to Bus		2.0	14.0	2.0	9.8	1.5	7.8	ns
t <sub>PHZ</sub> t <sub>P LZ</sub>	Output Disable Time xDIR or x $\overline{OE}$ to Bus		2.0	9.0	2.0	6.3	1.5	6.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW Bus to Clock		4.0	—	2.0	—	2.0	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW Bus to Clock		2.0	—	1.5	—	1.5	—	ns
t <sub>w</sub>	Clock Pulse Width HIGH or LOW		6.0	—	5.0	—	5.0	—	ns
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	—	0.5	ns

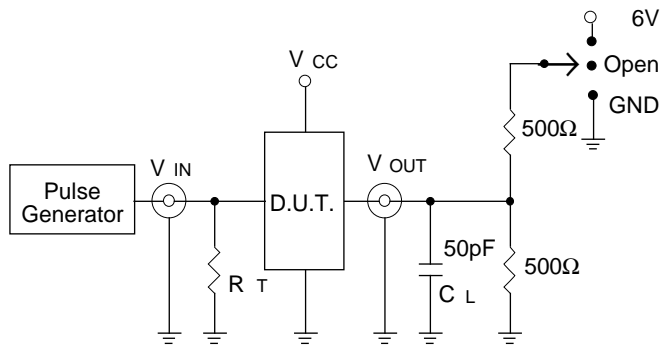
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V<sub>CC</sub> = 3.3V ± 0.3V, Normal Range. For V<sub>CC</sub> = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

2778 tbl 07

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



2778 drw 09

### SWITCH POSITION

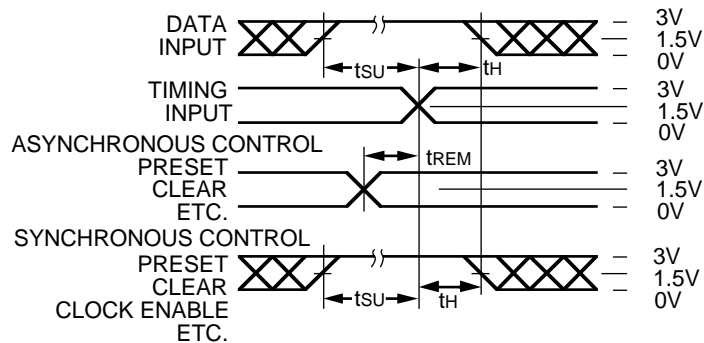
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

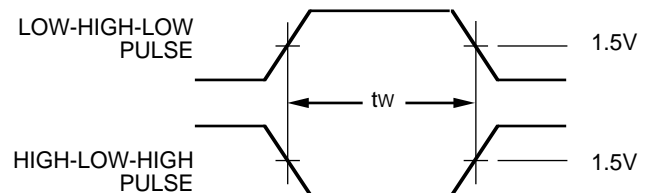
2778 Ink 08

### SET-UP, HOLD AND RELEASE TIMES



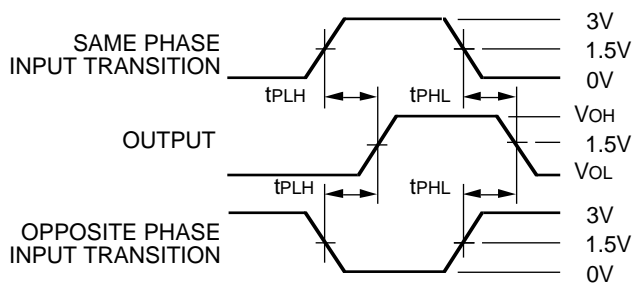
2778 drw 10

### PULSE WIDTH



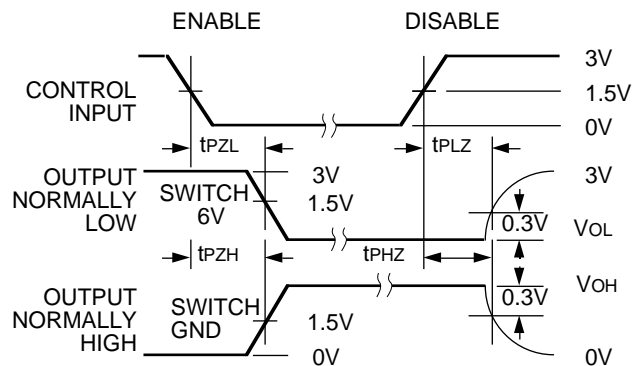
2778 drw 11

### PROPAGATION DELAY



2778 drw 12

### ENABLE AND DISABLE TIMES



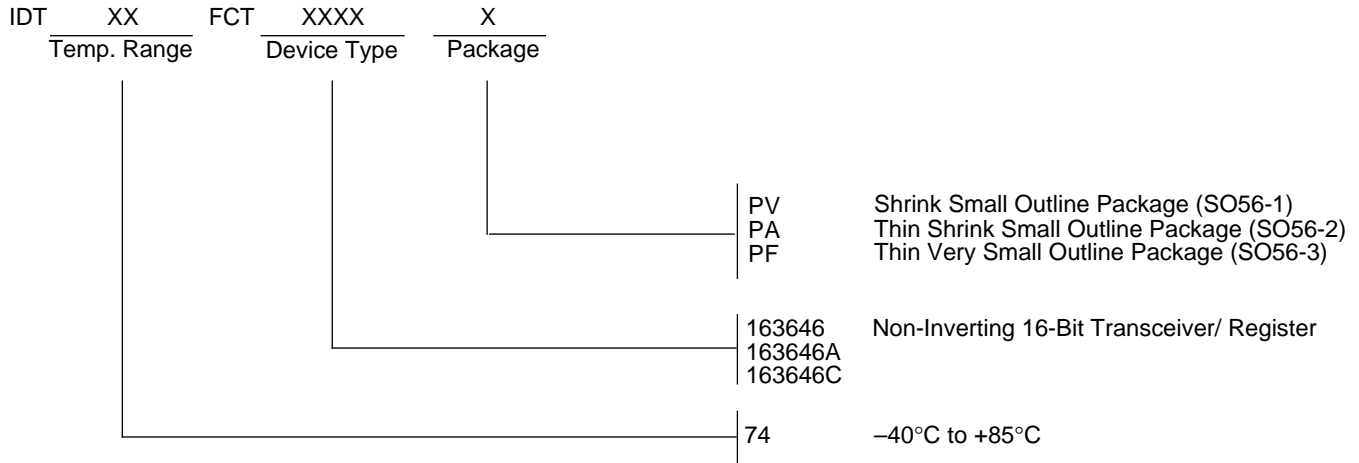
2778 drw 13

#### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$ .
3. If  $V_{CC}$  is below 3V, input voltage swings should be adjusted not to exceed  $V_{CC}$ .



## ORDERING INFORMATION



2778 drw14