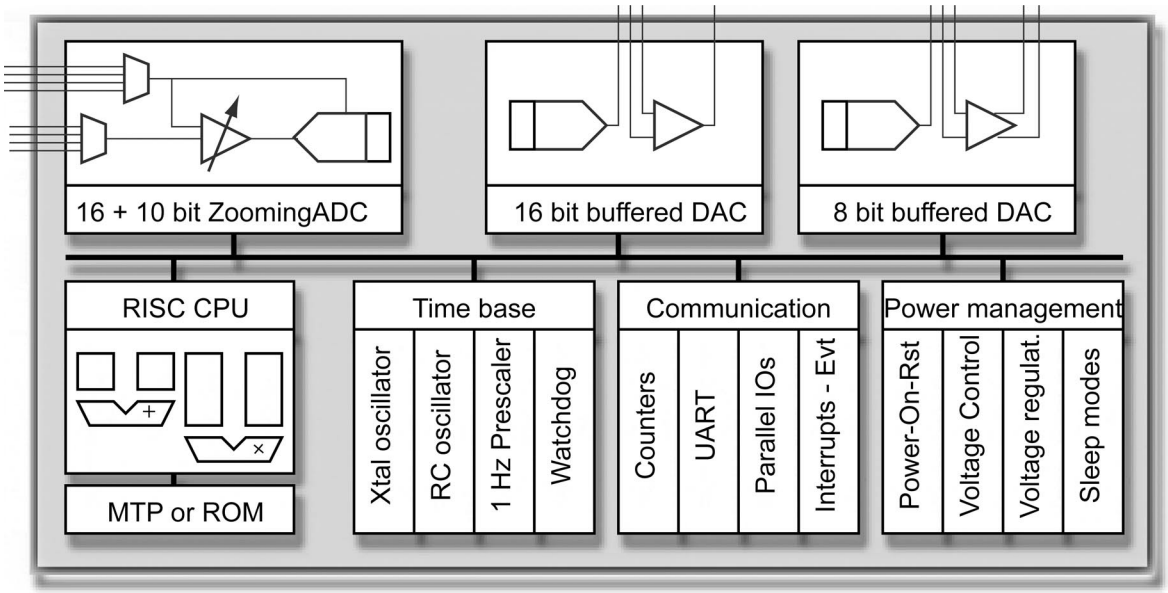

XE88LC05

16 + 10 bit Data Acquisition Ultra Low-Power Microcontroller

General Description

The XE88LC05 is an ultra low-power microcontroller unit (MCU) associated with a versatile analog-to-digital converter (ADC) including a programmable offset and gain pre-amplifier (PGA) and digital-to-analog converters (DACs).

XE88LC05 is available with on chip Multiple-Time-Programmable (MTP) Flash program memory and ROM.

Applications

- Internet connected appliances
- Portable, battery operated instruments
- Piezoresistive bridge sensors
- 4-20 mA bus sensors
- 0.5 - 4.5 V sensors
- HVAC control
- Motor control

Key product Features

- Low-power, high resolution ZoomingADC
  - 0.5 to 1000 gain with offset cancellation
  - up to 16 bits ADC
  - up to 13 input multiplexer
- Buffered signal-DAC (up to 16 bits)
- Buffered bias-DAC (up to 10 mA drive)
- Low-voltage low-power controller operation
  - 2 MIPS at 2.4 V to 5.5 V supply voltage
  - 300 µA at 1 MIPS, 2.4 V to 5.5 V supply
- 22 kByte (8 kInstruction) MTP, 520 Byte RAM
- RC and crystal oscillators
- 5 reset, 18 interrupt, 8 event sources

Ordering Information

Reference	Memory type	Temperature	Package
XE88LC05MI000	MTP Flash	-40°C to 85°C	die
XE88LC05MI028	MTP Flash	-40°C to 85°C	LQFP64
XE88LC05RI000	ROM	-40°C to 125°C	die
XE88LC05RI028	ROM	-40°C to 125°C	LQFP64

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1 Detailed Pin Description

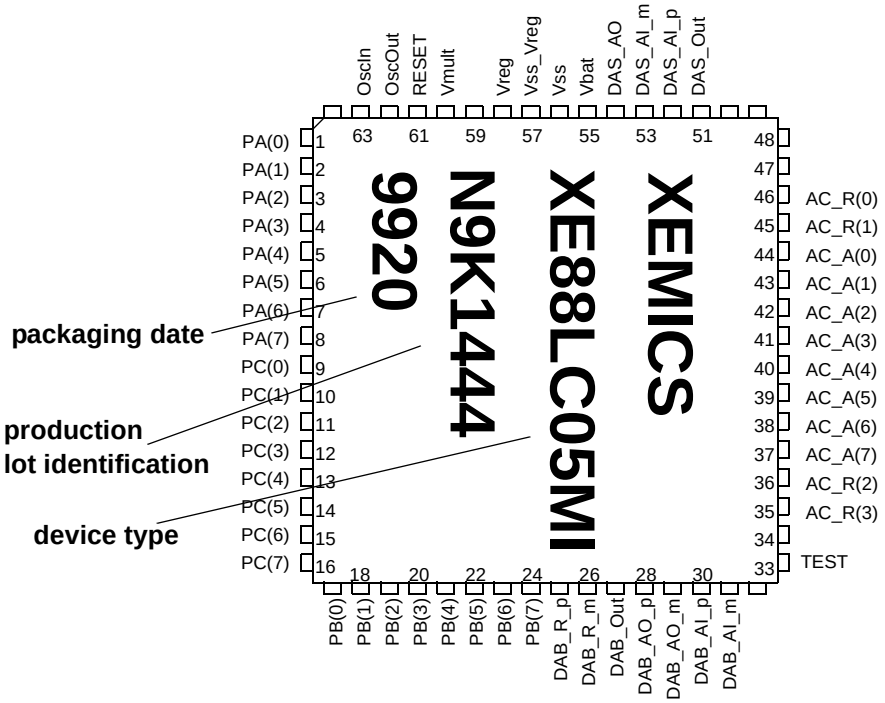


Figure 1.1: Pinout of the XE88LC05 in LQFP64 package

Pin				Description
Position	Function name	Second function name	Type	
1	PA(0)		Input	Input of Port A/ Data input for MTP programming/ Counter A input
2	PA(1)		Input	Input of Port A/ Data clock for MTP programming/ Counter B input
3	PA(2)		Input	Input of Port A/ Counter C input/ Counter capture input
4	PA(3)		Input	Input of Port A/ Counter D input/ Counter capture input
5	PA(4)		Input	Input of Port A
6	PA(5)		Input	Input of Port A
7	PA(6)		Input	Input of Port A
8	PA(7)		Input	Input of Port A
9	PC(0)		Input/Output	Input-Output of Port C
10	PC(1)		Input/Output	Input-Output of Port C
11	PC(2)		Input/Output	Input-Output of Port C
12	PC(3)		Input/Output	Input-Output of Port C
13	PC(4)		Input/Output	Input-Output of Port C
14	PC(5)		Input/Output	Input-Output of Port C
15	PC(6)		Input/Output	Input-Output of Port C
16	PC(7)		Input/Output	Input-Output of Port C

Table 1.1: Pin-out of the XE88LC05 in LQFP64
(see Table “IO pins performances” on page 17 for drive capabilities of the pins)

Pin				Description
Position	Function name	Second function name	Type	
17	PB(0)		Input/Output/Analog	Input-Output-Analog of Port B/ Data output for MTP programming/ PWM output
18	PB(1)		Input/Output/Analog	Input-Output-Analog of Port B/ PWM output
19	PB(2)		Input/Output/Analog	Input-Output-Analog of Port B
20	PB(3)	SOUT	Input/Output/Analog	Input-Output-Analog of Port B, Output pin of USRT
21	PB(4)	SCL	Input/Output/Analog	Input-Output-Analog of Port B/ Clock pin of USRT
22	PB(5)	SIN	Input/Output/Analog	Input-Output-Analog of Port B/ Data input or input-output pin of USRT
23	PB(6)	Tx	Input/Output/Analog	Input-Output-Analog of Port B/ Emission pin of UART
24	PB(7)	Rx	Input/Output/Analog	Input-Output-Analog of Port B/ Reception pin of UART
25	DAB_R_p		Analog	Positive reference of bias DAC
26	DAB_R_m		Analog	Negative reference of bias DAC
27	DAB_Out		Analog	Output of bias DAC
28	DAB_AO_p		Analog	Highest potential output of bias DAC buffer
29	DAB_AO_m		Analog	Lowest potential output of bias DAC buffer
30	DAB_AI_p		Analog	Positive input of bias DAC buffer
31	DAB_AI_m		Analog	Negative input of bias DAC buffer
32			Not connected	Spare pins to be connected to negative power supply
33	VPP	TEST/Vhigh	Special	Test mode/High voltage for MTP programming
34			Not connected	Spare pins to be connected to negative power supply
35	AC_R(3)		Analog	Highest potential node for 2nd reference of ADC
36	AC_R(2)		Analog	Lowest potential node for 2nd reference of ADC
37	AC_A(7)		Analog	ADC input node
38	AC_A(6)		Analog	ADC input node
39	AC_A(5)		Analog	ADC input node
40	AC_A(4)		Analog	ADC input node
41	AC_A(3)		Analog	ADC input node
42	AC_A(2)		Analog	ADC input node
43	AC_A(1)		Analog	ADC input node
44	AC_A(0)		Analog	ADC input node
45	AC_R(1)		Analog	Highest potential node for 1st reference of ADC
46	AC_R(0)		Analog	Lowest potential node for 1st reference of ADC
47-50			Not connected	Spare pins to be connected to negative power supply
51	DAS_Out		Analog	Output of signal DAC
52	DAS_AI_p		Analog	Positive input of signal DAC buffer
53	DAS_AI_m		Analog	Negative input of signal DAC buffer
54	DAS_AO		Analog	Output of signal DAC buffer
55	Vbat	VDD	Power	Positive power supply
56	Vss		Power	Negative power supply, connected to substrate
57	Vss_Reg		Power	Digital negative power supply, must be equal to Vss
58	Vreg		Analog	Regulated supply
59			Not connected	Spare pins to be connected to negative power supply
60	Vmult		Analog	Pad for optional voltage multiplier capacitor
61	RESET		Input	Reset pin (active high)
62	Xout	OscOut/ptck	Analog/Input	Connection to Xtal/ Peripheral clock for MTP programming
63	Xin	OscIn/crck	Analog/Input	Connection to Xtal/ CoolRISC clock for MTP programming
64	-		-	Do not connect, or VSS

Table 1.1: Pin-out of the XE88LC05 in LQFP64
(see Table “IO pins performances” on page 17 for drive capabilities of the pins)

2 Absolute maximum ratings

Stresses beyond these listed in this chapter may cause permanent damage to the device. No functional operation is implied at or beyond these conditions. Exposure to these conditions for an extended period may affect the device reliability.

Parameter	Value	Remarks
VBAT with respect to VSS	-0.3V to 6.0V	
Input voltage on any input pin	VSS-0.3V to VBAT+0.3V	
Storage temperature	-55°C to 125°C	1
Storage temperature for programmed MTP devices	-40°C to 85°C	1

Table 2.1: Absolute maximum ratings

Note: 1) For unprogrammed MTP devices. Blocking bits and software must be rewritten in MTP devices if storage temperature exceedes storage temperature for programmed devices.

These devices are ESD sensitive. Although these devices feature proprietary ESD protection structures, permanent damage may occur on devices subjected to high energy electrostatic discharges. Proper ESD precautions have to be taken to avoid performance degradation or loss of functionality.

3 Electrical Characteristics

All specification are -40°C to 85°C unless otherwise noted. ROM operates up to 125°C.

Operation conditions		min	typ	max	Unit	Remarks
Power supply	ROM version	2.4		5.5	V	
	MTP version	2.4		5.5	V	
Operating speed	2.4 V to 5.5 V	0.032		2	MHz	
Instruction cycle	any instruction		500		ns	7
Current requirement	CPU running at 1 MIPS			310	uA	1
	CPU running at 32 kHz on Xtal, RC off			10	uA	1
	CPU halt, timer on Xtal, RC off			1	uA	1
	CPU halt, timer on Xtal, RC ready			1.7	uA	1
	CPU halt, Xtal off timer on RC at 100 kHz			1.4	uA	1
Current requirement	CPU halt, ADC 16 bits at 4 kHz		190		uA	4,6
	CPU halt, ADC 12 bits at 4 kHz, PGA gain 100		460		uA	4,6
	CPU at 1 MIPS, ADC 12 bits and DAC 10 bits at 4 kHz		670		uA	3,4,6
	CPU at 1 MIPS, ADC 12 bits and DAC 10 bits at 4 kHz, PGA gain 10		790		uA	3,4,6
	CPU at 1 MIPS, ADC 12 bits and DAC 10 bits at 4 kHz, PGA gain 100		940		uA	3,4,6
	CPU at 1 MIPS, ADC 12 bits and DAC 10 bits at 4 kHz, PGA gain 1000		1100		uA	3,4,6
	Voltage level detection			15	uA	
MTP Flash instruction memory	Prog. voltage	10.3		10.8	V	
	Erase time	0.2		1	s	8
	Write/Erase cycles	10	100			5
	Data retention	10			year	2

Table 3.1: Specifications and current requirement of the XE88LC05

Note:
1) Power supply: 2.4 V - 5.5 V, temperature is 27°C.
2) Temperature < 85°C, < 10 erase cycles.
3) Output not loaded.
4) Current requirement can be divided by a factor of 2 or 4 by reducing the speed accordingly.
5) More cycles possible during development, with restraint retention

6) Power supply: 3.0V, at 27°C; see chapter Power Consumption on page 30 for variation of current with voltage and clock speed variation
7) With 2 MHz clock, all instructions are using exactly 1 clock cycle
8) Longer erase time may degrade retention

4 CPU

The XE88LC05 CPU is a low power RISC core. It has 16 internal registers for efficient implementation of the C compiler. Its instruction set is made of 35 generic instructions, all coded on 22 bits, with 8 addressing modes. All instructions are executed in one clock cycle, including conditional jumps and 8x8 multiplication.

5 Memory organization

The CPU uses a Harvard architecture, so that memory is organized in two separated fields: program memory and data memory. As both memories are separated, the central processing unit can read/write data at the same time it loads an instruction. Peripherals and system control registers are mapped on data memory space.

Program memory is made in one page. Data is made of several 256 bytes pages.

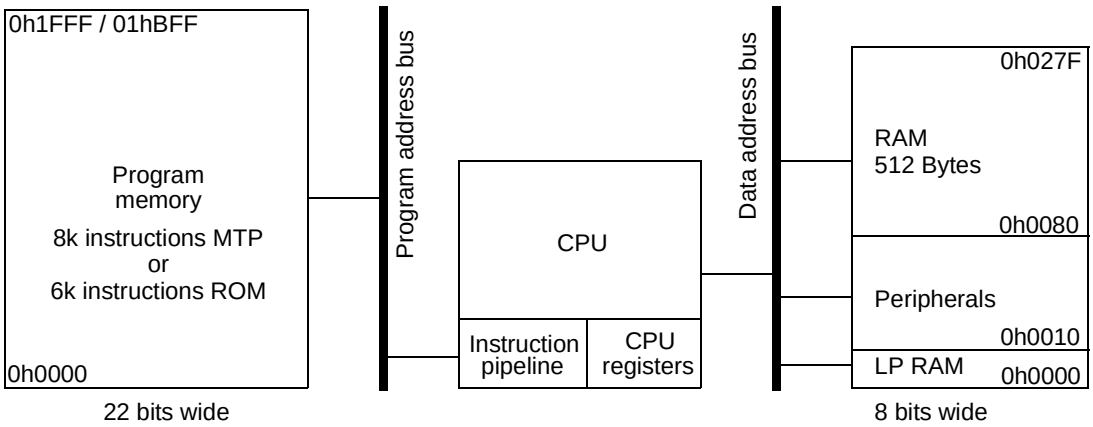


Figure 5.1: Memory organization

5.1 Program memory

The program memory is implemented as Multiple Time Programmable (MTP) Flash memory or ROM. The power consumption of MTP memory is linear with the access frequency (no significant static current).

Size of the MTP Flash memory is 8192 x 22 bits (= 22 kBytes)

Size of the ROM memory is 6144 x 22 bits (= 17 kBytes)

block	size	address
MTP	8192 x 22	H0000 - H1FFF
ROM	6144 x 22	H0000 - H1BFF

Table 5.1: Program addresses for MTP or ROM memory

5.2 Data memory

The data memory is implemented as static Random-Access Memory (RAM). The RAM size is 512 x 8 bits plus 8 low power RAM bytes that require very low current when addressed. Programs using the low-power RAM instead of RAM will use even less current.

block	size	address
LP RAM	8 x 8	H0000 - H0007
RAM	512 x 8	H0080 - H027F

Table 5.2: RAM addresses

6 Registers list

Left column include register name and address.

Right columns include bit name, access (r: read, r0: always 0 when read, w: write, c: cleared by writing any value, c1: cleared by writing 1), and reset status (0 or 1) and signal. Empty bits are reserved for future use and should not be written, neither should their read value be used for any purpose as it may change without notice.

6.1 Peripherals mapping

block	size	address	Page
LP RAM	8x8	H0000-H0007	Page 0
System control	16x8	H0010-H001F	
Port A	8x8	H0020-H0027	
Port B	8x8	H0028-H002F	
Port C	4x8	H0030-H0033	
Reserved	4x8	H0034-H0037	
MTP	4x8	H0038-H003B	
Event	4x8	H003C-H003F	
Interrupts control	8x8	H0040-H0047	
reserved	8x8	H0048-H004F	
UART	8x8	H0050-H0057	
Counters	8x8	H0058-H005F	
Zooming ADC	8x8	H0060-H0067	
Reserved	12x8	H0068-H0073	
DACs	8x8	H0074-H007B	
Other (VLD)	4x8	H007C-H007F	
RAM1	128x8	H0080 - H00FF	
RAM2	256x8	H0100 - H01FF	Page 1
RAM3	128x8	H0200 - H027F	Page 2

Table 6.1: Peripherals addresses

6.2 Resets

The reset source name is simplified in the following registers description. Name mapping is in the next table.

reset source	name in this document
resetsystem	global
resetSynch	
resetPOR	cold
resetCold	
resetPad	
resetPconf	pconf
resetSleep	sleep

Table 6.2: Reset signal name mapping

6.3 Low power RAM

Low power RAM is a small additionnal RAM area with extremely low power requirement.

Name Address	7	6	5	4	3	2	1	0
h0000	rw	rw	rw	rw	rw	rw	rw	rw
h0001	rw	rw	rw	rw	rw	rw	rw	rw
h0002	rw	rw	rw	rw	rw	rw	rw	rw
h0003	rw	rw	rw	rw	rw	rw	rw	rw
h0004	rw	rw	rw	rw	rw	rw	rw	rw
h0005	rw	rw	rw	rw	rw	rw	rw	rw
h0006	rw	rw	rw	rw	rw	rw	rw	rw
h0007	rw	rw	rw	rw	rw	rw	rw	rw

Table 6.3: Low power RAM

6.4 System, oscillators, prescaler and watchdog

Name Address	7	6	5	4	3	2	1	0
RegSysCtrl h0010, type 1	SleepEn rw, 0 por	EnRes-PConf rw, 0 cold	EnBus-Error rw, 0 cold	EnResWD rw, 0 cold				
RegSysReset h0011, type 1	Sleep w, 0 cold	ResPor r, 0	ResBus-Error rc, 0 cold	ResWD rc, 0 cold	ResPortA rc, 0 cold	ResPad-Deb rc, 0 cold	ResPad rc, 0 cold	
RegSysClock h0012, type 1	CpuSel rw, 0 sleep	ExtClk r, 0 cold	EnExtClk rw, 0 cold	BiasRC rw, 1 cold	ColdXtal r, 1 sleep	ColdRC r, 1 sleep	EnableXtal rw, 0 sleep	EnableRC rw, 1 sleep
RegSysMisc h0013, type 1					RCOnPA0 rw, 0 sleep	DebFast rw, 0 sleep	Output-CkXtal rw, 0 sleep	Output-CkCPU rw, 0 sleep
RegSysWD h0014					WatchDog(3) special	WatchDog(2) special	WatchDog(1) special	WatchDog(0) special
RegSysPre0 h0015								ResPre ClearLow-Prescal (*) w, 0 cold
RegSysRCTrim1 h001B				RCFreq-Range rw, 0 cold	RCFreq-Coarse(3) rw, 0 cold	RCFreq-Coarse(2) rw, 0 cold	RCFreq-Coarse(1) rw, 0 cold	RCFreq-Coarse(0) rw, 0 cold
RegSysRCTrim2 h001C			RCFreq-Fine(5) rw, 1 cold	RCFreq-Fine(4) rw, 0 cold	RCFreq-Fine(3) rw, 0 cold	RCFreq-Fine(2) rw, 0 cold	RCFreq-Fine(1) rw, 0 cold	RCFreq-Fine(0) rw, 0 cold

Table 6.4: System control registers

6.5 PortA

Name Address	7	6	5	4	3	2	1	0
RegPAIn h0020	PAIn(7) r	RegPAIn(6) r	PAIn(5) r	PAIn(4) r	PAIn(3) r	PAIn(2) r	PAIn(1) r	PAIn(0) r
RegPADebounce h0021	PADeb(7) rw, 0 pconf	PADeb(6) rw, 0 pconf	PADeb(5) rw, 0 pconf	PADeb(4) rw, 0 pconf	PADeb(3) rw, 0 pconf	PADeb(2) rw, 0 pconf	PADeb(1) rw, 0 pconf	PADeb(0) rw, 0 pconf
RegPAEdge h0022	PAEdge(7) rw, 0 global	PAEdge(6) rw, 0 global	PAEdge(5) rw, 0 global	PAEdge(4) rw, 0 global	PAEdge(3) rw, 0 global	PAEdge(2) rw, 0 global	PAEdge(1) rw, 0 global	PAEdge(0) rw, 0 global
RegPAPullup h0023, type 1	PAPullUp(7) rw, 0 pconf	PAPullUp(6) rw, 0 pconf	PAPullUp(5) rw, 0 pconf	PAPullUp(4) rw, 0 pconf	PAPullUp(3) rw, 0 pconf	PAPullUp(2) rw, 0 pconf	PAPullUp(1) rw, 0 pconf	PAPullUp(0) rw, 0 pconf
RegPARes0 h0024	PARes0(7) rw, 0 global	PARes0(6) rw, 0 global	PARes0(5) rw, 0 global	PARes0(4) rw, 0 global	PARes0(3) rw, 0 global	PARes0(2) rw, 0 global	PARes0(1) rw, 0 global	PARes0(0) rw, 0 global
RegPARes1 h0025	PARes1(7) rw, 0 global	PARes1(6) rw, 0 global	PARes1(5) rw, 0 global	PARes1(4) rw, 0 global	PARes1(3) rw, 0 global	PARes1(2) rw, 0 global	PARes1(1) rw, 0 global	PARes1(0) rw, 0 global

Table 6.5: Port A registers

6.6 PortB

Name Address	7	6	5	4	3	2	1	0
RegPBOut h0028	PBOut(7) rw, 0 pconf	PBOut(6) rw, 0 pconf	PBOut(5) rw, 0 pconf	PBOut(4) rw, 0 pconf	PBOut(3) rw, 0 pconf	PBOut(2) rw, 0 pconf	PBOut(1) rw, 0 pconf	PBOut(0) rw, 0 pconf
RegPBIn h0029	PBIn(7) r	PBIn(6) r	PBIn(5) r	PBIn(4) r	PBIn(3) r	PBIn(2) r	PBIn(1) r	PBIn(0) r
RegPBDir h002A	PBDir(7) rw, 0 pconf	PBDir(6) rw, 0 pconf	PBDir(5) rw, 0 pconf	PBDir(4) rw, 0 pconf	PBDir(3) rw, 0 pconf	PBDir(2) rw, 0 pconf	PBDir(1) rw, 0 pconf	PBDir(0) rw, 0 pconf
RegPBOpen h002B	PBOpen(7) rw, 0 pconf	PBOpen(6) rw, 0 pconf	PBOpen(5) rw, 0 pconf	PBOpen(4) rw, 0 pconf	PBOpen(3) rw, 0 pconf	PBOpen(2) rw, 0 pconf	PBOpen(1) rw, 0 pconf	PBOpen(0) rw, 0 pconf
RegPBPullup h002C	PBPullUp(7) rw, 0 pconf	PBPullUp(6) rw, 0 pconf	PBPullUp(5) rw, 0 pconf	PBPullUp(4) rw, 0 pconf	PBPullUp(3) rw, 0 pconf	PBPullUp(2) rw, 0 pconf	PBPullUp(1) rw, 0 pconf	PBPullUp(0) rw, 0 pconf
RegPBAna h002D					PBAna(3) rw, 0 pconf	PBAna(2) rw, 0 pconf	PBAna(1) rw, 0 pconf	PBAna(0) rw, 0 pconf

Table 6.6: Port B registers

6.7 PortC

Name Address	7	6	5	4	3	2	1	0
RegPCOut h0030	PCOut(7) rw, 0 pconf	PCOut(6) rw, 0 pconf	PCOut(5) rw, 0 pconf	PCOut(4) rw, 0 pconf	PCOut(3) rw, 0 pconf	PCOut(2) rw, 0 pconf	PCOut(1) rw, 0 pconf	PCOut(0) rw, 0 pconf
RegPCIn h0031	PCIn(7) r	PCIn(6) r	PCIn(5) r	PCIn(4) r	PCIn(3) r	PCIn(2) r	PCIn(1) r	PCIn(0) r
RegPCDir h0032	PCDir(7) rw, 0 pconf	PCDir(6) rw, 0 pconf	PCDir) rw, 0 pconf	PCDir(4) rw, 0 pconf	PCDir(3) rw, 0 pconf	PCDir(2) rw, 0 pconf	PCDir(1) rw, 0 pconf	PCDir(0) rw, 0 pconf

Table 6.7: Port C registers

6.8 MTP

Name Address	7	6	5	4	3	2	1	0
RegEEP h0038	rw	rw	rw	rw	rw	rw	rw	rw
RegEEP1 h0039	rw	rw	rw	rw	rw	rw	rw	rw
RegEEP2 h003A	special	special	special	special	special	special	special	special
RegEEP3 h003B	special	special	special	special	special	special	special	special

Table 6.8: MTP control registers

6.9 Events

Name Address	7	6	5	4	3	2	1	0
RegEvn h003C	EvnCntA rc1, 0 global	EvnCntC rc1, 0 global	EvnPre1 rc1, 0 global	EvnPA(1) rc1, 0 global	EvnCntB rc1, 0 global	EvnCntD rc1, 0 global	EvnPre2 rc1, 0 global	EvnPA(0) rc1, 0 global
RegEvnEn h003D	EvnEnCntA rw, 0 global	EvnEnCntC rw, 0 global	EvnEnPre1 rw, 0 global	EvnEnPA(1) rw, 0 global	EvnEnCntB rw, 0 global	EvnEnCntD rw, 0 global	EvnEnPre2 rw, 0 global	EvnEnPA(0) rw, 0 global
RegEvnPriority h003E	EvnPriority(7) r,1 global	EvnPriority(6) r,1 global	EvnPriority(5) r,1 global	EvnPriority(4) r,1 global	EvnPriority(3) r,1 global	EvnPriority(2) r,1 global	EvnPriority(1) r,1 global	EvnPriority(0) r,1 global
RegEvnEvn h003F							EvnHigh r, 0 global	EvnLow r, 0 global

Table 6.9: Events control registers

6.10 Interrupts

Name Address	7	6	5	4	3	2	1	0
RegIrqHig h0040	IrqAc rc1, 0 global	IrqPre1 rc1, 0 global		IrqCntA rc1, 0 global	IrqCntC rc1, 0 global		IrqUartTx rc1, 0 global	IrqUartRx rc1, 0 global
RegIrqMid h0041			IrqPA(5) rc1, 0 global	IrqPA(4) rc1, 0 global	IrqPre2 rc1, 0 global	IrqVld rc1, 0 global	IrqPA(1) rc1, 0 global	IrqPA(0) rc1, 0 global
RegIrqLow h0042	IrqPA(7) rc1, 0 global	IrqPA(6) rc1, 0 global	IrqCntB rc1, 0 global	IrqCntD rc1, 0 global	IrqPA(3) rc1, 0 global	IrqPA(2) rc1, 0 global		
RegIrqEnHig h0043	IrqEnAc rw, 0 global	IrqEnPre1 rw, 0 global		IrqEnCntA rw, 0 global	IrqEnCntC rw, 0 global		IrqEnUartTx rw, 0 global	IrqEnUartRx rw, 0 global
RegIrqEnMid h0044			IrqEnPA(5) rw, 0 global	IrqEnPA(4) rw, 0 global	IrqEnPre2 rw, 0 global	IrqEnVld rw, 0 global	IrqEnPA(1) rw, 0 global	IrqEnPA(0) rw, 0 global
RegIrqEnLow h0045	IrqEnPA(7) rw, 0 global	IrqEnPA(6) rw, 0 global	IrqEnCntB rw, 0 global	IrqEnCntD rw, 0 global	IrqEnPA(3) rw, 0 global	IrqEnPA(2) rw, 0 global		
RegIrqPriority h0046	IrqPriority(7) r, 1 global	IrqPriority(6) r, 1 global	IrqPriority(5) r, 1 global	IrqPriority(4) r, 1 global	IrqPriority(3) r, 1 global	IrqPriority(2) r, 1 global	IrqPriority(1) r, 1 global	IrqPriority(0) r, 1 global
RegIrqIrq h0047						IrqHig r, 0 global	IrqMid r, 0 global	IrqLow r, 0 global

Table 6.10: Interrupts control registers

6.11 USRT

Name Address	7	6	5	4	3	2	1	0
RegUsrtSin h0048								UsrtSin rw, 1 global
RegUsrtScl h0049								UsrtScl rw, 1 global
RegUsrtCtrl h004A					UsrtWaitS0 r, 0 global	UsrtEnWait-Cond1 rw, 0 global	UsrtEnWaitS0 rw, 0 global	UsrtEnable rw, 0 global
RegUsrtData h004D								UsrtData r
RegUsrtEdgeScl h004E								UsrtEdgeScl r, 0 global

Table 6.11: USRT control registers

6.12 UART

Name Address	7	6	5	4	3	2	1	0
RegUartCtrl h0050	UartEcho rw, 0 global	UartEnRx rw, 0 global	UartEnTx rw, 0 global	UartXRx rw, 0 global	UartXTx rw, 0 global	UartBR(2) rw, 1 global	UartBR(1) rw, 0 global	UartBR(0) rw, 1 global
RegUartCmd h0051	SelXtal rw, 0 global	UartWakeup rw, 0 global	UartRCSel(2) rw, 0 global	UartRCSel(1) rw, 0 global	UartRCSel(0) rw, 0 global	UartPM rw, 0 global	UartPE rw, 0 global	UartWL rw, 1 global
RegUartTx h0052	UartTx(7) rw, 0 global	UartTx(6) rw, 0 global	UartTx(5) rw, 0 global	UartTx(4) rw, 0 global	UartTx(3) rw, 0 global	UartTx(2) rw, 0 global	UartTx(1) rw, 0 global	UartTx(0) rw, 0 global
RegUartTxSta h0053							UartTxBusy r, 0 global	UartTxFull r, 0 global
RegUartRx h0054	UartRx(7) r	UartRx(6) r	UartRx(5) r	UartRx(4) r	UartRx(3) r	UartRx(2) r	UartRx(1) r	UartRx(0) r
RegUartRxSta h0055			UartRxSErr r	UartRxPErr r	UartRxFErr r	UartRxOErr c	UartRxBusy r	UartRxFull r

Table 6.12: UART control registers

6.13 Counters

Name Address	7	6	5	4	3	2	1	0
RegCntA h0058	CounterA(7) rw	CounterA(6) rw	CounterA(5) rw	CounterA(4) rw	CounterA(3) rw	CounterA(2) rw	CounterA(1) rw	CounterA(0) rw
RegCntB h0059	CounterB(7) rw	CounterB(6) rw	CounterB(5) rw	CounterB(4) rw	CounterB(3) rw	CounterB(2) rw	CounterB(1) rw	CounterB(0) rw
RegCntC h005A	CounterC(7) rw	CounterC(6) rw	CounterC(5) rw	CounterC(4) rw	CounterC(3) rw	CounterC(2) rw	CounterC(1) rw	CounterC(0) rw
RegCntD h005B	CounterD(7) rw	CounterD(6) rw	CounterD(5) rw	CounterD(4) rw	CounterD(3) rw	CounterD(2) rw	CounterD(1) rw	CounterD(0) rw
RegCntCtrlCk h005C	CntDSel(1) rw	CntDSel(0) rw	CntCSel(1) rw	CntCSel(0) rw	CntBSel(1) rw	CntBSel(0) rw	CntASel(1) rw	CntASel(0) rw
RegCntConfig1 h005D	CntDDownUp rw	CntCDownUp rw	CntBDownUp rw	CntADownUp rw	CascadeCD rw	CascadeAB rw	CntPWM1 rw, 0 global	CntPWM0 rw, 0 global
RegCntConfig2 h005E	CapSel(1) rw, 0 global	CapSel(0) rw, 0 global	CapFunc(1) rw, 0 global	CapFunc(0) rw, 0 global	PWM1Size(1) rw	PWM1Size(0) rw	PWM0Size(1) rw	PWM0Size(0) rw
RegCntOn h005F					CntDEnable rw, 0 global	CntCEnable rw, 0 global	CntBEnable rw, 0 global	CntAEnable rw, 0 global

Table 6.13: Counters control registers

6.14 Acquisition chain

Name Address	7	6	5	4	3	2	1	0
RegAcOutLsb h0060	AdcOutL(7) r	AdcOutL(6) r	AdcOutL(5) r	AdcOutL(4) r	AdcOutL(3) r	AdcOutL(2) r	AdcOutL(1) r	AdcOutL(0) r
RegAcOutMsb h0061	AdcOutM(7) r	AdcOutM(6) r	AdcOutM(5) r	AdcOutM(4) r	AdcOutM(3) r	AdcOutM(2) r	AdcOutM(1) r	AdcOutM(0) r
RegAcCfg0 h0062	Start r0w, 0 global	NelConv(1) rw, 0 global	NelConv(0) rw, 1 global	OSR(2) rw, 0 global	OSR(1) rw, 1 global	OSR(0) rw, 0 global	Cont rw, 0 global	
RegAcCfg1 h0063	IbAmpADC(1) rw, 1 global	IbAmpAdc(0) rw, 1 global	IbAmpPga(1) rw, 1 global	IbAmpPga(0) rw, 1 global	Enable(3) rw, 0 global	Enable(2) rw, 0 global	Enable(1) rw, 0 global	Enable(0) rw, 1 global
RegAcCfg2 h0064	Fin(1) rw, 0 global	Fin(0) rw, 0 global	Pga2Gain(1) rw, 0 global	Pga2Gain(0) rw, 0 global	Pga2Off(3) rw, 0 global	Pga2Off(2) rw, 0 global	Pga2Off(1) rw, 0 global	Pga2Off(0) rw, 0 global
RegAcCfg3 h0065	Pga1Gain rw, 0 global	Pga3Gain(6) rw, 0 global	Pga3Gain(5) rw, 0 global	Pga3Gain(4) rw, 0 global	Pga3Gain(3) rw, 1 global	Pga3Gain(2) rw, 1 global	Pga3Gain(1) rw, 0 global	Pga3Gain(0) rw, 0 global
RegAcCfg4 h0066		Pga3Off(6) rw, 0 global	Pga3Off(5) rw, 0 global	Pga3Off(4) rw, 0 global	Pga3Off(3) rw, 0 global	Pga3Off(2) rw, 0 global	Pga3Off(1) rw, 0 global	Pga3Off(0) rw, 0 global
RegAcCfg5 h0067	Busy r, 0 global	Def wr0	AMux(4) rw, 0 global	AMux(3) rw, 0 global	AMux(2) rw, 0 global	AMux(1) rw, 0 global	AMux(0) rw, 0 global	VMux rw, 0 global

Table 6.14: Acquisition chain control registers

6.15 DACs

Name Address	7	6	5	4	3	2	1	0
RegDasInLsb h0074	DasInLSB(7) w	DasInLSB(6) w	DasInLSB(5) w	DasInLSB(4) w	DasInLSB(3) w	DasInLSB(2) w	DasInLSB(1) w	DasInLSB(0) w
RegDasInMsb h0075	DasInMSB(7) w	DasInMSB(6) w	DasInMSB(5) w	DasInMSB(4) w	DasInMSB(3) w	DasInMSB(2) w	DasInMSB(1) w	DasInMSB(0) w
RegDasCfg0 h0076	NSOrder(1) rw, 0 global	NSOrder(0) rw, 0 global	CodeIMax(2) rw, 0 global	CodeIMax(1) rw, 0 global	CodeIMax(0) rw, 0 global	DasEnable(1) rw, 0 global	DasEnable(0) rw, 0 global	Fin rw, 0 global
RegDasCfg1 h0077							BW rw, 0 global	Inv rw, 0 global
RegDab1In h0078	DabIn(7) w	DabIn(6) w	DabIn(5) w	DabIn(4) w	DabIn(3) w	DabIn(2) w	DabIn(1) w	DabIn(0) w
RegDab1Cfg h0079							Dab1- Enable(1) rw, 0 global	Dab1- Enable(0) rw, 0 global

Table 6.15: DACs control registers

6.16 Vmult and Vld registers

Name Address	7	6	5	4	3	2	1	0
RegVmultCfg0 h007C						Enable rw, 0 global	Fin(1) rw, 0 global	Fin(0) rw, 0 global
RegVldCtrl h007E					VldMult rw, 0 cold	VldTune(2) rw, 0 cold	VldTune(1) rw, 0 cold	VldTune(0) rw, 0 cold
RegVldStat h007F						VldIrq r, 0 global	VldValid r, 0 global	VldEn rw, 0 global

Table 6.16: Vmult and Vld control registers

7 Peripherals

The XE88LC05 includes usual microcontroller peripherals and some other blocks more specific to low-voltage or mixed-signal operation. There are 3 parallel ports, one input port (A), one IO and analog port (B) with analog switching capabilities and one general purpose IO port (C). A watchdog is available, connected to a prescaler. Four 8-bit counters, with capture, PWM and chaining capabilities are available. The UART can handle transmission speeds as high as 115kbaud.

Low-power low-voltage blocks include a voltage level detector, two oscillators (one internal 0.1-2 MHz RC oscillator and a 32 kHz crystal oscillator) and a specific regulation scheme that largely uncouples current requirement from external power supply (usual CMOS ASICs require much more current at 5.5 V than they need at 2.4 V. This is not the case for the XE88LC05).

Analog blocks (ZoomingADC (acquisition path), bias DAC and signal DAC) are defined below. All these blocks operate on 2.4 - 5.5 V power supply range.

7.1 Counters

- 4 8-bit counters
- Daisy chain on 16 bits
- PWM on 8-16 bits
- Capture - compare on 16 bits
- Events and interrupts generation

7.2 Prescaler

- Interrupt generated with 8 millisecond or 1 second period for ultra low power hibernation mode

7.3 Watchdog

- 2 seconds watchdog

7.4 UART

- full duplex operation with buffered receiver and transmitter.
- internal baud rate generator with programmable baud rate (300 - 115000 bauds).
- 7 or 8 bits word length.
- even, odd, or no-parity bit generation and detection
- 1 stop bit
- error receive detection: Start, Parity, Frame and Overrun
- receiver echo mode
- 2 interrupts (receive full and transmit empty)
- enable receive and/or transmit
- invert pad Rx and/or Tx

7.5 Xtal clock

The Xtal Oscillator operates with an external crystal of 32’768 Hz.

symbol	description	min	typ	max	unit	comments
f_clk32k	nominal frequency		32768		Hz	
st_x32k	oscillator start-up time		1	2	s	for full precision
duty_clk32k	duty cycle on the digital output	30	50	70	%	
fstab_1	relative frequency deviation from nominal, for a crystal with CL=8.2 pF and temperature between -40° and +85°C	-100		+300	ppm	not included: crystal frequency tolerance and aging crystal frequency - temperature dependence

Table 7.1: Xtal oscillator specifications.

Note: Board layout recommendations for safer crystal oscillation and lower current consumption:
Keep lines xtal_in and xtal_out short and insert a VSS line between them.
Connect package of the crystal to VSS.
No noisy or digital lines near xtal_in and xtal_out.
Insert guards at VSS where needed.

7.6 RC oscillator

The RC Oscillator is always turned on at power-on reset and can be turned off after the optional Xtal oscillator has been started. The RC oscillator has two frequency ranges: sub-MHz (100KHz to 1MHz) and above-MHz (1MHz to max MCU frequency). Inside a range, the frequency can be tuned by software for coarse and fine adjustment.

Note: No external component is required for the RC oscillator.

The RC oscillator can be in 3 modes. In mode 1(RC on), the RC oscillator and its bias are on. In mode 2 (RC ready), the RC oscillator is off and the bias is on. In mode 3 (RC off), the RC oscillator and the bias are off. RC ready mode is a compromise between power consumption and start-up time.

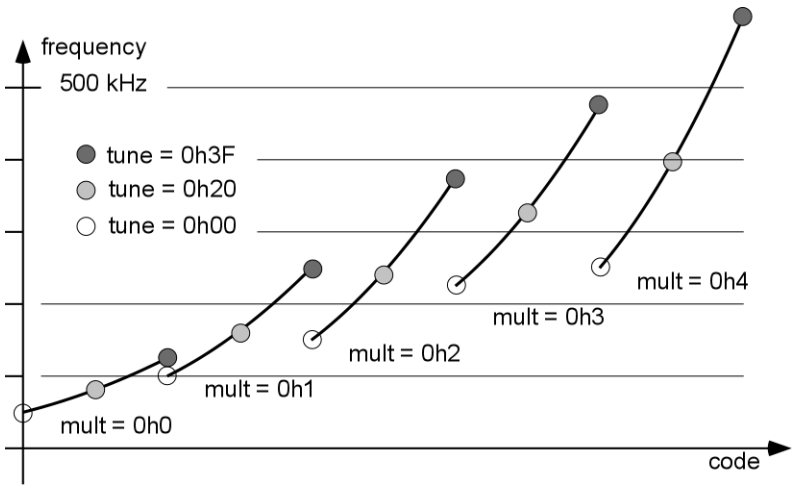


Figure 7.1: RC frequencies programming example for low range (typical values)

symbol	description	min	typ	max	unit	comments
F_{st}	frequency at start-up	50	80	110	kHz	at 27°C
range	range selection	1		10		multiplies F_{st}

Table 7.2: RC specifications

symbol	description	min	typ	max	unit	comments
mult[3:0]	coarse tuning range	1		16		4 bits, multiplies F_{st} * range
tune[5:0]	fine tuning range	0.65		1.5		6 bits, multiplies F_{st} * range * mult
	fine tuning step		1.4	2	%	
T_{st}	start-up time		30	50	ms	bias current is off (RC off)
O_{st}	overshoot at start-up			50	%	bias current is off (RC off)
T_{wu}	wakeup time		3	5	ms	bias current is on (RC ready)
O_{wu}	overshoot at wakeup			50	%	bias current is on (RC ready)
jit	jitter rms		2		$^{o}/_{oo}$	
Tdf	temperature drift		0.1		%/°C	

Table 7.2: RC specifications

7.7 Parallel IO ports

- 8 bit input port A with interrupt, reset and event generation.
- 8 bit input-output-analog port B with analog switching capabilities.
- 8 bit input-output port C.

sym	description	condition	min	typ	max	unit	Comments
	Port A: low threshold limit	Vbat = 2.4 V		1		V	
	Port A: high threshold limit			1.5		V	
	output drop when sinking 1 mA					V	
	output drop when sinking 8 mA				0.4	V	
	output drop when sourcing 1 mA					V	
	output drop when sourcing 8 mA				0.4	V	
	Port A: low threshold limit	Vbat = 5.0 V		2		V	
	Port A: high threshold limit			3		V	
	output drop when sinking 1 mA					V	
	output drop when sinking 8 mA				0.4	V	
	output drop when sourcing 1 mA					V	
	output drop when sourcing 8 mA				0.4	V	
	pull-up, pull-down resistor		50		150	kohm	

Table 7.3: IO pins performances

7.8 Voltage level detector

- Can be switched off, on or simultaneously with CPU activities
- Generates an interrupt if power supply is below a pre-determined level

The Voltage Level Detector monitors the state of the system battery. It returns a logical high value (an interrupt) in the status register if the supplied voltage drops below the user defined level.

symbol	description	min	typ	max	unit	comments	
Vth	Threshold voltage	Note 1			V	trimming values:	
						VldRange	VldTune
			1.53			0	000
			1.44			0	001
			1.36			0	010
			1.29			0	011
			1.22			0	100
			1.16			0	101
			1.11			0	110
			1.06			0	111
			3.06			1	000
			2.88			1	001
			2.72			1	010
			2.57			1	011
			2.44			1	100
			2.33			1	101
			2.22			1	110
			2.13			1	111
T_{EOM}	duration of measurement		2.0	2.5	ms	Note 2	
T_{PW}	Minimum pulse width detected		875	1350	us	Note 2	

Table 7.4: Voltage level detector operation

Note: **1)** Absolute precision of the threshold voltage is ±10%.
2) This timing is respected in case the internal RC or crystal oscillators are selected. Refer to the clock block documentation in case the external clock is used.

8 ZoomingADC

The fully differential acquisition chain is formed of a programmable gain (0.5 - 1000) and offset amplifier and a programmable speed and resolution ADC (example: 12 bits at 4 kHz, 16 bits at 1 kHz). It can handle inputs with very low full scale signal and large offsets.

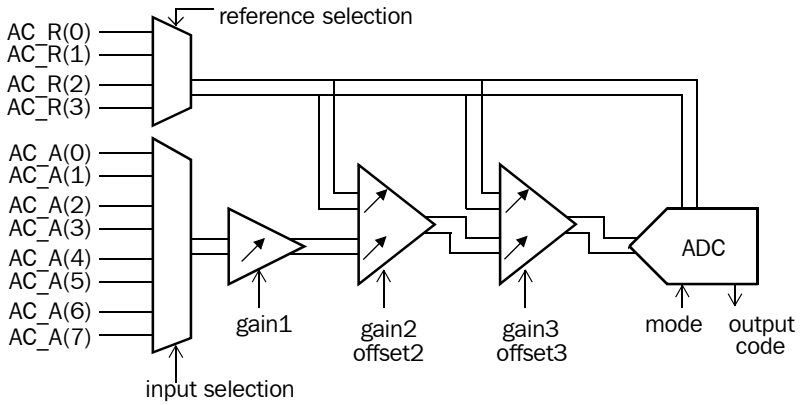


Figure 8.1: Acquisition channel block diagram

Input selection is made from 1 of 4 differential pair or 1 of seven single signal versus AC_A(0). Reference is chosen from the 2 differential references.

The gain of each amplifier is programmed individually. Each amplifier is powered on and off on command to minimize the total current requirement. All blocks can be set to low frequency operation and lower their current requirement by a factor 2 or 4.

The ADC can run continuously (end of conversion signalled by an interrupt, event or by pooling the ready bit), or it can be started on request.

8.1 PGA 1

symbol	description	min	typ	max	unit	Comments
GD1	PGA1 Signal Gain	1		10	-	GD1 = 1 or 10
GD_preci	Precision on gain settings	-5		+5	%	
GD_TC	Temperature dependency of gain settings	-5		+5	ppm/°C	
fs	input sampling frequency			512	kHz	
Zin1	Input impedance	150			kΩ	1
Zin1p	Input impedance for gain 1	1500			kΩ	1
VN1	Input referred noise		28.6		nV/ sqrt(Hz)	2

Table 8.1: PGA1 Performances

Note: 1) Measured with block connected to inputs through AMUX block. Normalized input sampling frequency for input impedance is 512 kHz. This figure has to be multiplied by 2 for fs = 256 kHz and 4 for fs = 128 kHz.
2) Input referred rms noise is 205 uV per input sample with gain = 1, 20.5 uV with gain = 10. This corresponds to 28.6 nV/sqrt(Hz) for fs = 512 kHz and gain = 10.

8.2 PGA2

sym	description	min	typ	max	unit	Comments
GD2	PGA2 Signal Gain	1		10	-	GD2 = 1, 2, 5 or 10
GDoff2	PGA2 Offset Gain	-1		1	FS	
GDoff2_step	GDoff2(code+1) – GDoff2(code)	0.18	0.2	0.22	-	
GD_preci	Precision on gain settings	-5		+5	%	valid for GD2 and GDoff2
GD_TC	Temperature dependency of gain settings	-5		+5	ppm/°C	
fs	Input sampling frequency			512	kHz	
Zin2	Input impedance	150			kΩ	1
VN2	Input referred noise		47.5		nV/ sqrt(Hz)	2

Table 8.2: PGA2 Performances

Note: 1) Measured with block connected to inputs through AMUX block. Normalized input sampling frequency for input impedance is 512 kHz. This figure has to be multiplied by 2 for fs = 256 kHz and 4 for fs = 128 kHz.
2) Input referred rms noise is 340 uV per input sample with gain = 1, 34 uV with gain = 10.This corresponds to 47.5 nV/sqrt(Hz) for fs = 512 kHz and gain = 10.

8.3 PGA3

sym	description	min	typ	max	unit	Comments
GD3	PGA3 Signal Gain	0		10	-	
GDoff3	PGA3 Offset Gain	-5		5	FS	
GD3_step	GD3(code+1) - GD3(code)	0.075	0.08	0.085	-	
GDoff3_step	GDoff2(code+1) – GDoff2(code)	0.075	0.08	0.085	-	
GD_preci	Precision on gain settings	-5		+5	%	valid for GD3 and GDoff3
GD_TC	Temperature dependency of gain settings	-5		+5	ppm/°C	
fs	Input sampling frequency			512	kHz	
Zin3	Input impedance	150			kΩ	1
VN3	Input referred noise		51.0		nV/ sqrt(Hz)	2

Table 8.3: PGA3 Performances

Note: 1) Measured with block connected to inputs through AMUX block. Normalized input sampling frequency for input impedance is 512 kHz. This figure has to be multiplied by 2 for fs = 256 kHz and 4 for fs = 128 kHz.
2) Input referred rms noise is 365 uV per imput sample with gain = 1, 36.5 uV with gain = 10. This corresponds to 51.0 nV/sqrt(Hz) for fs = 512 kHz.

8.4 Analog to digital converter (ADC)

The whole analog to digital conversion sequence is basically made of an initialisation, a set of Nelconv elementary incremental conversions and finally a termination phase(**N_{umCONV}** is set by 2 bits on **RegACCfg0**). The result is a mean of the results of the elementary conversions.

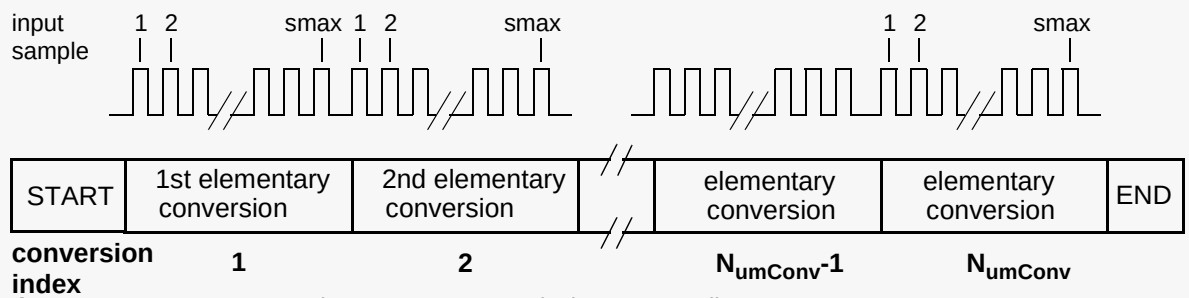


Figure 8.2: Conversion sequence. smax is the oversampling rate.

Note: **N_{umCONV}** elementary conversions are performed, each elementary conversion being made of smax input samples.

$N_{umCONV} = 2^{NELCONV}$

$smax = 8*2^{OSR}$

During the elementary conversions, the operation of the converter is the same as in a sigma delta modulator. During one conversion sequence, the elementary conversions are alternatively performed with direct and crossed PGA-ADC differential inputs, so that when two elementary conversions or more are performed, the offset of the converter is cancelled.

Some additional clock cycles (N_{INIT}+N_{END}) clock cycles are used to initiate and terminate the conversion properly.

8.5 ADC performances

sym	description	min	typ	max	unit	Comments
VINR	Input range	-0.5		0.5	Vref	
Resol	Resolution	6		16	bits	
NResol	Numerical resolution			16	bits	3
DNL	Differential non-linearity	-0.1		0.1	LSB	LSB at 16 bits
INL	Integral non-linearity	-3		2	LSB	2, LSB at 16 bits
fs	sampling frequency	10		512	kHz	
smax	Oversampling Ratio	8		1024	-	1
N_{UMCONV}	Number of elementary conversions in incremental mode	1		8	-	1
Ninit	Number of periods for incremental conversion initialization			5	-	
Nend	Number of periods for incremental conversion termination			5	-	

Table 8.4: ADC Performances

Note: 1) Only powers of 2
2) INL is defined as the deviation of the DC transfer curve from the best fit straight line. This

specification holds over 100% of the full scale.
3) NResol is the maximal readable resolution of the digital filter.

8.6

resolution	conditions	input frequency	conversion time	output frequency
6	oversampling per conversion = 8 1 conversion (no offset rejection)	512 kHz	40 us	25 kHz
8	oversampling per conversion = 16 1 conversion (no offset rejection)	512 kHz	50 us	20 kHz
12	oversampling per conversion = 64 1 conversion (no offset rejection)	512 kHz	150 us	6.7 kHz
13	oversampling per conversion = 64 2 conversions (offset rejection)	512 kHz	275 us	3.6 kHz
16	oversampling per conversion = 256 1 conversion (no offset rejection)	512 kHz	500 us	2 kHz
16	oversampling per conversion = 256 2 conversions (offset rejection)	512 kHz	1 ms	1 kHz
16	oversampling per conversion = 1024 8 conversion s(offset rejection)	512 kHz	16.5 ms	60 Hz

Table 8.5: ADC performances examples

8.7 Linearity

To quantify linearity errors, Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) were measured for the ADC alone and for gains of 1, 5, 10, 20, 100, 1000, and a resolution of 12 bits and 16 bits.

INL is defined as the deviation (in LSB) of the DC transfer curve of each individual code from the best-fit straight line. This specification holds over the full scale.

DNL is defined as the difference (in LSB) between the ideal (1 LSB) and measured code transitions for successive codes. INL and DNL are specified after gain and offset errors have been removed.

8.8 Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) for <u>12-bit resolution</u>

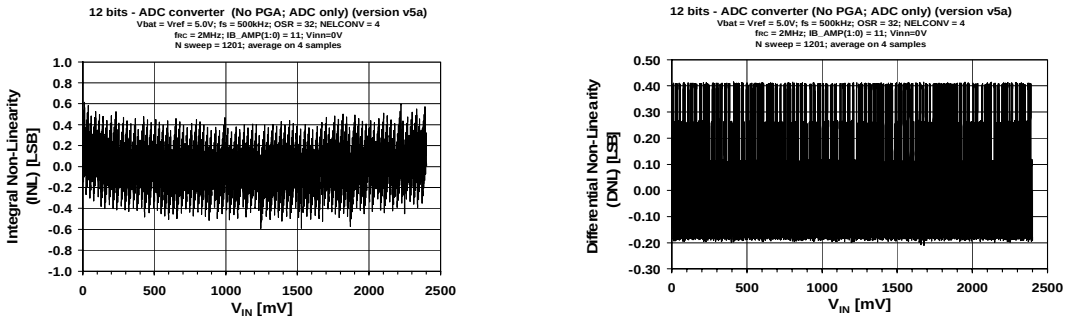
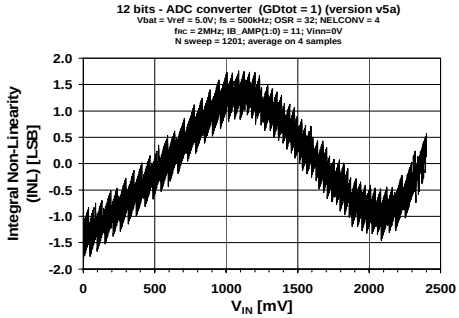


Figure 8.3: NO GAIN (ONLY ADC), 12 bit ADC setting



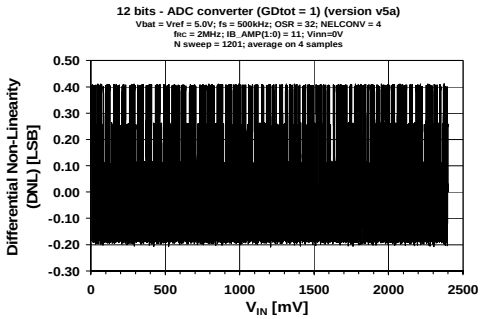
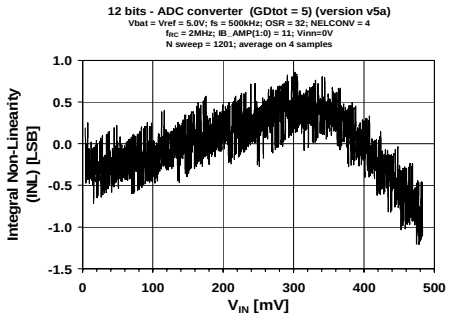


Figure 8.4: GAIN=1, 12 bit ADC setting



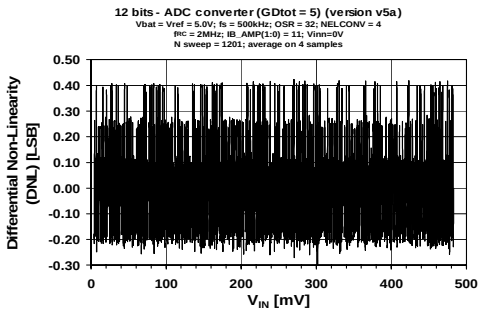
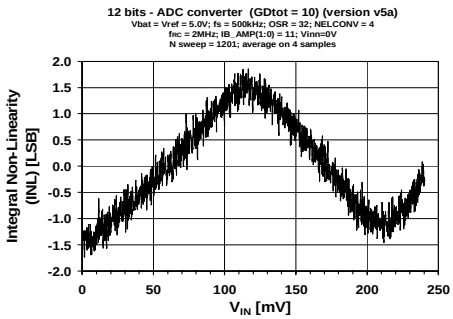


Figure 8.5: GAIN=5, 12 bit ADC setting



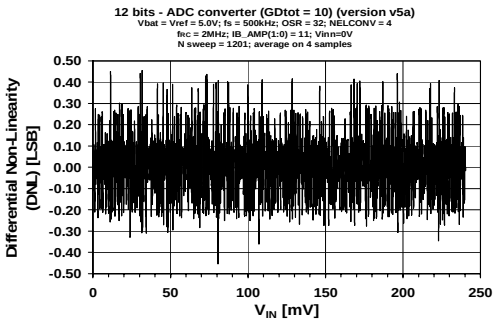
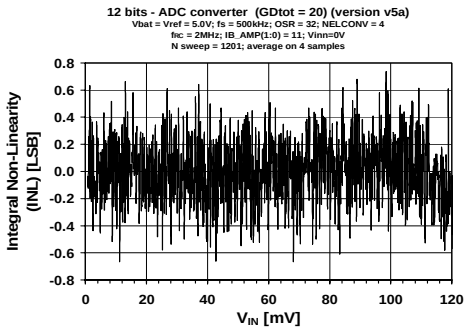


Figure 8.6: GAIN=10, 12 bit ADC setting



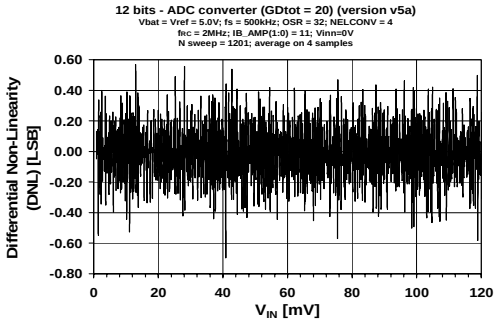
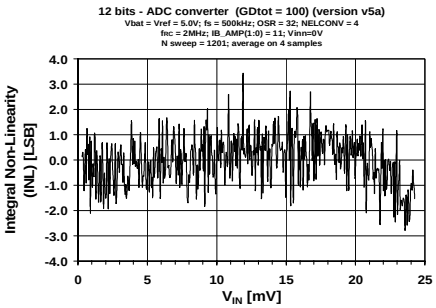


Figure 8.7: GAIN=20, 12 bit ADC setting



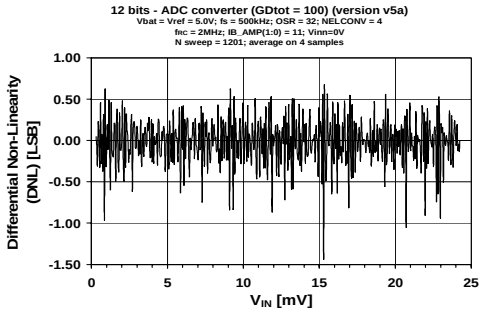
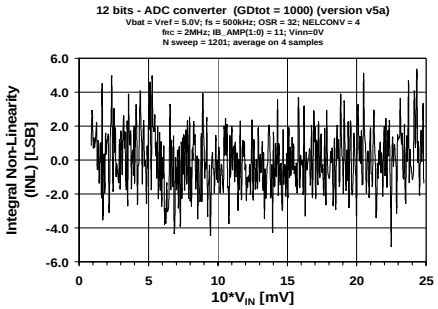


Figure 8.8: GAIN=100, 12 bit ADC setting



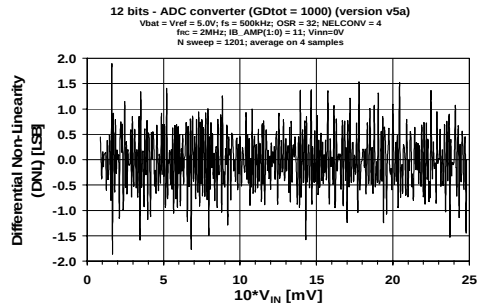


Figure 8.9: GAIN=1000, 12 bit ADC setting

8.9 Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) for 16-bit resolution

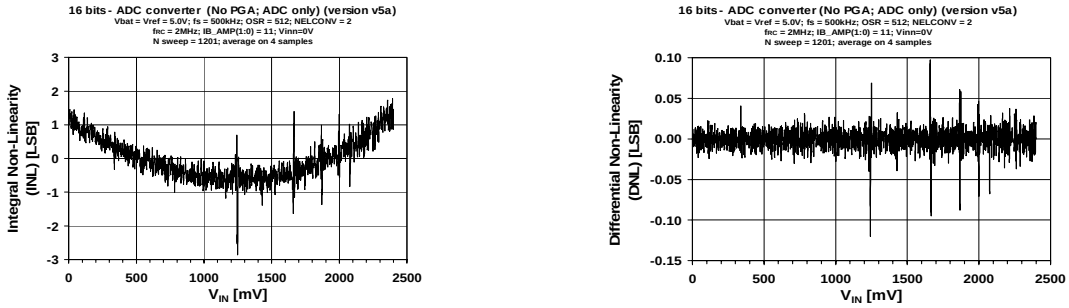


Figure 8.10: NO GAIN (ONLY ADC), 16 bit ADC setting

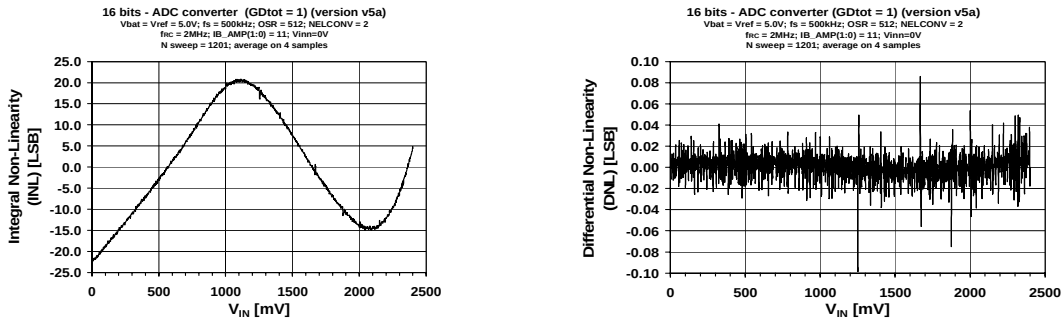


Figure 8.11: GAIN=1, 16 bit ADC setting

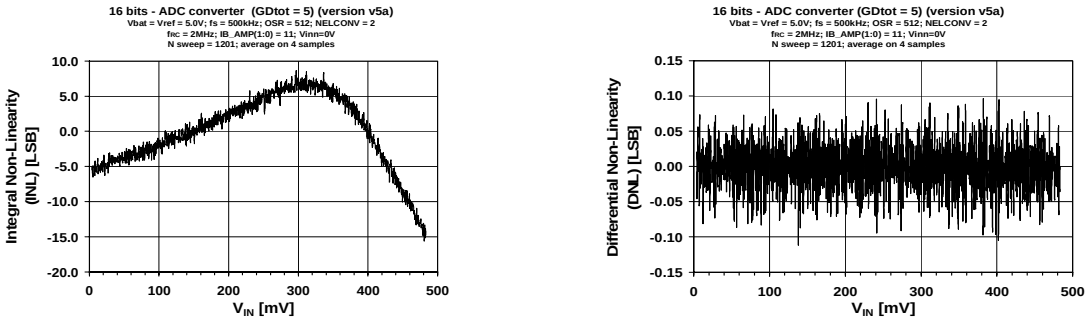


Figure 8.12: GAIN=5, 16 bit ADC setting

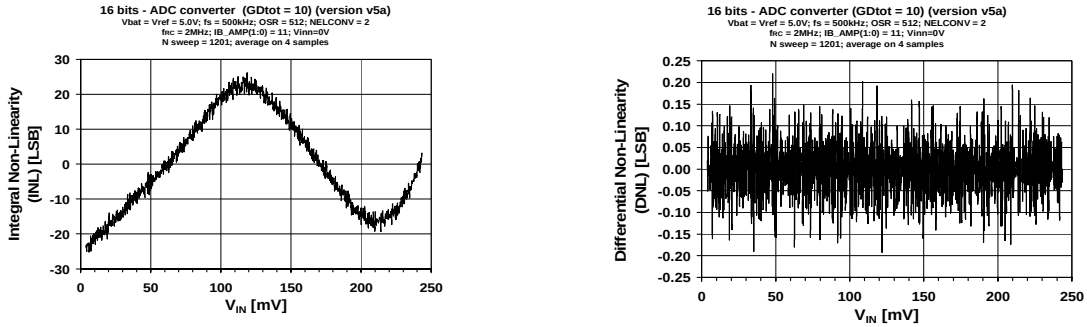


Figure 8.13: GAIN=10, 16 bit ADC setting

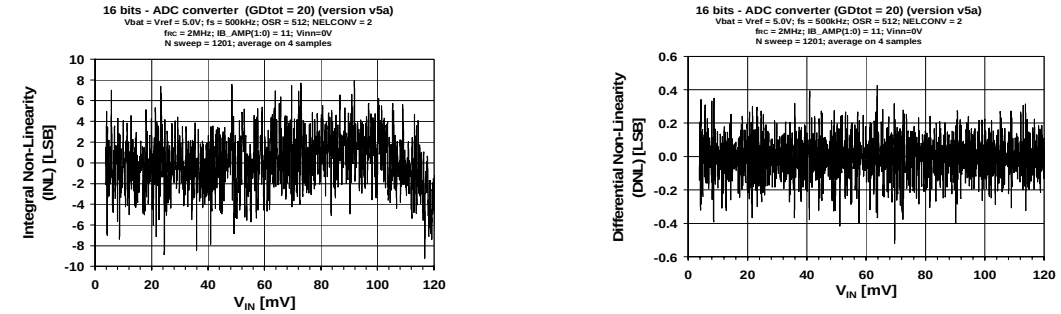


Figure 8.14: GAIN=20, 16 bit ADC setting

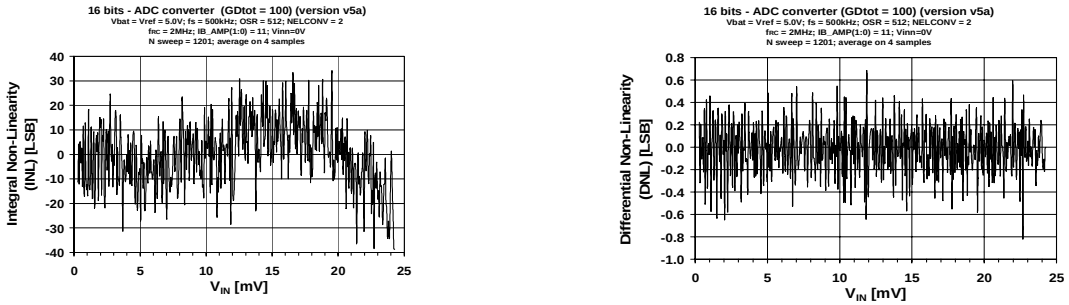


Figure 8.15: GAIN=100, 16 bit ADC setting

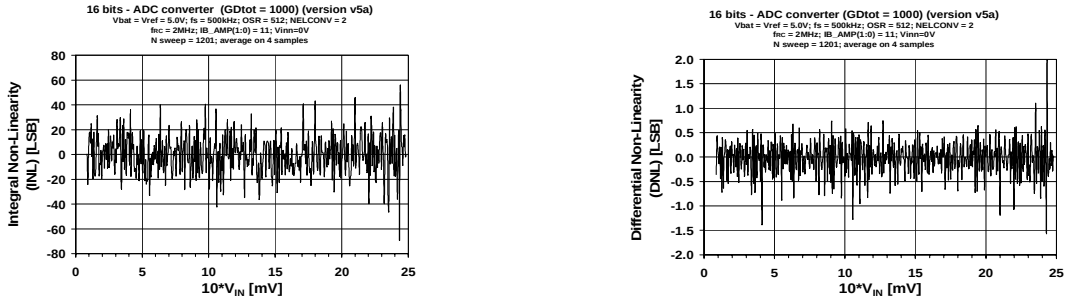


Figure 8.16: GAIN=1000, 16 bit ADC setting

The gain settings of each PGA stage for the plots of above figure are those of the table below.

PGA Gain GD_{TOT} (V/V)	PGA1 Gain GD1 (V/V)	PGA2 Gain GD2 (V/V)	PGA3 Gain GD3 (V/V)
1	1	bypassed	bypassed
5	1	5	bypassed
10	10	bypassed	bypassed
20	10	2	bypassed
100	10	10	bypassed
1000	10	10	10

Table 8.6: Individual PGA gains for INL & DNL measurements
Table 8.7:

8.10 Noise

Ideally, a constant input voltage V_{IN} should result in a constant output code. However, because of circuit noise, the output code may vary for a fixed input voltage. The figure shows the distribution for the ADC alone (PGA1, 2, and 3 bypassed) and of several configurations of the PGAs. Quantization noise is dominant in this case of ADC only, and, thus, the ADC thermal noise is negligible.

One has to considere two points when computing final noise of the acquisition chain:

- this is a type of amplifier (switched-cap with constant capacitive load) that maintains its output noise when changing the gain. Therefore input refered noise is lowered when the gain of an amplifier is increased.
- the ADC is oversampled, and the number of samples taken lowers the thermal noise

Total input refered noise can be computed using the following equation:

$$V^2_{n,in} = \frac{\left(\frac{V_{n,out1}}{gain1}\right)^2 + \left(\frac{V_{n,out2}}{gain1 \cdot gain2}\right)^2 + \left(\frac{V_{n,out3}}{gain1 \cdot gain2 \cdot gain3}\right)^2}{numconv \cdot smax}$$

Where $V_{n,outx}$ is the rms output noise of amplifier x.

Amplifier	Symbol	Typical output noise per over-sample	Unit
PGA1	$V_{n,out1}$	205	uVrms
PGA2	$V_{n,out2}$	340	uVrms
PGA3	$V_{n,out3}$	365	uVrms

Typical output noise of ZoomingADC preamplifiers

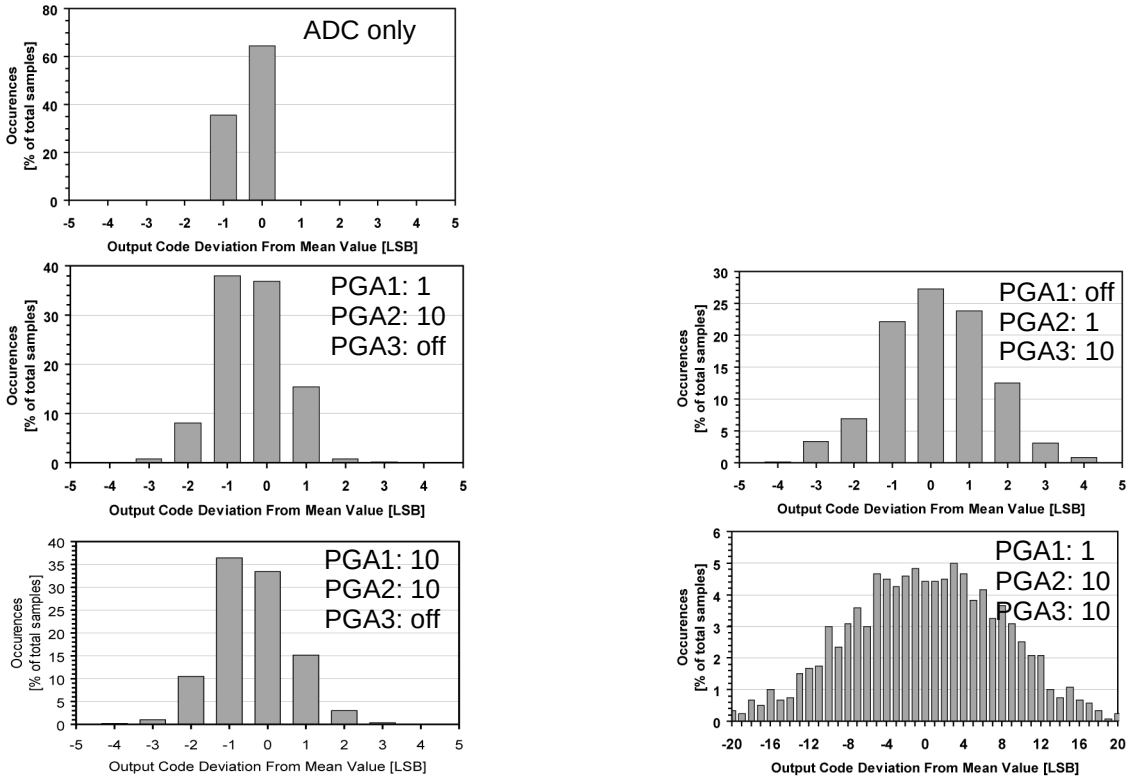


Figure 8.17: Noise measured at the output of the ZoomingADC

As one can see on the figures above, increase the gain of the first amplifier lowers the output noise for constant global gain. It also lowers sensitivity to temperature drift as offset is better compensated on first amplifier.

8.11 Gain Error and Offset Error

Gain error is defined as the amount of deviation between the ideal transfer function and the measured transfer function (with the offset error removed). The left figure shows gain error vs. temperature for different PGA gains. The curves are expressed in% of Full-Scale Range (FSR) normalized to 25°C.

Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). The measured offset errors vs. temperature curves for different PGA gains are depicted in the right figure below. The output offset error, expressed in (LSB), is normalized to 25°C.

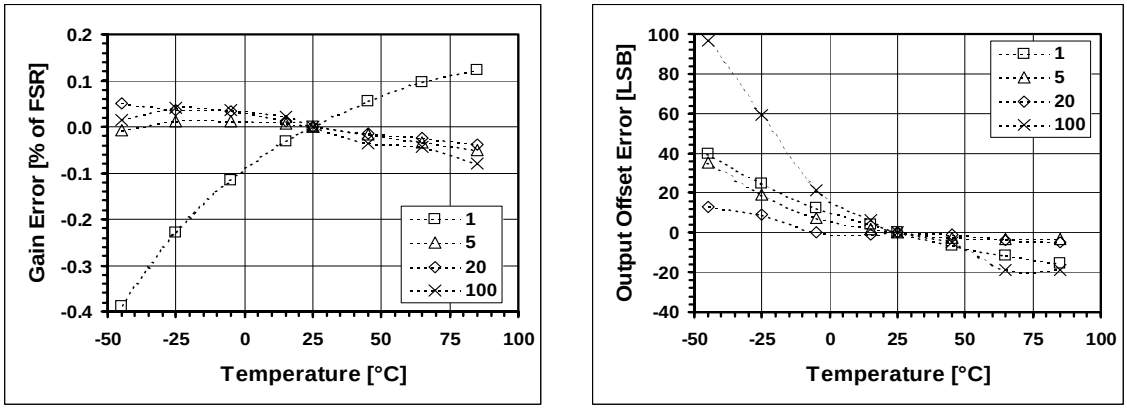


Figure 8.18: Gain and offset error vs temperature for several gains, normalized to 25°C, offset cancellation disabled. When the offset cancellation is enabled, the offset of PGA1 and ADC

8.12 Power Consumption

Left figure below plots the variation of quiescent current consumption with supply voltage V_{DD}, as well as the distribution between the 3 PGA stages and the ADC. As shown in the right figure, quiescent current consumption is not greatly affected by sampling frequency. It can be seen that the quiescent current varies by about 20% between 100kHz and 2MHz. Quiescent current consumption vs. temperature is shown in the second set of figures, showing a relative increase of nearly 40% between -45 and +85°C.

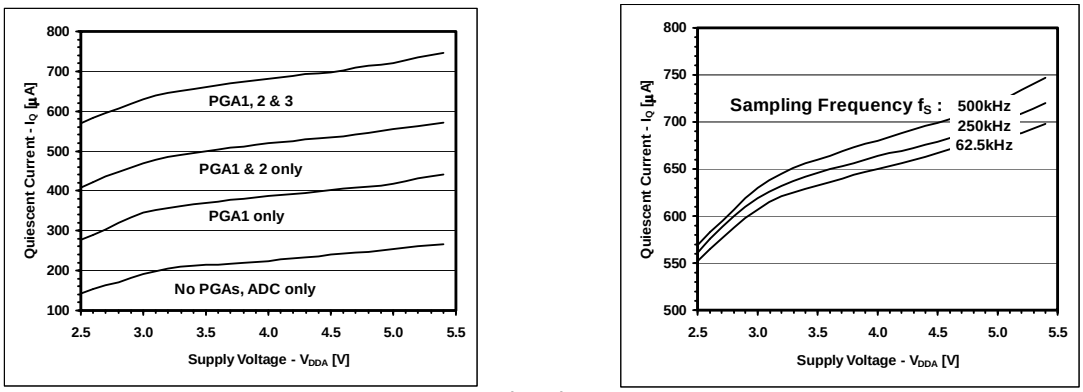


Figure 8.19: Quiescent current versus supply voltage for different gains and clock speed (not using the PGA and ADC low power modes)

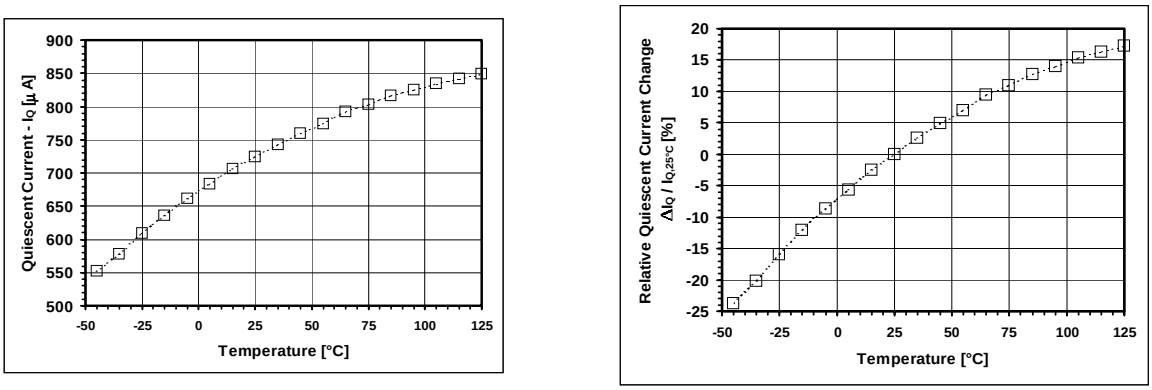


Figure 8.20: Absolute and (b) relative change in quiescent current consumption vs. temperature

Supply	ADC	PGA1	PGA2	PGA3	TOTAL	Unit
V_{DD} = 5V	250	165	130	175	720	µA
V_{DD} = 3V	190	150	120	160	620	µA

Table 8.8: Typical quiescent current distributions in acquisition chain (n = 16 bits, f_S = 500kHz)

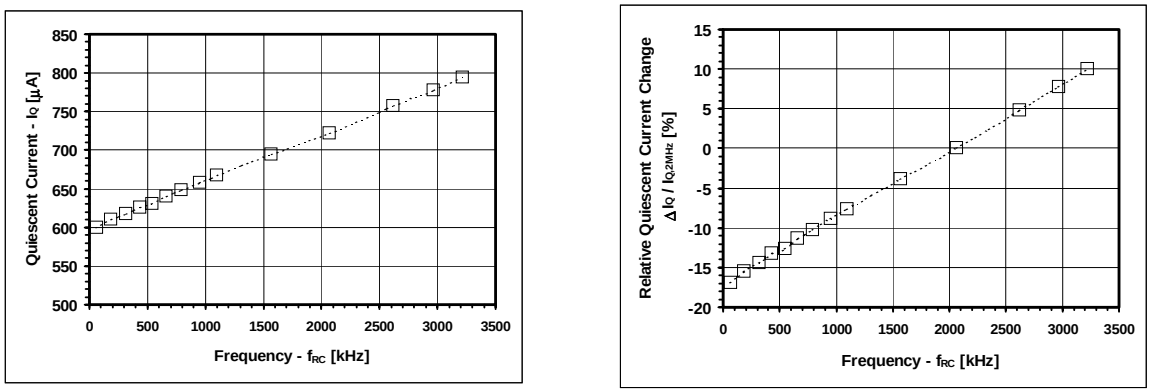


Figure 8.21: Absolute and (b) relative change in quiescent current consumption vs. clock speed

8.13 Power Supply Rejection Ratio

Figure below shows power supply rejection ratio (PSRR) at 3V and 5V supply voltage, and for various PGA gains. PSRR is defined as the ratio (in dB) of voltage supply change (in V) to the change in the converter output (in V). PSRR depends on both PGA gain and supply voltage V_{DD}.

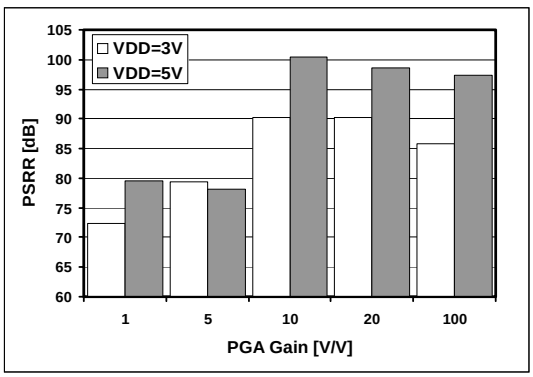


Figure 8.22: Power supply rejection ratio (PSRR)

Supply	GAIN = 1	GAIN =5	GAIN = 10	GAIN = 20	GAIN =100	Unit
V_{DD} = 5V	79	78	100	99	97	dB
V_{DD} = 3V	72	79	90	90	86	dB

Table 8.9: PSRR (n = 16 bits, $V_{IN} = V_{REF} = 2.5V$, $f_S = 500kHz$)

8.14 Frequency Response

The incremental ADC of the XE88LC05 is an over-sampled converter with two main blocks: an analog modulator and a low-pass digital filter. The main function of the digital filter is to remove the quantization noise introduced by the modulator. As shown below, this filter determines the frequency response of the transfer function between the output of the ADC and the analog input V_{IN}. Notice that the frequency axes are normalized to one elementary conversion

period OSR/f_S. The plots below also show that the frequency response changes with the number of elementary conversions N_{ELCONV} performed. In particular, notches appear for N_{ELCONV} Š 2. These notches occur at:

$$f_{NOTCH}(i) = \frac{i \cdot f_S}{OSR \cdot N_{ELCONV}} \text{ (Hz)for } i = 1,2,...,(N_{ELCONV} - 1)$$

and are repeated every f_S/OSR.

Information on the location of these notches is particularly useful when specific frequencies must be filtered out by the acquisition system. For example, consider a 5Hz-bandwidth, 16-bit sensing system where 50Hz line rejection is needed. Using the above equation and the plots below, we set the 4th notch for N_{ELCONV} = 4 to 50Hz, i.e. 1.25Þf_S/OSR = 50Hz. The sampling frequency is then calculated as f_S = 20.48kHz for OSR = 512. Notice that this choice yields also good attenuation of 50Hz harmonics.

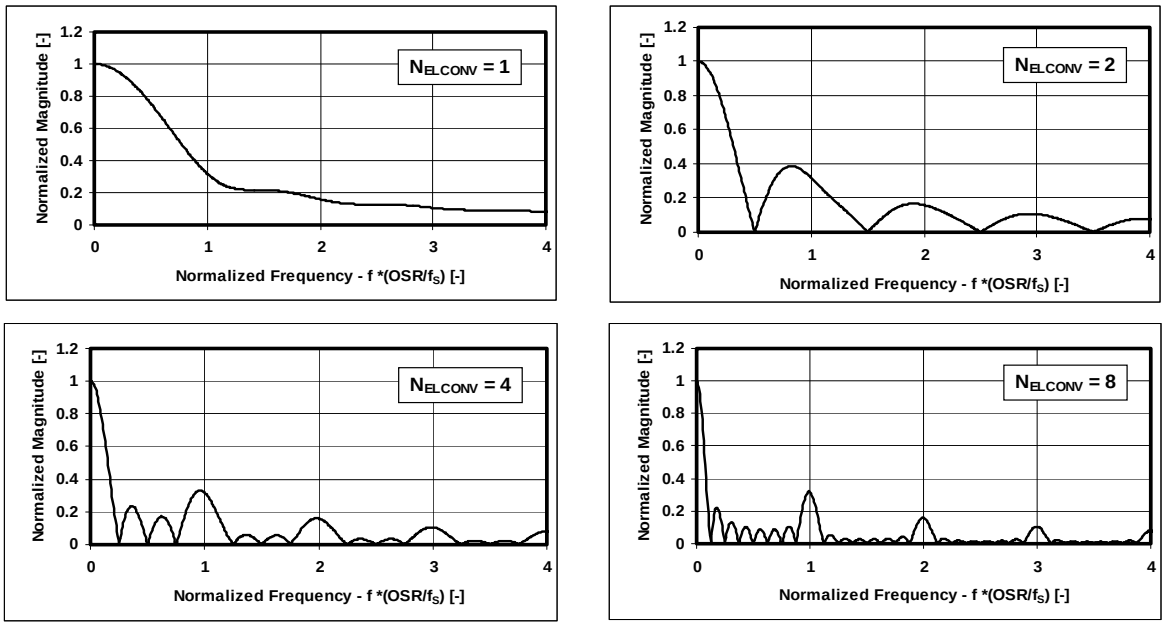


Figure 8.23: Frequency response: normalized magnitude vs. frequency for different N_{ELCONV}

9 Digital to analog converters (DACs)

The XE88LC05 includes 2 DACs: a signal DAC and a bias DAC.

9.1 Bias DAC

The bias DAC is a low resolution (8 bits) DAC with a buffer perfectly adapted to sensor bridge bias. It can be used to bias a bridge in current (figure) or in voltage by choosing the pins connection.

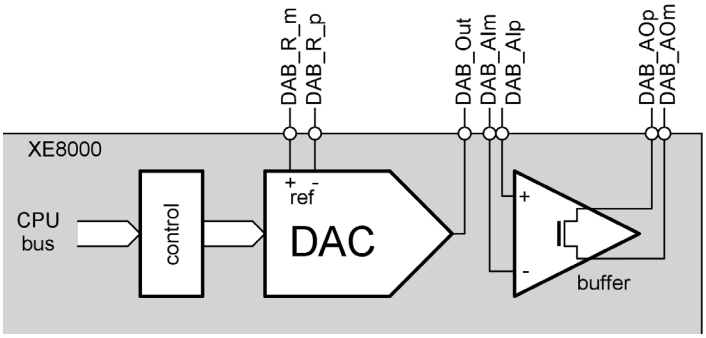


Figure 9.1: General block diagram of the bias DAC

The bias DAC itself is built of a series of resistors which two extremes are available outside the chip, so that one can connect it to an external source when the output of the DAC should not be ratiometric to the power supply.

9.2 The DAC of bias DAC

The DAC convertor is a resistive divider connected between pads DAB_R_m and DAB_R_p.

sym	description	min	typ	max	unit	Comments
wda	number of input bits		8		bits	
tstep	step response			100	ms	1
range	DAC output range	DAB_R_m		DAB_R_p		2
INL	integral non-linearity			1	LSB	3
DNL	differential non-linearity			1	LSB	3

Table 9.1: DAC performances

Note: 1) Time to reach the final value within 5%. Node not charged.
2) In most cases DAB_R_m will be connected to VSS and DAB_R_p to VDD.
3) For DAB_R_m connected to VSS and DAB_R_p to VDD, VDD > 2.4 V.

9.3 The amplifier of bias DAC

The amplifier can be used in several configurations as for biasing a bridge in voltage or current. Application examples are given in application note AN8000.03.

sym	description	min	typ	max	unit	Comments
gain	gain at DC	60			dB	1
GBW	gain bandwidth product	100			Hz	1

Table 9.2: Amplifier performances

sym	description	min	typ	max	unit	Comments
fm	phase margin	60			°	1
rl	resistive load	300		100000	ohm	4,5
cl	capacitive load			1	nF	
CMR	common mode input range	vss		vdd	V	
OR	output range	vss+0.2		vdd-0.2	V	3
outp vr	outp pin voltage range	vss+2.3		vdd	V	
voff	offset			±10	mV	
noise	integrated input noise			100	uVrms	
isourc	max source current			10	mA	4
PSRR	power supply rejection ratio	40			dB	2
ibias	quiescent bias current		2	5	uA	5
ioff	off current			1	uA	

Table 9.2: Amplifier performances

Note: 1) For all possible combinations of resistive load and capacitive load.
2) At DC.
3) For voltage controlled bias control. For current controlled operation the voltage drop on the pMOS output transistor has to be less than 200mV at maximum current.
4) Short circuit protection at ~80mA.
5) This amplifier must be loaded for correct operation. Ibias is without load current.

9.4 Signal DAC

The signal DAC is build around a programmable DAC and a buffer. It can generate fast (up to 64 kHz) or high resolution (resolution up to 16 bits) output. The output can be controlled in current or voltage.

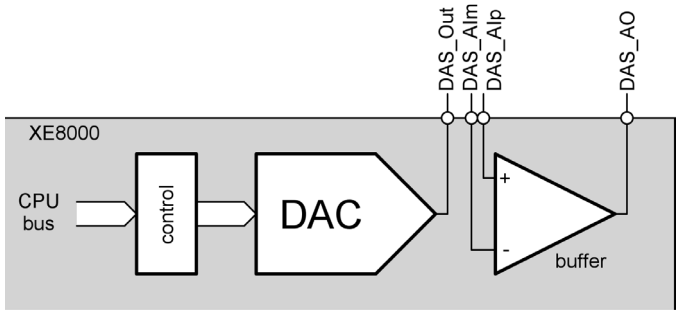


Figure 9.2: General block diagram of the signal DAC

9.5 The amplifier of signal DAC

The amplifier can be used in several configurations. Therefore, it is not connected internally.

sym	description	min	typ	max	unit	Comments
gain	gain at DC	80			dB	1
GBW0	gain bandwidth product	25			kHz	4
cl0	capacitive load			5	nF	4
GBW1	gain bandwidth product	125			kHz	5
cl1	capacitive load			200	pF	5
fm	phase margin	55			°	6
rl	resistive load	5			kohm	3
SR	slew rate	10			kV/s	7
CMR	common mode input range	vss-0.2		vdd-1.2	V	
OR	output range	vss+0.2		vdd-0.2	V	

Table 9.3: DAC signal amplifier performances

sym	description	min	typ	max	unit	Comments
voff	offset			±5	mV	
CMRR	common mode rejection	60			dB	2
noise	integrated input noise			100	uVrms	
ibias	quiescent bias current		200	500	uA	
ioff	off current			1	uA	

Table 9.3: DAC signal amplifier performances

Note:
1) For the minimal resistive load and the maximal capacitive load
2) At DC
3) Short circuit protection at ~5mA.
4) GBW when the maximal load is cl0 and with the bit BW=0
5) GBW when the maximal load is cl1 and with the bit BW=1
6) In both cases BW=0 and BW=1 for the maximal capacitive load and the minimal resistive load.
7) For maximal load cl0, BW=0 and maximal resistive load rl

9.6 The DAC of signal DAC

The DAC of signal DAC can be used as a regular PWM DAC (NSorder set to 00), or a sigma-delta DAC (first or second order). The most efficient setting is the second order sigma-delta (NSorder set to 10), and this is the mode that we describe below. In order to function according to the following computation, it must be followed by a second order filter or larger with a given cut-off frequency.

Note: The DAC output is ratiometric to power supply. It is highly important to avoid parasitic on power supply. It is recommended to have no heavy switching on output ports for precise DAC output.

The D/A resolution in bits is given by (second order filter):

$$resolution(bit) = -0.226 + m + (NSorder \cdot (q - 2.65))$$

with:

m = PWM resolution in bits (4 .. 11)

code_lmax	m (PWM resolution in bits)
000	4
001	5
010	6
011	7
100	8
101	9
110	10
111	11

Table 9.4: PWM resolution setting

NSorder = order of the noise shaper = (0 .. 2)

ns_order(1:0)	Noise shaping order
00	0
01	1
1x	2

Table 9.5: Noise shaper order setting

q = ratio between the pulse repetition frequency (*fs*) and the cut-off frequency of the external low pass filter (*fc*)

$$q = \log_2((fs)/(fc))$$

fs = PWM pulse repetition frequency

$$fs = \frac{(frc)/(fdiv)}{2^m}$$

with *frc* the RC oscillator frequency; *fdiv* is the division factor of the *frc* as set by **FIN**.

FIN(1:0)	RC clock division factor: *fdiv*
0	1
1	2

Table 9.6: RC clock division factor

Example: f_{RC} =2MHz, FIN=1, m=4, *fc*=1kHz, *NSorder*=2 and therefore, the resolution is:

$$fs = 2MHz/2^4 = 125kHz$$
$$q = \log_2(125kHz/1kHz) = 6.96$$
$$resolution = -0.226 + 4 + 2*(6.96 - 2.65) = 12.4bit$$

Settings					Performances		
frc	fin	m	fc	ns	fs	q	resolution
Hz			Hz		Hz		bits
2’000’000	1	4	4’000	2	125’000	4.97	8.4
2’000’000	1	4	2’000	2	125’000	5.97	10.4
2’00’0000	1	4	1’000	2	125’000	6.97	12.4
2’000’000	1	4	500	2	125’000	7.97	14.4
2’000’000	1	4	250	2	125’000	8.97	16.0
2’000’000	1	5	1’000	2	62’500	5.97	11.4
2’000’000	1	6	1’000	2	31’250	4.97	10.4
2’000’000	1	11	250	2	977	1.97	9.4
2’000’000	2	4	1’000	2	62’500	5.97	10.4

Table 9.7: Examples of resolution for different settings of the signal DAC and of the filter

10 Physical description

10.1 LQFP64 package

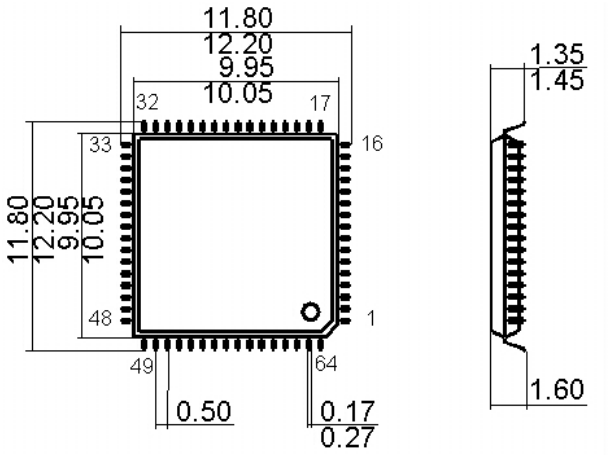


Figure 10.1: LQFP64 package, size in mm.

10.2 Die

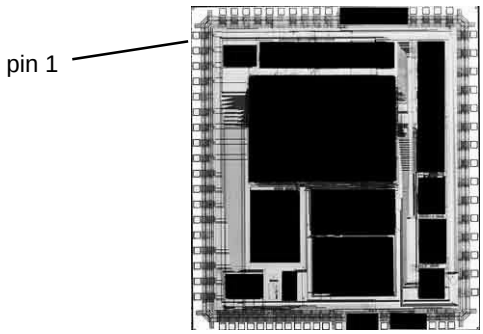


Figure 10.2: Die. Chip size is 4.2 x 4.7mm2 for 0.3 mm thickness.
Physical chip size and exact pad positioning can change without notification.

10.2.1 Bonding pad location

Coordinates start with a point near to the bottom left border (with respect to above picture). X is horizontal, Y is vertical.

Pad size is 85 x 85 um.

Symbol	Pad	X	Y	Symbol	Pad	X	Y
		um	um			um	um
1	PA(0)	52.6	4123.5	33	NC	3363.5	47.6
2	PA(1)	52.6	3908.5	34	DAB_AI_p	3498.5	47.6
3	PA(2)	52.6	3693.5	35	DAB_AI_n	3628.5	47.6
4	PA(3)	52.6	3478.5	36	TEST	3958.4	508.5
5	NC	52.6	3263.5	37	AC_R(3)	3958.4	768.5
6	PA(4)	52.6	3048.5	38	AC_R(2)	3958.4	1028.5
7	PA(5)	52.6	2833.5	39	AC_A(7)	3958.4	1283.5
8	PA(6)	52.6	2618.5	40	AC_A(6)	3958.4	1543.5
9	PA(7)	52.6	2403.5	41	AC_A(5)	3958.4	1798.5
10	PC(0)	52.6	2188.5	42	NC	3958.4	2058.5
11	PC(1)	52.6	1973.5	43	AC_A(4)	3958.4	2313.5
12	PC(2)	52.6	1758.5	44	AC_A(3)	3958.4	2573.5
13	PC(3)	52.6	1543.5	45	AC_A(2)	3958.4	2828.5
14	NC	52.6	1328.5	46	AC_A(1)	3958.4	3088.5
15	PC(4)	52.6	1113.5	47	AC_A(0)	3958.4	3343.5
16	PC(5)	52.6	898.5	48	NC	3958.4	3603.5
17	PC(6)	52.6	683.5	49	AC_R(1)	3958.4	3858.5
18	PC(7)	52.6	468.5	50	AC_R(0)	3958.4	4118.5
19	PB(0)	398.5	47.6	51	DAS_Out	3628.5	4453.4
20	PB(1)	533.5	47.6	52	DAS_AI_p	3458.5	4453.4
21	PB(2)	668.5	47.6	53	DAS_AI_n	3293.5	4453.4
22	PB(3)	798.5	47.6	54	DAS_AO	3114.6	4453.4
23	PB(4)	933.5	47.6	55	Vbat	1923.5	4453.4
24	NC	1063.5	47.6	56	Vss	1753.5	4453.4
25	PB(5)	1198.5	47.6	57	Vss_Vreg	1588.5	4453.4
26	PB(6)	1328.5	47.6	58	Vreg	1418.5	4453.4
27	PB(7)	1463.5	47.6	59	Vmult	1252.9	4453.4
28	DAB_R_p	1593.5	47.6	60	RESET	1088.5	4453.4
29	DAB_R_n	1728.5	47.6	61	OscOut	923.5	4453.4
30	DAB_Out	1858.5	47.6	62	NC	758.5	4453.4
31	DAB_AO_p	2042.4	47.6	63	OscIn	593.5	4453.4
32	DAB_AO_n	2683.3	47.6	64	Vss	428.5	4453.4

Table 10.1: Bonding pads location. Do not connect pads named NC. Pins 56, 57 and 64 must be connected to VSS.

11 Contacting XEMICS

11.1 Web site:

http://www.xemics.com

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You will find more information about the XE88LC05 and other XEMICS products, as well as the addresses of our representatives and distributors for your region on www.xemics.com.